

CXD5602 User Manual

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1 Introduction

1.1 Introduction

This manual is intended for CXD5602 users.

1.2 Notation

1.2.1 Notation of numerical value

The table below shows notation of numerical values used in this document.

Table Notation-1 Notation of Numerical Value

Base	Notation	Example
Base 16	adds prefixed "0x"	0x2A
	or, adds prefixed "<bit width>'h"	8'h2A
Base 10	describes numerical value only	256
Base 2	adds prefixed "<bit width>'b"	4'b1010

Numerical numbers are noted in the format shown below when the status of the signal (signed/unsigned) and the position of the decimal point should be indicated.

- [sign][bit number of integer part].[bit number of decimal part]

In the [sign], U or S is described. U represents unsigned, and S, signed.

- When the sign is U, bit number of integer part plus bit number of decimal part equals the total bit number.
- When the sign is S, 1(sign bit) plus bit number of integer part plus bit number of decimal part equals the total bit number.

The notation examples are as follows.

- 5-bit unsigned signal with integer number is noted as U5.0.
- 5-bit unsigned signal with decimal point [1].[0] position is noted as U4.1.
- 5-bit unsigned signal with decimal point [-1].[-2] position is noted as U6.-1.
- 5-bit signed signal with integer number is noted as S4.0.
- 5-bit signed signal with decimal point [1].[0] position is noted as S3.1.

2 CXD5602 Outline

2.1 Introduction

CXD5602GF/GG is a 32 bit RISC low power microprocessor solution for wearable applications. It is based on the Arm® Cortex®-M4 processor with FPU 32 bit RISC and It integrates Arm® Cortex®-M0+ 32 bit RISC specifically for the system controller (power management, clock, reset) and I/O processor. It incorporates embedded 1.5 MByte of SRAM, 64 KByte of backup SRAM, and 256 KByte of I/O processor SRAM.

The Arm® Cortex®-M4 processor with FPU and Arm® Cortex®-M0+ are power-gated by the Power Management Unit, respectively, that is, the CPUs are powered off by internal power switches. Processor SRAMs are able to retain data, and it's possible to restart processors quickly.

To provide optimized hardware performance for sensor fusion and audio processing services, the device integrates ultra-low power GNSS Domain, Audio Codec Domain and Sensor Domain. Integrated Audio Codec Domain supports digital noise cancelling and digital equalizer. Sensor Domain provides the specialized engine for sensor processing.

Eliminating the need for a discrete sensor hub, these features enable various sensor applications (activity recognition, voice recognition, etc.) low power audio applications such as music playback (MP3 decode, Bluetooth A2DP, etc.) and hands-free communication (Bluetooth HFP).

2.2 Features

The features of CXD5602GF/GG are:

- Application Processor
 - Arm® Cortex®-M4 processor with FPU 32 bit RISC
 - Operating frequency up to 156 MHz
- 1.5 MByte Application Memory
- Application Multi-layer Bus
 - 32 bit Multi-layer bus architecture
 - Application Domain for Arm® Cortex®-M4 processor with FPU 32 bit RISC, Audio Codec, Connectivity, Storage and Image Block
- Audio Codec
 - Digital Equalizer (DEQ)
 - Two I2S Interfaces supported
 - Unique Audio Data Format (Pulse Density Modulation) between CXD5602GF/GG and CXD5247GF
- 8 bit parallel Camera Interface supported
- 2D Graphics Acceleration

- BitBLT, Rotate, Scaling, Blender
 - Connectivity/Storage Interface
 - On-chip USB2.0 Device supported
 - eMMC 4.41 for eMMC Device
 - SD3.0 Host Controller interface
 - SPI and SDIO support for external Wi-Fi transceivers
 - UART support for external Bluetooth transceivers
 - Quad SPI-FLASH Interface
 - Display Interface
 - SPI Interface up to 40.96 Mbps
 - 8/16/24/32 bpp LCD or E-Ink recommend up to QVGA resolution
 - System and I/O Processor (SYSCPU)
 - Arm® Cortex®-M0+ 32 bit RISC
 - Operating frequency up to 100 MHz at 1.0 V
 - 256 KByte SRAM
 - 128 KByte ROM for secure booting
 - System and IOP Domain multi-layer bus
 - 32 bit Multi-layer bus architecture
 - SYSIOP for Arm® Cortex®-M0+ 32 bit RISC, PMU, GNSS, Sensor engine, HostIF, Configurable IO
 - Power management
 - I2C and GPIO interface connections to Power Management IC (assuming CXD5247GF)
 - power on reset
 - power gate control
 - Clock and Reset management
 - X'tal, RTC, RCOSC, PLL
 - 64 KByte Backup SRAM
 - Timer
 - RTC
 - A general-purpose 32 bit timer each Processor Unit
 - Host Interface
 - I2C, SPI or UART interface
 - 1 KByte Host communication Memory
 - Sensor engine
 - SPI and Two I2C Interfaces
 - 40 KByte Sensory Data FIFO
 - Pre-processing unit for sensor fusion
 - Up to Four PWMs
 - ADCs
 - Four channel 10 bit low power ADC
-

Two channels 10 bit high performance ADC

- Multi-GNSS Controller
 - Arm® Cortex®-M4 processor with FPU 32 bit RISC
 - Operating frequency up to 98.208 MHz
 - 64 KByte ROM
 - 640 KByte SRAM
 - CORDIC engine for GNSS support
- Multi-GNSS receiver
 - GPS (L1 C/A)
 - GLONASS (L1OF)
 - QZSS (L1 C/A, L1 SAIF)
 - SBAS (L1 C/A)
 - WAAS, EGNOS, MSAS
 - BeiDou (B1)
 - Galileo (E1 CBOC)
- Configurable I/O
 - I2C/SPI/GPIO Interfaces
- Debug
 - Serial wire debug (SWD), Embedded Trace Macrocell
 - UART supported

2.3 Block Diagram

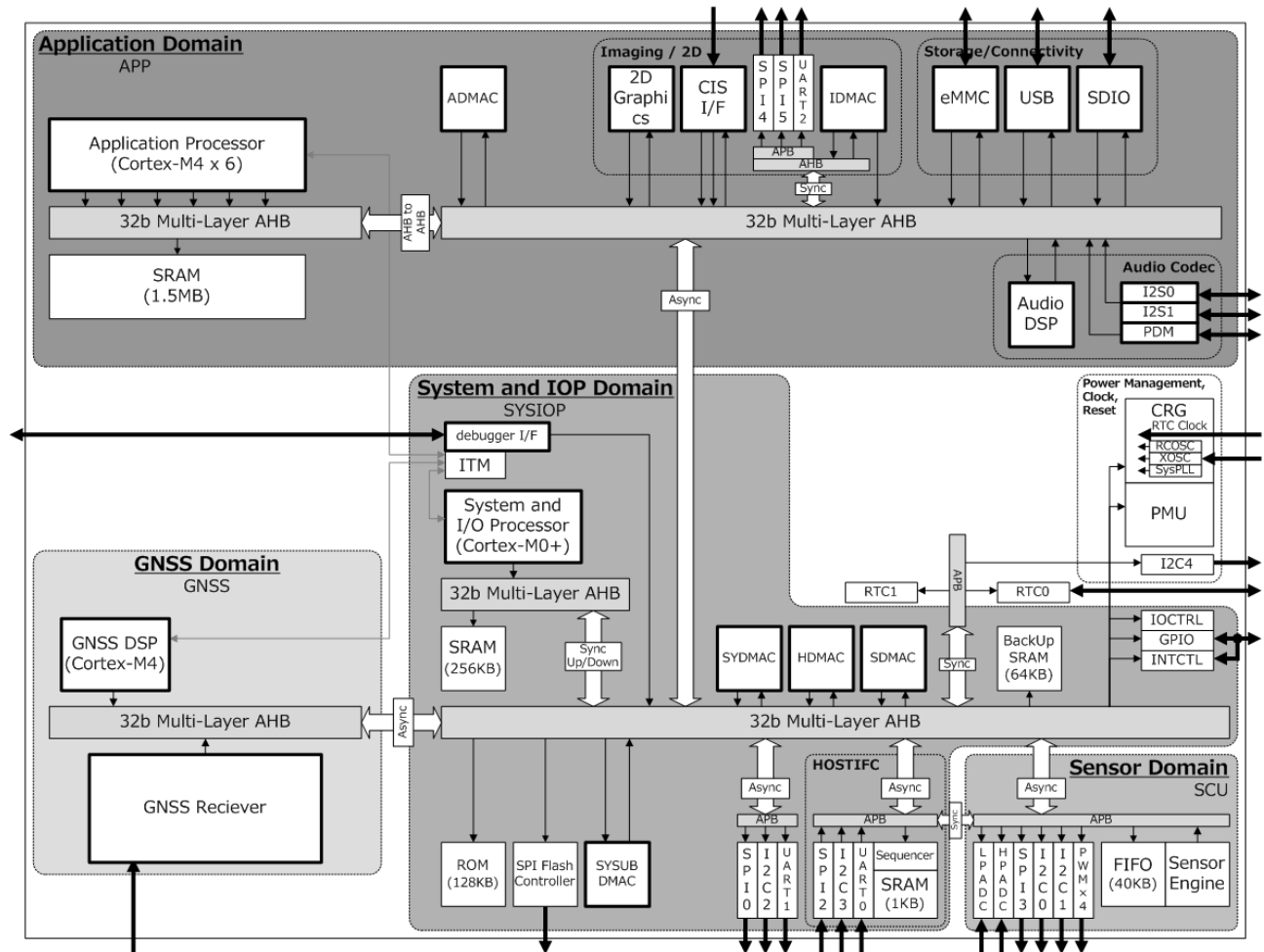


Figure Block Diagram-1 CXD5602 Block Diagram

2.4 Architecture Overview

The CXD5602 has one Arm® Cortex®-M0 and seven Arm® Cortex®-M4 (includes FPU) inside. Each CPU is connected each other through multi-layer AHB matrixes and bus bridges separately. Arm® Cortex®-M0 is inside the SYSIOP. One Arm® Cortex®-M4 is prepared for the GNSS only, and the remainder six Arm® Cortex®-M4 for the APP.

The CXD5602 has a bus architecture using the Bus Matrix so that eight CPUs and the other bus masters can independently access to each slave, not affected by any bus traffic.

By Round-robin arbitration inside the Bus Matrix, bus master need not to wait for a long time to access to slave even if access competition occurs.

As Figure Block Diagram-1 shows, each bus in the APP/SYSIOP/GNSS is independent.

In addition, between the SYSIOP and the GNSS, and between the SYSIOP and the APP, each peripheral is connected to the bus bridge.

2.5 CPU Processor

2.5.1 Application Processor

The application processor integrates six Cortex®-M4 processors with FPU to meet the requirements of wearable devices, which demand operation in low power and performance-optimized consumer applications with the ability to scale in speed up to 156.0 MHz, the Arm® Cortex®-M4 processor with FPU.

The key features include:

- Arm® Cortex®-M4 processor
 - ISA Support: Thumb/Thumb-2 technology
 - DSP Extension: Single cycle 16/32 bit MAC, Single cycle dual 16 bit MAC, 8/16 bit SIMD arithmetic, Hardware Divide (2-12 Cycles)
 - Floating Point Unit: Single precision floating point unit, IEEE 754 compliant
- Processor system peripherals
 - Programmable Interrupts Controller
 - 128 channel peripheral Interrupt support for each processor
 - Timers
 - AMBA® Design Kit (ADK) SP804
 - Two-channel supported
 - One Timer module for each processor (Total: Six Timers)
 - Watchdog Timer
 - AMBA® Design Kit (ADK) SP805
 - One channel for each processor (Total: Six Watchdog Timers)

2.5.2 System and I/O Processor

The I/O processor integrates Cortex®-M0+ to meet the requirements of wearable devices, which demand operation in low power and performance-optimized consumer applications with the ability to scale in speed from 32 MHz to 100 MHz, the Arm® Cortex®-M0 Processor.

The key features are:

- Arm® Cortex®-M0+ processor
 - ISA Support: Thumb Thumb-2 subset
- System and I/O Processor Memory
 - ROM: 128 KByte
 - SRAM: 256 KByte
- Boot Modes
 - At startup, the BOOT_MODE pin is used to select one of Two boot options
 - Boot from Quad SPI flash

Boot from embedded ROM

- It is used to download the program to either SPI-Flash memory or eMMC via one of the available interfaces (USB device, Configurable I/O<UART>, or the Host Interface<SPI, UART, and I2C>).
- Processor system peripherals
 - Inter-processor communication unit
 - communication FIFO (Tx, Rx) support
 - 16 binary semaphores support
 - Programmable Interrupts Controller
 - One channel software Generated Interrupt for each processor
 - 128 channel shared peripheral Interrupts for the application processors
 - Timers
 - AMBA® Design Kit (ADK) SP804
 - Two channel supported
 - Watchdog Timer
 - AMBA® Design Kit (ADK) SP805
 - One channel supported for each application processor

2.6 Memory Mapping

Overview of Memory Map Configuration

Memory map is made up of three types of views. The “SYS View” can be referred from System and I/O Processor, the “GNSS View” can be referred from the GNSS DSP, and the “APP View” can be referred from Application Processor. The SYS Window, the GNSS Window, and the APP Window are defined so that each of them can be accessed to the same address from its own processor.

The SYS Window defines addresses of the master device and the slave device inside the SYSIOP and the SCU. The GNSS Window defines addresses of the master device and the slave device inside the GNSS, the APP Window, inside the APP, as well.

Figure Memory Mapping-2 shows memory map configuration.

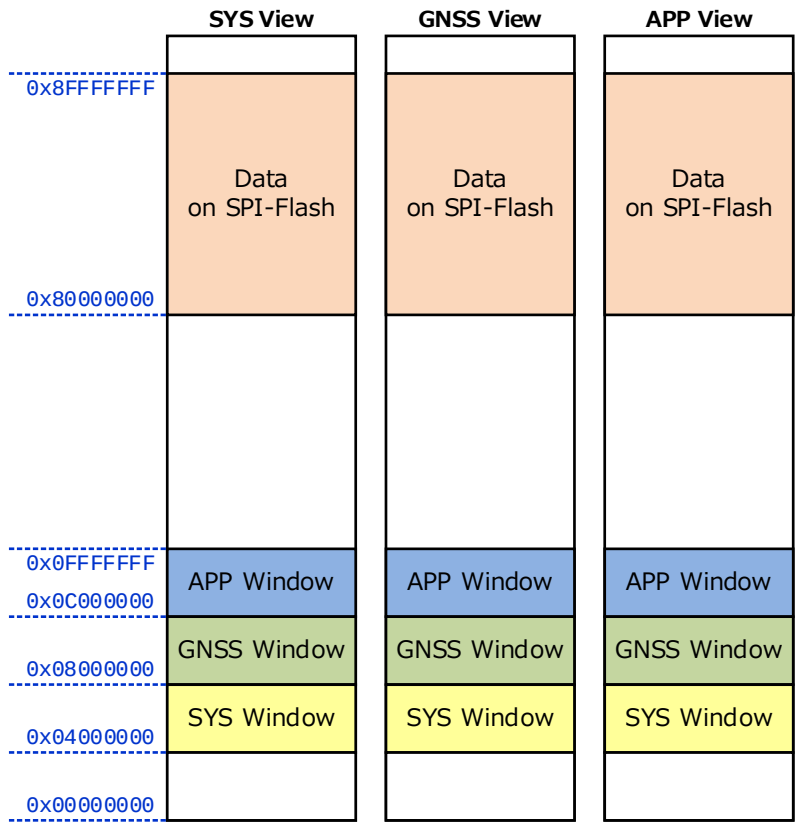


Figure Memory Mapping-2 Memory Map of the SYSIOP, GNSS, and APP

2.6.1 Memory Map of Each Block

For detailed address information of the SYSIOP block, the GNSS block, and each functional block, refer to the content of each functional block.

Table Memory Mapping-2 Memory Mapping of the SYSIOP Block (SYS Window)

Category	Pheripheral Name	Start Address	End Address	Size (4k bytes unit)
ROM	ROM(128KB)	0x04000000	0x0401FFFF	128K
Reserved	Reserved	0x04020000	0x040FFFFF	896K
Top Peripheral	PMU, CRG, GPIO, I/O Config	0x04100000	0x04105FFF	24K
	I2C4	0x04106000	0x04106FFF	4K
	FREQDISC	0x04107000	0x04107FFF	4K
	RTC0	0x04108000	0x04108FFF	4K
	RTC1	0x04109000	0x04109FFF	4K
Reserved	Reserved	0x0410B000	0x0410FFFF	20K
SPI Flash Controller	SPI Flash Controller(REG)	0x04110000	0x04110FFF	4K
Reserved	Reserved	0x04111000	0x0411FFFF	60K
DMAC	SDMAC	0x04120000	0x04120FFF	4K
	HDMAC	0x04121000	0x04121FFF	4K
	SYDMAC	0x04122000	0x04122FFF	4K
	SYSUBDMAC	0x04123000	0x04123FFF	4K
Reserved	Reserved	0x04124000	0x0417FFFF	368K
SCU	FIFO Control	0x04180000	0x04182FFF	12K
	FIFO(40K)	0x04183000	0x0418CFFF	40K
	SPI3	0x0418D000	0x0418D3FF	1K
	I2C0	0x0418D400	0x0418D7FF	1K
	I2C1	0x0418D800	0x0418DBFF	1K
	HPADC, LPADC	0x0418DC00	0x0418DFFF	1K
	Reserved	0x0418E000	0x0418FFFF	8K
	Sensor Engine	0x04190000	0x04194FFF	20K
	SCU Register	0x04195000	0x04195FFF	4K
	Reserved	0x04196000	0x0419FFFF	40K
HOSTIFC	SPI2	0x041A0000	0x041A03FF	1K
	I2C3	0x041A0400	0x041A07FF	1K
	SRAM(1KB)	0x041A0800	0x041A0BFF	1K
	Reserved	0x041A0C00	0x041A0FFF	1K
	SEQ	0x041A1000	0x041A3FFF	12K
	Reserved	0x041A4000	0x041A8FFF	20K
	UART0	0x041A9000	0x041A9FFF	4K
CONFIGIO	I2C2	0x041AA000	0x041AAFFF	4K
	SPI0	0x041AB000	0x041ABFFF	4K
	UART1	0x041AC000	0x041ACFFF	4K
Reserved	Reserved	0x041AD000	0x043FFFFFFF	2.3M
Backup SRAM	SRAM(64KB)	0x04400000	0x0440FFFF	64K
Reserved	Reserved	0x04410000	0x04FFFFFFF	11.9M
SYSCPU Local	System and I/O Processor	0x05000000	0x07FFFFFFF	48M

Table Memory Mapping-3 Memory Mapping of the APP Block (APP Window)

Category	Peripheral Name	Start Address	End Address	Size (4k bytes unit)
Reserved	Reserved	0x0C000000	0x0CFFFFFF	16M
SRAM	SRAM(1.5MB)	0x0D000000	0x0D17FFFF	1.5M
Reserved	Reserved	0x0D180000	0x0DFFFFFF	14M
APP Local	CRG and Application Processor	0x0E000000	0x0E013FFF	80M
Reserved	Reserved	0x0E014000	0x0E01FFFF	48K
DMA	ADMAC	0x0E020000	0x0E020FFF	4K
Reserved	Reserved	0x0E021000	0x0E0FFFFF	892K
Imaging/2D	CIS I/F	0x0E100000	0x0E100FFF	4K
	2D Graphics	0x0E101000	0x0E101FFF	4K
	IDMAC	0x0E102000	0x0E102FFF	4K
	UART2	0x0E103000	0x0E1033FF	1K
	SPI4	0x0E103400	0x0E103BFF	1K
	SPI5	0x0E103C00	0x0E104FFF	5K
Reserved	Reserved	0x0E105000	0x0E1FFFFF	1004K
Storage/Connectivity	USB	0x0E200000	0x0E200FFF	4K
	eMMC	0x0E201000	0x0E201FFF	4K
	SDIO	0x0E202000	0x0E202FFF	4K
Reserved	Reserved	0x0E203000	0x0E2FFFFF	1012K
Audio Codec	AUDIO DSP, I2S, PDM	0x0E300000	0x0E304FFF	20K
Reserved	Reserved	0x0E305000	0x0E3FFFFFFF	28M

2.6.2 Main Memory

There is 1.5 MByte SRAM in total which is connected to AHB of the Application Processor.

The SRAM is made up of 128 KByte Logic Tiles. Each of them has the AHB I/F individually.

In addition, the Logic Tile is the unit for the SRAM access protection function.

You can use protection feature that keeps masters with specific Master ID from accessing specific SRAM Logic Tiles. The protection feature can be controlled via buses.

Power domain of Main Memory is PWD_APP. When PWD_APP is turned off, this memory cannot be used.

Power on/off can be controlled suitably by power switch inside SRAM for each 128 KByte Logic Tile. There are two operation modes for SRAM power-off; they can be set by system control registers.

- Retention mode
 - A mode in which only the power supply of SRAM memory array is ON, and the power supply of the peripheral circuitry is turned OFF. In Retention mode, the SRAM cannot be accessed, but the data within the SRAM is retained. By turning on (ON mode) the power supply of peripheral circuitry of the SRAM once again, the data within the SRAM can be accessed. Retention mode enables reduction of the leakage power and recovery of high speed of peripheral circuitry for SRAMs that are temporarily not used.
- Shutdown mode
 - A mode that turns OFF both the power supply of the SRAM memory array and peripheral circuitry. This mode consumes less power than the Retention mode, but the data in the SRAM is not retained.

2.6.3 System Memory

There is 256 KByte SRAM in total which is connected to the AHB of the System and I/O Processor.

The SRAM block is made up of four 64K Byte Logic Tiles. One tile of the four is divided into four sub Logic Tiles of: 8 KByte, 8 KByte, 16 KByte, and 32 KByte.

Each Logic Tile has the AHB I/F individually. The application program can access data from each Logic Tile via local AHB. In addition, the Logic Tile is the unit for the SRAM access protection function. You can use protection feature that keeps masters with specific Master ID from accessing specific SRAM Logic Tiles. The protection feature can be controlled via buses. You can assign only Arm® Cortex®-M0+ of SYSCPU as master that can control the protection feature. Shortly after the POR, all masters can access all Logic Tiles.

Power domain is PWD_CORE. When PWD_CORE is turned OFF, this memory cannot be used. Each sub area tile is allocated to serial addresses; therefore, each sub Logic Tile can be turned ON/OFF individually. There are two operation modes for the SRAM power-off: Retention mode and Shutdown mode. They can be set by system control registers.

2.6.4 Backup Memory

There is 64 KByte SRAM in total which is connected to the AHB in System and IOP Domain for backup.

You can use protection feature that keeps masters with specific Master ID from accessing specific SRAM Logic Tiles. The protection feature can be controlled via buses.

Power domain belongs to PWD_PMU area. You can use protection feature that keeps masters with specific Master ID from accessing specific SRAM Logic Tiles. The protection feature can be controlled via buses. Power ON/OFF can be controlled by registers. There are two operation modes for the SRAM power-off: Retention mode and Shutdown mode. They can be set by system control registers.

2.7 Clock and Reset

2.7.1 Overview

The clock architecture inside the CXD5602 enables circuit blocks to select a variety of clock sources. It can support wide range of application with optimized power consumption, from low speed sensing operation with low power consumption, to high speed application processing using multi-core processor.

The CXD5602 has five types of usable clock sources and is made up of main five clock domains in accordance

with functional blocks. A variety of processors can dynamically select multiple usable clock source, and use most suitable clock frequency optimized for the operating conditions by using divider circuit architecture.

The functions of clock and reset of the CXD5602 are described below.

- **Clock Source**

The CXD5602 has following clocks.

- **RTC Clock:**
 - is 32.768 kHz real time clock input from outside chip
 - is assumed to be input as the RTC clock from external the RTC oscillator or the PMIC containing the RTC oscillator
 - can be used as clock for the RTC counter circuit incorporated in the chip, as system clock in operation with low power, and as clock of sensing circuit in operation with low power such as the SCU, as well.
- **RCOSC (RC Oscillator) Clock:**
 - is 8.192 MHz incorporated ring oscillator
 - becomes 8.192 MHz by being calibrated with RTC clock
 - incorporates POR system
- **XOSC (X'tal Oscillator) Clock:**
 - X'tal 26MHz
 - can be used as CPU operation clock, in addition, can be supplied to SYSPLL and RFPLL as reference clock
- **SYSPLL Clock:**
 - incorporates low power PLL which realizes high CPU operation frequency without any input of high speed clock from outside.
 - Following frequencies can be selected as SYSPLL clock according to the combination of suitable X'tal frequency variation and the division ratio of the PLL.
 - Under high speed oscillation setting: 195.000 MHz
 - Under usual speed oscillation setting: 156.000 MHz
- **RFPLL Clock (Clock generated in PWD_GNSS):**
 - is provided from the PLL (RFPLL) included in the PWD_GNSS for the RF block
 - Following frequencies can be selected as RFPLL clock according to the suitable X'tal frequency variation.
 - GPS/Beidou mode: 196.416 MHz

- **Reset Source**

The following reset functions are prepared for whole chip reset.

- Power On reset (POR) issued from the external PMIC
 - The POR issued from the POR circuit incorporated in the RCOSC
 - The above POR can be enabled or disabled with external input.
-

- System reset from Watchdog Timer (WDT)
 - It is a whole chip reset controlled by the WDT of the SYSCPU.
 - You can enable/disable whole chip reset controlled by the WDT with register setting.

2.7.2 Clock Architecture

The figure below shows CX5602 clock diagram. The CXD5602 has main five clock domains according to functional blocks. Clock can be selected in accordance with the operating conditions of each functional block.

- Always On
 - The RTC clock and the RCOSC clock can be selected.
- Application Domain
 - The Application Processor can change the frequency dynamically with the frequency divider.
- System and IOP Domain
 - Four clock sources: the SYSPLL, the XOSC, the RCOSC, and the RTC can be selected, and can be switched dynamically in accordance with the use case.
 - The System and I/O Processor can change the frequency dynamically with the frequency divider.
- Sensor Domain
 - Three clock sources: the RTC, XOSC, and RCOSC can be selected.
- GNSS Domain
 - The clock selected by the System and I/O Processor in the System and IOP Domain is distributed to the GNSS DSP. Frequency division ratio can be set independently.
 - The clock generated by either the SYSPLL or the RFPLL is distributed to the baseband signal processing block. Operational constraints depend on which PLL is selected. For details, refer to Chapter of the GNSS.

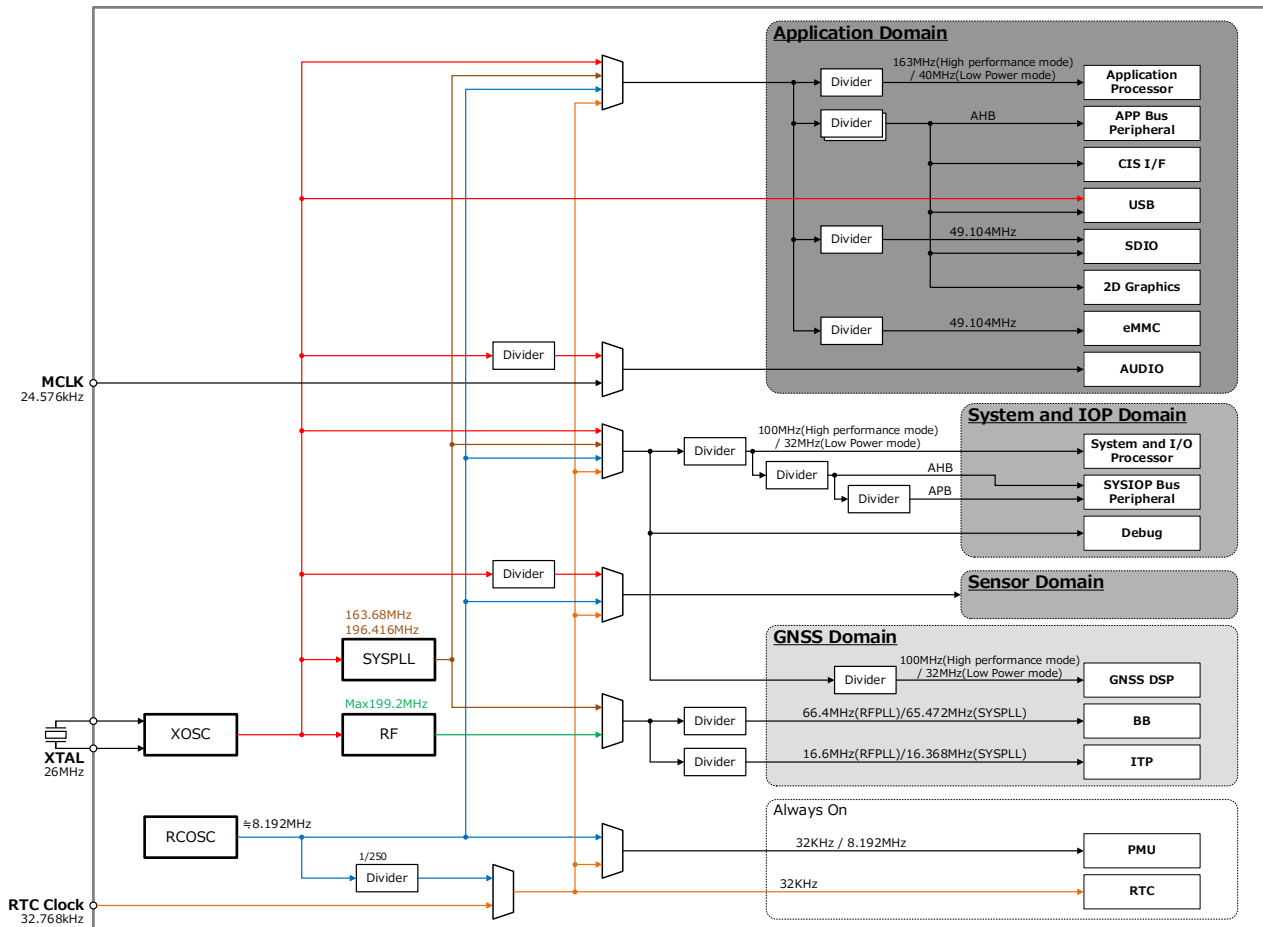


Figure Clock and Reset-3 Clock Diagram

2.8 Power Management

2.8.1 Overview

The CXD5602 has a large power domain, which is divided into 11 domains. It performs ON control of necessary functions only, while performing OFF control of the unnecessary ones, thereby reducing the power consumption. Additionally, the SRAM or analog circuits such as the ADC within the power supply domains enable individual power supply control.

Power supply control is implemented by setting on the Power Management Unit (referred as “PMU” hereinafter). You can check with the PMU about the present power state.

2.8.2 Power Domain

The 11 power domains comprise a layer structure as shown in Figure Power Management-4. The lower-layer power domains cannot be turned ON when the upper-layer power domains are OFF. Furthermore, PWD_GNSS can be turned ON only when both PWD_GNSS_ITP and PWD_SYSIOP are ON.

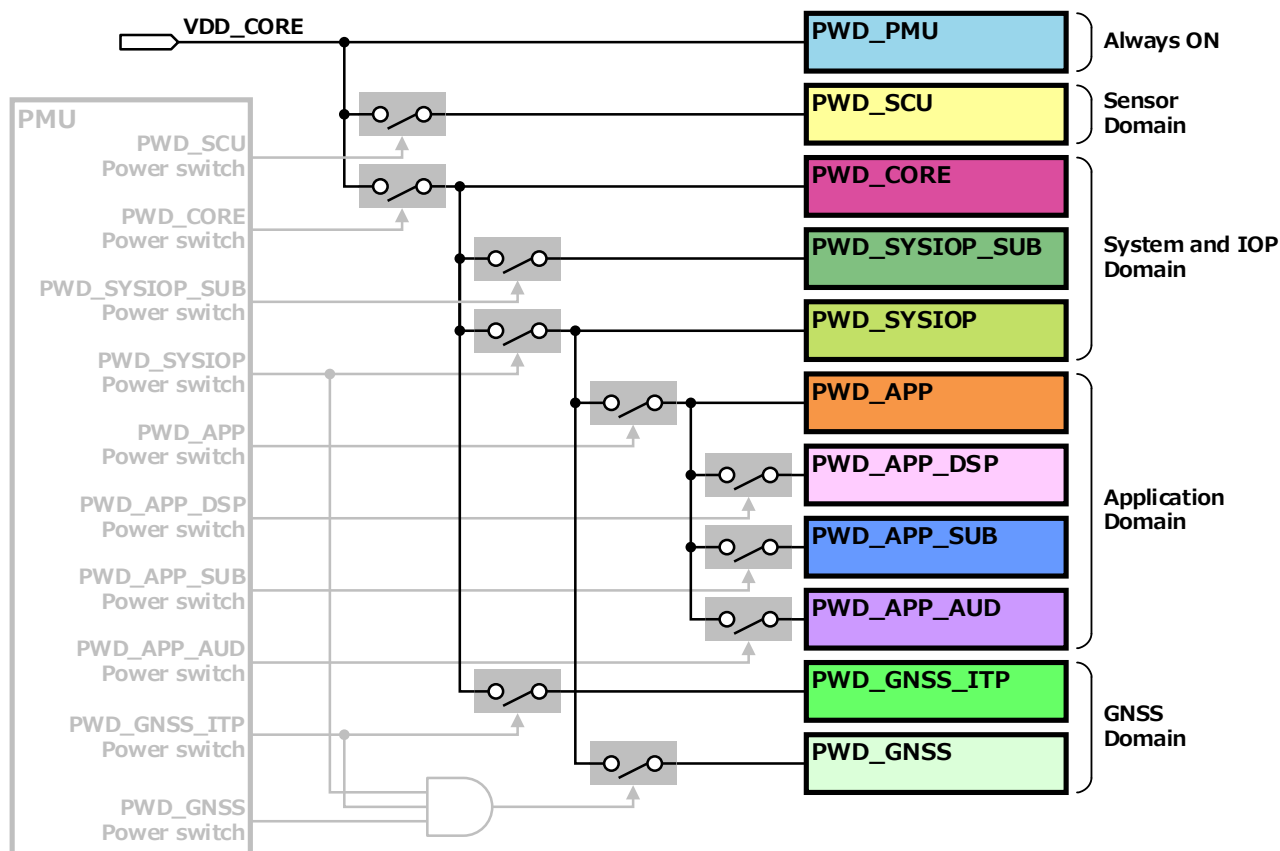


Figure Power Management-4 Power Domain Layers

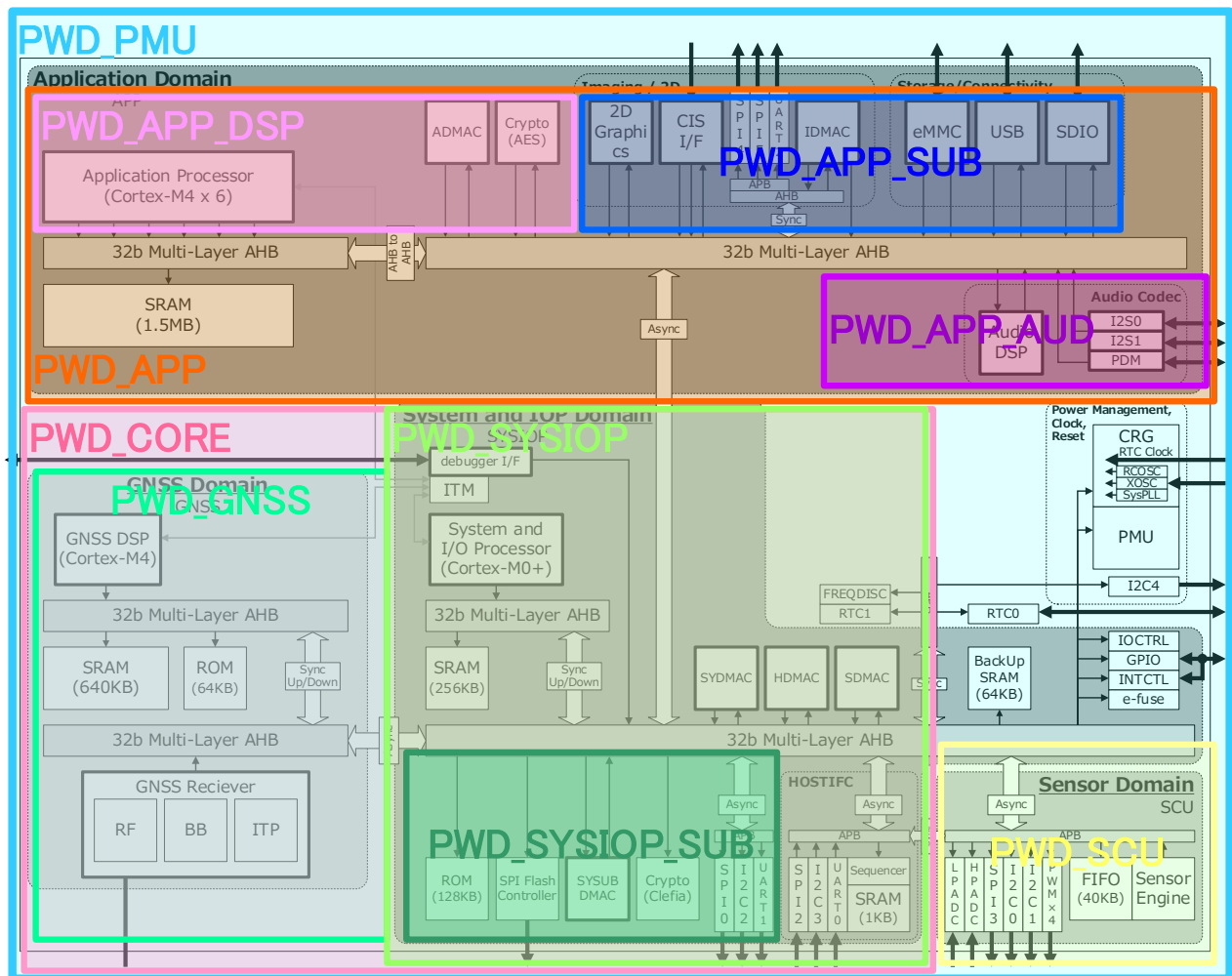


Figure Power Management-5 CXD5602 Power Domain

The following describes the functions of each power domain.

Application Domain

- PWD_APP
 - All components of Application Domain
 - Including 1.5 MByte SRAM in Application memory and Application Multi-layer Bus
- PWD_APP_DSP
 - Application processors
 - DSP block
 - ADMAC
- PWD_APP_SUB
 - Connectivity, Storage I/F and Camera, Display Interface in Application Domain
- PWD_APP_AUD

- Audio Codec

System and IOP Domain

- PWD_SYSIOP
 - System and IOP Domain
 - Excluding 256 KByte SRAM in System and I/O Processor Memory
- PWD_SYSIOP_SUB
 - Configurable I/O (I2C, SPI, UART) Interface
 - SPI-FLASH Interface
 - 128 KByte ROM in System and I/O Processor Memory
 - Crypto Engine in System and IOP Domain
 - SYSUB-DMAC
- PWD_CORE
 - All components of System and IOP Domain and GNSS Domain
 - Including 256 KByte SRAM in System and I/O Processor Memory
 - Including 640 KByte SRAM in GNSS Memory
 - Including ALIVE I/O (I2C, GPIO)
 - Including GNSS-RF
 - Including Key generation in System and IOP Domain
 - ALIVE I2C

GNSS Domain

- PWD_GNSS
 - Components of GNSS Domain
 - Excluding RF and 640 KByte SRAM in GNSS Memory
- PWD_GNSS_ITP
 - ITP Block in GNSS Domain

Sensor Domain

- PWD_SCU
 - Components of sensor engine
 - Including LP-ADC, HP-ADC

Always ON

- PWD_PMU
 - All components of VDD supplied logic, SRAM, ROM and analog
 - Including Clock, reset and Power Management Domain and BackUp SRAM
 - Including XOSC, SYSPLL
 - ALIVE GPIO

2.8.3 Power Supply States

The following describes the main power supply states.

Table Power Management-4 Power Supply States

	Power supply state	Description
1	Power Off	Both the CXD5602 (referred to as “the LSI” hereinafter) and the CXD5247 are OFF.
2	Deep Sleep	The LSI is OFF and the CXD5247 is ON. In this state, the RTC of the CXD5247 is counting, and time information can be obtained from the CXD5247 after the LSI is started.
3	Reset	In this state, the LSI and the CXD5247 are both ON, and the LSI is being reset.
4	Normal	The LSI and the CXD5247 are both ON, and the System Control (PWD_SYSIOP) turns ON, enabling power supply control of each Domain.

The state begins from “Power OFF,” and after the CXD5247 starts, power is supplied to the LSI and a reset is enabled, changing the state to “Reset.” After releasing the reset of the LSI, the System Control of the System and IOP Domain is automatically started, and the state enters to “Normal.” In the “Normal” state, the power supply control of each feature’s Domain can be controlled.

By issuing the Deep Sleep command to the CXD5247, the state changes to “Deep Sleep”. When events of the CXD5247 occur, such as the timer or interrupts, the state changes to “Reset” and then to “Normal.”

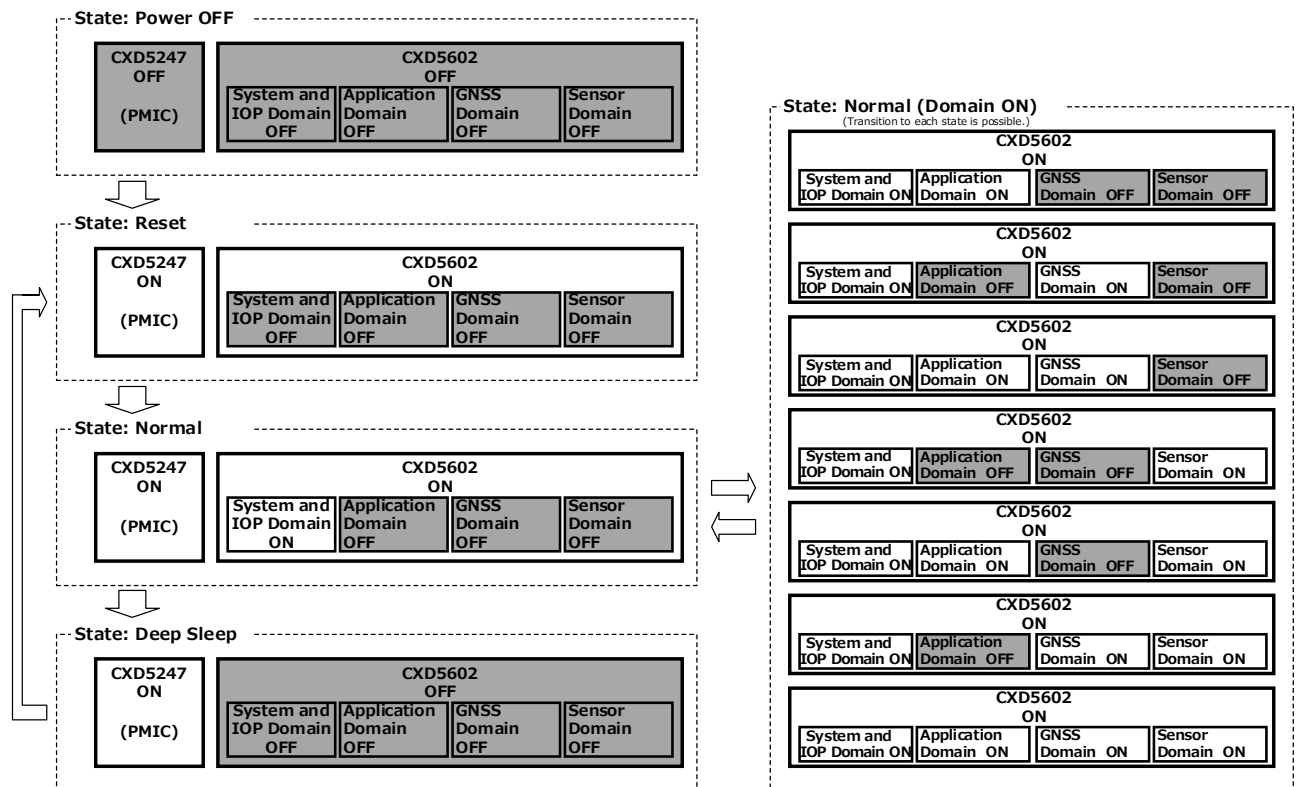


Figure Power Management-6 Changes of Power Supply States

3 Function Details

3.1 I/O Configuration

3.1.1 Outline

I/O Configuration switches between HOST I/F select function and Serial Wire Debug (SWD) function, and controls Pin Multiplexer.

3.1.2 Function List

Table I/O Configuration-5 shows I/O Configuration function list.

Table I/O Configuration-5 Function List

No	Function Name	Description
1	Switching between HOST I/F select function and SWD function	This function decides communication tools. After it decides a HOST I/F, it switches SYSTEM0/1 pin to use as SWD.
2	Pin Multiplexer	To a pin, Pin Multiplexer can assign a role selecting from up to four options. Multiple roles cannot be played at a time.

3.1.3 Switching between HOST I/F Select Function and SWD

Function

Once clock is provided to this block after Power-on Reset (POR) release, values of pin SYSTEM0 and pin SYSTEM1 are held inside. A HOST I/F is selected from I2C, SPI, or UART in accordance with the held values. Then, pin SYSTEM0 and pin SYSTEM1 are switched to SWD function.

Figure I/O Configuration-7 shows switching between HOST I/F Select function and SWD function.

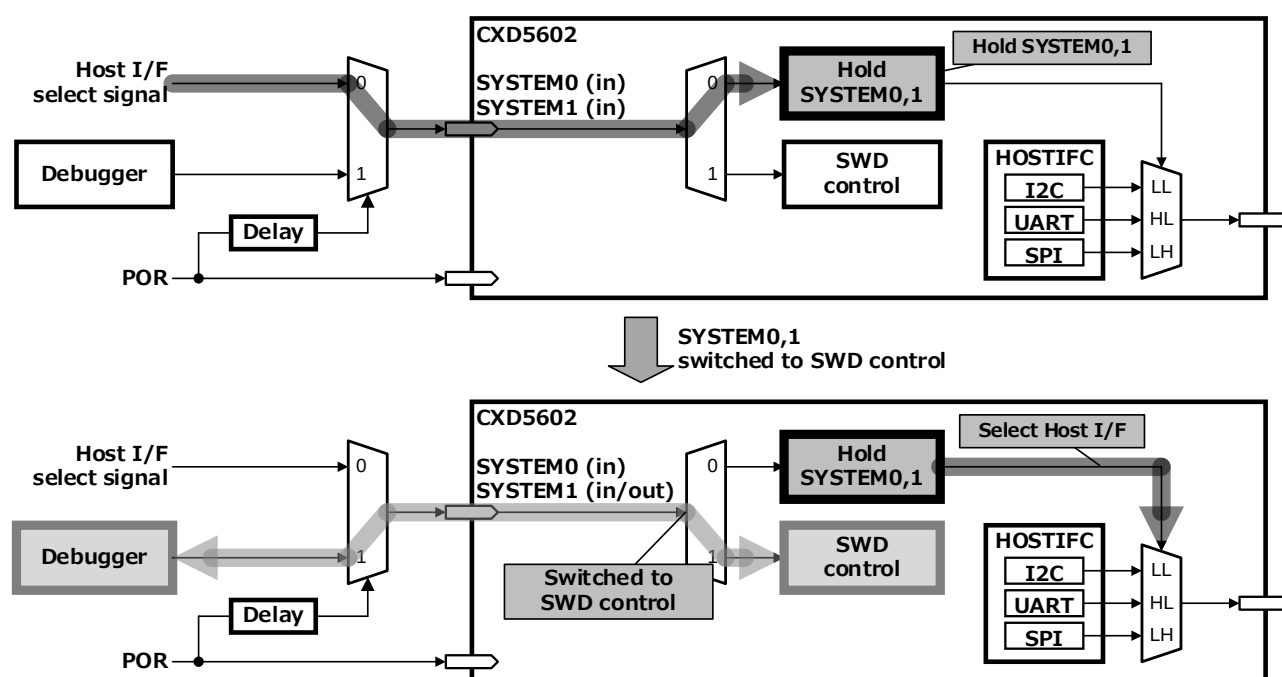


Figure I/O Configuration-7 Switching between HOST I/F Function and SWD Function

Table I/O Configuration-6 shows HOST I/F decided in accordance with the held values of pin SYSTEM0 and pin SYSTEM1 after POR release.

Table I/O Configuration-6 HOST I/F Decided in Accordance with Pin SYSTEM{0,1}

Pin name	SYSTEM0=L SYSTEM1=L	SYSTEM0=H SYSTEM1=L	SYSTEM0=L SYSTEM1=H	SYSTEM0=H SYSTEM1=H
P00_00	I2C3_BCK	UART0_TXD	SPI2_CSX	-
P00_01	I2C3_BDT	UART0_RXD	SPI2_SCK	-
P01_00	-	-	SPI2_MOSI	-
P01_01	-	-	SPI2_MISO	-

3.1.4 Pin Multiplexer

To each pin of this LSI, Pin Multiplexer can assign a role selecting from up to four options. Multiple roles cannot be played at a time. Not only General Purpose Input/Output (GPIO) mode controlled by register, but also Inter-Integrated Circuit (I2C), Serial Peripheral Interface (SPI), Universal Asynchronous Receiver Transmitter (UART), Pulse Width Modulation (PWM), Secure Digital Input/Output (SDIO), Embedded Multi Media Card (EMMC), or AUDIO can be selected.

3.1.4.1 List of Registers

Table I/O Configuration-7 shows list of registers for controlling Pin Multiplexer. Table I/O Configuration-8 shows list of registers that control Input/Output and Pull up/down of IOCELL. And Table I/O Configuration-9 shows list of registers for AUDIO Output Enable Control, and for input value setting on IP (SDIO) when SDIO function is not used.

Table I/O Configuration-7 List of Registers for Controlling Pin Multiplexer

Address	Register Name	Attribute	Function	Initial Value
0x041007C0	IOCSYS_IOMD0	RW	selects pin function (System)	0x00000000
0x041007C4	IOCSYS_IOMD1	RW	selects pin function (System)	0x00000000
0x041014A0	IOCAPP_IOMD	RW	selects pin function (Application)	0x00000000

Table I/O Configuration-8 List of Registers for Controlling IOCELL

Address	Register Name	Attribute	Function	Initial Value
0x04100800	IO_RTC_CLK_IN	RW	IOCELL setting for pin RTC_CLK_IN	0x00010100
0x04100804	IO_I2C4_BCK	RW	IOCELL setting for pin P10_00	0x01010100
0x04100808	IO_I2C4_BDT	RW	IOCELL setting for pin P10_01	0x01010100
0x0410080C	IO_PMIC_INT	RW	IOCELL setting for pin P11_00	0x01010100
0x04100810	IO_RTC_IRQ_OUT	RW	IOCELL setting for pin P12_00	0x01010100
0x04100814	IO_AP_CLK	RW	IOCELL setting for pin P13_00	0x01010100
0x04100818	IO_GNSS_1PPS_OUT	RW	IOCELL setting for pin P14_00	0x01010100
0x0410081C 0x04100840	Reserved	RO	Reserved	0x00000000

0x04100844	IO_SPI0_CS_X	RW	IOCELL setting for pin P16_00	0x01010100
0x04100848	IO_SPI0_SCK	RW	IOCELL setting for pin P16_01	0x01010100
0x0410084C	IO_SPI0_MOSI	RW	IOCELL setting for pin P17_00	0x01010100
0x04100850	IO_SPI0_MISO	RW	IOCELL setting for pin P17_01	0x01010100
0x04100854	IO_SPI1_CS_X	RW	IOCELL setting for pin P18_00	0x00010100
0x04100858	IO_SPI1_SCK	RW	IOCELL setting for pin P18_01	0x00010100
0x0410085C	IO_SPI1_IO0	RW	IOCELL setting for pin P18_02	0x00010100
0x04100860	IO_SPI1_IO1	RW	IOCELL setting for pin P18_03	0x00010100
0x04100864	IO_SPI1_IO2	RW	IOCELL setting for pin P19_00	0x00010100
0x04100868	IO_SPI1_IO3	RW	IOCELL setting for pin P19_01	0x00010100
0x0410086C	IO_SPI2_CS_X	RW	IOCELL setting for pin P00_00	0x01010100
0x04100870	IO_SPI2_SCK	RW	IOCELL setting for pin P00_01	0x01010100
0x04100874	IO_SPI2_MOSI	RW	IOCELL setting for pin P01_00	0x01010100
0x04100878	IO_SPI2_MISO	RW	IOCELL setting for pin P01_01	0x01010100
0x0410088C	IO_HIF_IRQ_OUT	RW	IOCELL setting for pin P02_00	0x01010100
0x04100880	IO_HIF_GPIO0	RW	IOCELL setting for pin P03_00	0x01010100
0x04100884 0x04100890	Reserved	R0	Reserved	0x00000000
0x04100894	IO_SEN_IRQ_IN	RW	IOCELL setting for pin P1e_00	0x01010100
0x04100898	IO_SPI3_CS0_X	RW	IOCELL setting for pin P1f_00	0x01010100
0x0410089C	IO_SPI3_CS1_X	RW	IOCELL setting for pin P1g_00	0x01010100
0x041008A0	IO_SPI3_CS2_X	RW	IOCELL setting for pin P1h_00	0x01010100
0x041008A4	IO_SPI3_SCK	RW	IOCELL setting for pin P1i_00	0x01010100
0x041008A8	IO_SPI3_MOSI	RW	IOCELL setting for pin P1i_01	0x01010100
0x041008AC	IO_SPI3_MISO	RW	IOCELL setting for pin P1i_02	0x01010100
0x041008B0	IO_I2C0_BCK	RW	IOCELL setting for pin P1j_00	0x01010100
0x041008B4	IO_I2C0_BDT	RW	IOCELL setting for pin P1j_01	0x01010100
0x041008B8	IO_PWM0	RW	IOCELL setting for pin P1r_00	0x01010100
0x041008BC	IO_PWM1	RW	IOCELL setting for pin P1r_01	0x01010100
0x041008C0	IO_PWM2	RW	IOCELL setting for pin P1r_02	0x01010100
0x041008C4	IO_PWM3	RW	IOCELL setting for pin P1r_03	0x01010100
0x041008C8 0x041008D0	Reserved	RO	Reserved	0x00000000
0x041008D4	IO_DBG_SWOCLK	RW	IOCELL setting for pin SWOCLK	0x00010100
0x041008D8	IO_DBG_SWO	RW	IOCELL setting for pin SWO	0x01010100
0x041008E0	IO_IS_CLK	RW	IOCELL setting for pin P1m_00	0x01010100

0x041008E4	IO_IS_VSYNC	RW	IOCELL setting for pin P1m_01	0x01010100
0x041008E8	IO_IS_HSYNC	RW	IOCELL setting for pin P1m_02	0x01010100
0x041008EC	IO_IS_DATA0	RW	IOCELL setting for pin P1m_03	0x01010100
0x041008F0	IO_IS_DATA1	RW	IOCELL setting for pin P1m_04	0x01010100
0x041008F4	IO_IS_DATA2	RW	IOCELL setting for pin P1m_05	0x01010100
0x041008F8	IO_IS_DATA3	RW	IOCELL setting for pin P1m_06	0x01010100
0x041008FC	IO_IS_DATA4	RW	IOCELL setting for pin P1m_07	0x01010100
0x04100900	IO_IS_DATA5	RW	IOCELL setting for pin P1m_08	0x01010100
0x04100904	IO_IS_DATA6	RW	IOCELL setting for pin P1m_09	0x01010100
0x04100908	IO_IS_DATA7	RW	IOCELL setting for pin P1m_10	0x01010100
0x0410090C	IO_UART2_TXD	RW	IOCELL setting for pin P1n_00	0x01010100
0x04100910	IO_UART2_RXD	RW	IOCELL setting for pin P1n_01	0x01010100
0x04100914	IO_UART2_CTS	RW	IOCELL setting for pin P1n_02	0x01010100
0x04100918	IO_UART2_RTS	RW	IOCELL setting for pin P1n_03	0x01010100
0x0410091C	IO_SPI4_CS_X	RW	IOCELL setting for pin P1o_00	0x01010100
0x04100920	IO_SPI4_SCK	RW	IOCELL setting for pin P1o_01	0x01010100
0x04100924	IO_SPI4_MOSI	RW	IOCELL setting for pin P1o_02	0x01010100
0x04100928	IO_SPI4_MISO	RW	IOCELL setting for pin P1o_03	0x01010100
0x0410092C	IO_EMMC_CLK	RW	IOCELL setting for pin P1p_00	0x01010100
0x04100930	IO_EMMC_CMD	RW	IOCELL setting for pin P1p_01	0x01010100
0x04100934	IO_EMMC_DATA0	RW	IOCELL setting for pin P1p_02	0x01010100
0x04100938	IO_EMMC_DATA1	RW	IOCELL setting for pin P1p_03	0x01010100
0x0410093C	IO_EMMC_DATA2	RW	IOCELL setting for pin P1q_00	0x01010100
0x04100940	IO_EMMC_DATA3	RW	IOCELL setting for pin P1q_01	0x01010100
0x04100944	IO_SDIO_CLK	RW	IOCELL setting for pin P1r_00	0x01010100
0x04100948	IO_SDIO_CMD	RW	IOCELL setting for pin P1r_01	0x01010100
0x0410094C	IO_SDIO_DATA0	RW	IOCELL setting for pin P1r_02	0x01010100
0x04100950	IO_SDIO_DATA1	RW	IOCELL setting for pin P1r_03	0x01010100
0x04100954	IO_SDIO_DATA2	RW	IOCELL setting for pin P1r_04	0x01010100
0x04100958	IO_SDIO_DATA3	RW	IOCELL setting for pin P1r_05	0x01010100
0x0410095C	IO_SDIO_CD	RW	IOCELL setting for pin P1s_00	0x01010100
0x04100960	IO_SDIO_WP	RW	IOCELL setting for pin P1s_01	0x01010100
0x04100964	IO_SDIO_CMDDIR	RW	IOCELL setting for pin P1t_00	0x01010100
0x04100968	IO_SDIO_DIR0	RW	IOCELL setting for pin P1t_01	0x01010100
0x0410096C	IO_SDIO_DIR1_3	RW	IOCELL setting for pin P1t_02	0x01010100
0x04100970	IO_SDIO_CLKI	RW	IOCELL setting for pin P1u_00	0x01010100

0x04100974	IO_I2S0_BCK	RW	IOCELL setting for pin P1v_00	0x01010100
0x04100978	IO_I2S0_LRCK	RW	IOCELL setting for pin P1v_01	0x01010100
0x0410097C	IO_I2S0_DATA_IN	RW	IOCELL setting for pin P1v_02	0x01010100
0x04100980	IO_I2S0_DATA_OUT	RW	IOCELL setting for pin P1v_03	0x01010100
0x04100984	IO_I2S1_BCK	RW	IOCELL setting for pin P1w_00	0x01010100
0x04100988	IO_I2S1_LRCK	RW	IOCELL setting for pin P1w_01	0x01010100
0x0410098C	IO_I2S1_DATA_IN	RW	IOCELL setting for pin P1w_02	0x01010100
0x04100990	IO_I2S1_DATA_OUT	RW	IOCELL setting for pin P1w_03	0x01010100
0x04100994	IO_MCLK	RW	IOCELL setting for pin P1x_00	0x01010100
0x04100998	IO_PDM_CLK	RW	IOCELL setting for pin P1y_00	0x01010100
0x0410099C	IO_PDM_IN	RW	IOCELL setting for pin P1y_01	0x01010100
0x041009A0	IO_PDM_OUT	RW	IOCELL setting for pin P1y_02	0x01010100
0x041009A4	IO_USB_VBUSINT	RW	IOCELL setting for pin P1z_00	0x01010100

Table I/O Configuration-9 List of Registers for AUDIO and SDIO Control

Address	Register Name	Attribute	Function	Initial Value
0x04101470	AUDIO_IF_SEL	RW	PDM_CLK output signal selection	0x00000000
0x04101474	IOOEN_APP	RW	I2S output control	0x00000033
0x04101478	IOFIX_APP	RW	input value setting on IP (SDIO) when SDIO is not used	0x00000003

3.1.4.2 Register Descriptions

3.1.4.2.1 Registers for selecting a role of the I/O pins belonging to SYS group

Table I/O Configuration-10 shows registers for selecting a role of the I/O pins belonging to SYS group. Setting examples are explained in “3.1.4.3 Function Details”.

Table I/O Configuration-10 Overview of Registers for Selecting a Role of the I/O Pins Belonging to SYS Group

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041007C0	IOCSYS_IOMD0	Reserved	-	[31:28]	-	For pin functions selected by IOCSYS_IOMOD1,0, refer to Table I/O Configuration-11.
		HIFEXT	RW	[27:26]	0	
		HIFIRQ	RW	[25:24]	0	
		SPI2B	RW	[23:22]	0	
		SPI2A	RW	[21:20]	0	
		SPI1B	RW	[19:18]	0	
		SPI1A	RW	[17:16]	0	
		SPI0B	RW	[15:14]	0	
		SPI0A	RW	[13:12]	0	
		Reserved	-	[11:10]	-	
		GNSS_1PPS_OUT	RW	[9:8]	0	
		AP_CLK	RW	[7:6]	0	
		RTC_IRQ_OUT	RW	[5:4]	0	
		PMIC_INT	RW	[3:2]	0	
		I2C4	RW	[1:0]	0	
0x041007C4	IOCSYS_IOMD1	Reserved	-	[31:24]	-	
		PWMB	RW	[23:22]	0	
		PWMA	RW	[21:20]	0	
		I2C0	RW	[19:18]	0	
		SPI3	RW	[17:16]	0	
		SPI3_CS2_X	RW	[15:14]	0	
		SPI3_CS1_X	RW	[13:12]	0	
		SPI3_CS0_X	RW	[11:10]	0	
		SEN_IRQ_IN	RW	[9:8]	0	
		Reserved	-	[7:0]	-	

Table I/O Configuration-11 shows pin functions selected by **IOCSYS_IOMD0** and **IOSYS_IOMD1**.

Table I/O Configuration-11 Table of Role Selection for I/O Pins Belonging to SYS Group

Pin Name	Register Name	Register Setting value			
		0	1	2	3
P10_00	IOCSYS_IOMD0.I2C4	GPIO	I2C_BCK	GPIO	GPIO
P10_01		GPIO	I2C_BDT	GPIO	GPIO
P11_00	IOCSYS_IOMD0.PMIC_INT	GPIO	PMIC_INT	RTC_IRQ_OUT (Open Drain) with PMIC_INT (Open Drain)	GPIO
P12_00	IOCSYS_IOMD0.RTC_IRQ_OUT	GPIO	RTC_IRQ_OUT	RTC_IRQ_OUT (Open Drain)	GPIO
P13_00	IOCSYS_IOMD0.AP_CLK	GPIO	AP_CLK	PMU_WDT	PMU_WDT (Open Drain)
P14_00	IOCSYS_IOMD0.GNSS_1PPS_OUT	GPIO	GNSS_1PPS_O UT	CPU_WDT	CPU_WDT (Open Drain)
P16_00	IOCSYS_IOMD0.SPI0A	GPIO	UART1_TXD	SPI0_CS_X	Reserved
P16_01		GPIO	UART1_RXD	SPI0_SCK	Reserved
P17_00	IOCSYS_IOMD0.SPI0B	GPIO	I2C2_BCK	SPI0_MOSI	Reserved
P17_01		GPIO	I2C2_BDT	SPI0_MISO	Reserved
P18_00	IOCSYS_IOMD0.SPI1A	GPIO	SPI1_CS_X	SPI0_CS_X	Reserved
P18_01		GPIO	SPI1_SCK	SPI0_SCK	Reserved
P18_02		GPIO	SPI0_IO0	SPI0_MOSI	Reserved
P18_03		GPIO	SPI0_IO1	SPI0_MISO	Reserved
P19_00	IOCSYS_IOMD0.SPI1B	GPIO	SPI1_IO2	GPIO	Reserved
P19_01		GPIO	SPI1_IO3	GPIO	Reserved
P00_00	IOCSYS_IOMD0.SPI2A	GPIO	SPI2_CS_X	UART0_TXD	I2C3_BCK
P00_01		GPIO	SPI2_SCK	UART0_RXD	I2C3_BDT
P01_00	IOCSYS_IOMD0.SPI2B	GPIO	SPI2_MOSI	UART0_CTS	GPIO
P01_01		GPIO	SPI2_MISO	UART0_RTS	GPIO
P02_00	IOCSYS_IOMD0.HIFIRQ	GPIO	HIF_IRQ_OUT	HIF_IRQ_OUT (Open Drain)	GNSS_1PPS_OU T
P03_00	IOCSYS_IOMD0.HIFEXT	GPIO	GPIO	GPIO	GPS_EXTLD
P1e_00	IOCSYS_IOMD1.SEN_IRQ_IN	GPIO	SEN_IRQ_IN	Reserved	Reserved
P1f_00	IOCSYS_IOMD1.SPI3_CS0_X	GPIO	SPI3_CS0_X	Reserved	Reserved
P1g_00	IOCSYS_IOMD1.SPI3_CS1_X	GPIO	SPI3_CS1_X	Reserved	Reserved
P1h_00	IOCSYS_IOMD1.SPI3_CS2_X	GPIO	SPI3_CS2_X	Reserved	Reserved

P1i_00	IOCSYS_IOMD1.SPI3	GPIO	SPI3_SCK	Reserved	Reserved
P1i_01		GPIO	SPI3_MOSI	Reserved	Reserved
P1i_02		GPIO	SPI3_MISO	Reserved	Reserved
P1j_00	IOCSYS_IOMD1.I2C0	GPIO	I2C0_BCK	Reserved	Reserved
P1j_01		GPIO	I2C0_BDT	Reserved	Reserved
P1k_00	IOCSYS_IOMD1.PWMA	GPIO	PWM0	Reserved	Reserved
P1k_01		GPIO	PWM1	GPIO	Reserved
P1l_00	IOCSYS_IOMD1.PWMB	GPIO	PWM2	I2C1_BCK	Reserved
P1l_01		GPIO	PWM3	I2C1_BDT	Reserved

3.1.4.2.2 Register for selecting a role of the I/O pins belonging to APP group

Table I/O Configuration-12 shows registers for selecting a role of the I/O pins belonging to APP group. Setting examples are explained in “3.1.4.3 Function Details”.

Table I/O Configuration-12 Overview of Registers for Selecting a Role of the I/O Pins Belonging to APP Group

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041014A0	IOCAPP_IOMD	Reserved	-	[31:28]	-	For pin functions selected by IOCAPP_IOMD, refer to Table I/O Configuration-13.
		USBVBUS	RW	[27:26]	0	
		PDM	RW	[25:24]	0	
		MCLK	RW	[23:22]	0	
		I2S1	RW	[21:20]	0	
		I2S0	RW	[19:18]	0	
		SDIOD	RW	[17:16]	0	
		SDIOC	RW	[15:14]	0	
		SDIOB	RW	[13:12]	0	
		SDIOA	RW	[11:10]	0	
		EMMCB	RW	[9:8]	0	
		EMMCA	RW	[7:6]	1	
		SPI4	RW	[5:4]	0	
		UART2	RW	[3:2]	0	
		IS	RW	[1:0]	0	

Table I/O Configuration-13 shows pin functions selected by IOCAPP_IOMD.

Table I/O Configuration-13 Table of Role Selection for the I/O Pins Belonging to APP Group

Pin Name	Register Name	Register Setting value			
		0	1	2	3
P1m_00	IOCAPP_IOMD.IS	GPIO	IS_CLK	GPIO	GPIO
P1m_01		GPIO	IS_VSYNC	GPIO	GPIO
P1m_02		GPIO	IS_HSYNC	GPIO	GPIO
P1m_03		GPIO	IS_DATA0	GPIO	GPIO
P1m_04		GPIO	IS_DATA1	GPIO	GPIO
P1m_05		GPIO	IS_DATA2	GPIO	GPIO
P1m_06		GPIO	IS_DATA3	GPIO	GPIO
P1m_07		GPIO	IS_DATA4	GPIO	GPIO
P1m_08		GPIO	IS_DATA5	GPIO	GPIO
P1m_09		GPIO	IS_DATA6	GPIO	GPIO
P1m_10		GPIO	IS_DATA7	GPIO	GPIO
P1n_00	IOCAPP_IOMD.UART2	GPIO	UART2_TXD	Reserved	GPIO
P1n_01		GPIO	UART2_RXD	Reserved	GPIO
P1n_02		GPIO	UART2_CTS	Reserved	GPIO
P1n_03		GPIO	UART2_RTS	Reserved	GPIO
P1o_00	IOCAPP_IOMD.SPI4	GPIO	SPI4_CS_X	Reserved	GPIO
P1o_01		GPIO	SPI4_SCK	Reserved	GPIO
P1o_02		GPIO	SPI4_MOSI	Reserved	GPIO
P1o_03		GPIO	SPI4_MISO	Reserved	GPIO
P1p_00	IOCAPP_IOMD.EMMCA	GPIO	EMMC_CLK	SPI5_SCK	GPIO
P1p_01		GPIO	EMMC_CMD	SPI5_CS_X	GPIO
P1p_02		GPIO	EMMC_DATA0	SPI5_MOSI	GPIO
P1p_03		GPIO	EMMC_DATA1	SPI5_MISO	GPIO
P1q_00	IOCAPP_IOMD.EMMCB	GPIO	EMMC_DATA2	Reserved	GPIO
P1q_01		GPIO	EMMC_DATA3	Reserved	GPIO
P1r_00	IOCAPP_IOMD.SDIOA	GPIO	SDIO_CLK	SPI5_SCK	GPIO
P1r_01		GPIO	SDIO_CMD	SPI5_CS_X	GPIO
P1r_02		GPIO	SDIO_DATA0	SPI5_MOSI	GPIO
P1r_03		GPIO	SDIO_DATA1	SPI5_MISO	GPIO
P1r_04		GPIO	SDIO_DATA2	GPIO	GPIO
P1r_05		GPIO	SDIO_DATA3	GPIO	GPIO
P1s_00	IOCAPP_IOMD.SDIOB	GPIO	SDIO_CD	GPIO	GPIO
P1s_01		GPIO	SDIO_WP	GPIO	GPIO

P1t_00	IOCAPP_IOMD.SDIOC	GPIO	SDIO_CMDDIR	GPIO	GPIO
P1t_01		GPIO	SDIO_DIR0	GPIO	GPIO
P1t_02		GPIO	SDIO_DIR1_3	GPIO	GPIO
P1u_00	IOCAPP_IOMD.SDIOD	GPIO	SDIO_CLKI	GPIO	GPIO
P1v_00	IOCAPP_IOMD.I2S0	GPIO	I2S0_BCK	Reserved	GPIO
P1v_01		GPIO	I2S0_LRCK	Reserved	GPIO
P1v_02		GPIO	I2S0_DATA_IN	Reserved	GPIO
P1v_03		GPIO	I2S0_DATA_OUT	Reserved	GPIO
P1w_00	IOCAPP_IOMD.I2S1	GPIO	I2S1_BCK	Reserved	GPIO
P1w_01		GPIO	I2S1_LRCK	Reserved	GPIO
P1w_02		GPIO	I2S1_DATA_IN	Reserved	GPIO
P1w_03		GPIO	I2S1_DATA_OUT	Reserved	GPIO
P1x_00	IOCAPP_IOMD.MCLK	GPIO	MCLK	Reserved	GPIO
P1y_00	IOCAPP_IOMD.PDM	GPIO	PDM_CLK	Reserved	GPIO
P1y_01		GPIO	PDM_IN	GPIO	GPIO
P1y_02		GPIO	PDM_OUT	GPIO	GPIO
P1z_00	IOCAPP_IOMD.USBVBUS	GPIO	USB_VBUSINT	GPIO	Reserved

3.1.4.2.3 IOCELL Control Register

These registers set IOCELL of each I/O pin. Table I/O Configuration-14 shows overview of registers. Figure I/O Configuration-8 shows a visualized function inside IOCELL controlled by the parameter that is set by IOCELL control register. And Table I/O Configuration-15 Table I/O Configuration-15 Correspondence Table of IOCELL Control Registers and Controllable I/O Pins shows correspondence table of registers and I/O pins.

Table I/O Configuration-14 Overview of Registers to Select Function of IOCELL

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100800 0x041009A4	IO_* (1*)	Reserved	-	[31:25]	-	-
		LOWEMI	RW	[24]	1	Output Current Control 0: 4mA(Max64MHz), 1: 2mA(Max32MHz)
		Reserved	-	[23:17]	-	-
		PDN	RW	[16]	1	Pulldown Control 0: Pulldown, 1: Normal
		Reserved	-	[15:9]	-	-
		PUN	RW	[8]	1	Pullup Control 0: Pullup, 1: Normal
		Reserved	-	[7:1]	-	-
		ENZI	RW	[0]	0	Input Enable Control 0: Input Disable, 1: Input Enable

(1*) : For pin names corresponding to registers, refer to Table I/O Configuration-15.

The following IOCELL control registers are different from those listed above.

- **IO_DBG_SWO_CLK.ENZI** is reserved.
- **O_DBG_SWO.ENZI** is reserved.
- **IO_RTC_CLK_IN.LOWEMI** is reserved.
- The initial value of **IO_SPI1_CS_X.LOWEMI** is "0".
- The initial value of **IO_SPI1_SCK.LOWEMI** is "0".
- The initial value of **IO_SPI1_IO0.LOWEMI** is "0".
- The initial value of **IO_SPI1_IO1.LOWEMI** is "0".
- The initial value of **IO_SPI1_IO2.LOWEMI** is "0".
- The initial value of **IO_SPI1_IO3.LOWEMI** is "0".
- The initial value of **IO_DBG_SWOCLK.LOWEMI** is "0".

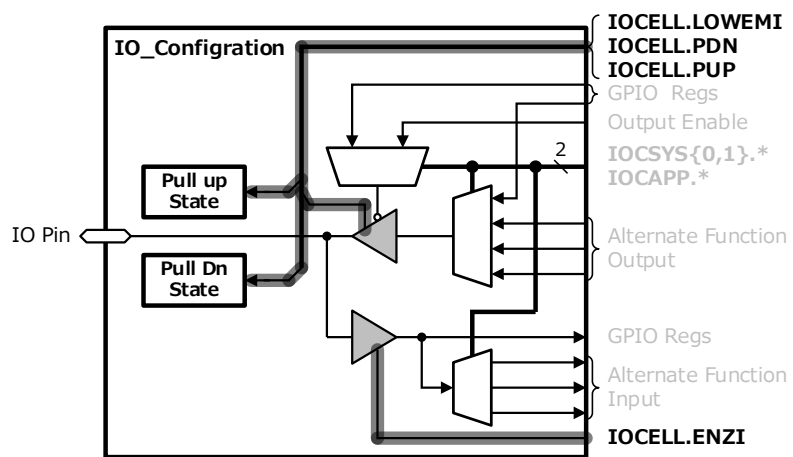


Figure I/O Configuration-8 Visualized Function inside IOCELL Controlled by IOCELL Control Register

Table I/O Configuration-15 Correspondence Table of IOCELL Control Registers and Controllable I/O Pins

Register Name	Pin Name	Register Name	Pin Name	Register Name	Pin Name
IO_I2C4_BCK	P10_00	IO_I2C0_BCK	P1j_00	IO_EMMC_DATA2	P1q_00
IO_I2C4_BDT	P10_01	IO_I2C0_BDT	P1j_01	IO_EMMC_DATA3	P1q_01
IO_PMIC_INT	P11_00	IO_PWM0	P1k_00	IO_SDIO_CLK	P1r_00
IO_RTC_IRQ_OUT	P12_00	IO_PWM1	P1k_01	IO_SDIO_CMD	P1r_01
IO_AP_CLK	P13_00	IO_PWM2	P1l_00	IO_SDIO_DATA0	P1r_02
IO_GNSS_1PPS_OUT	P14_00	IO_PWM3	P1l_01	IO_SDIO_DATA1	P1r_03
IO_SPI0_CS_X	P16_00	IO_IS_CLK	P1m_00	IO_SDIO_DATA2	P1r_04
IO_SPI0_SCK	P16_01	IO_IS_VSYNC	P1m_01	IO_SDIO_DATA3	P1r_05
IO_SPI0_MOSI	P17_00	IO_IS_HSYNC	P1m_02	IO_SDIO_CD	P1s_00
IO_SPI0_MISO	P17_01	IO_IS_DATA0	P1m_03	IO_SDIO_WP	P1s_01
IO_SPI1_CS_X	P18_00	IO_IS_DATA1	P1m_04	IO_SDIO_CMDDIR	P1t_00
IO_SPI1_SCK	P18_01	IO_IS_DATA2	P1m_05	IO_SDIO_DIR0	P1t_01
IO_SPI1_IO0	P18_02	IO_IS_DATA3	P1m_06	IO_SDIO_DIR1_3	P1t_02
IO_SPI1_IO1	P18_03	IO_IS_DATA4	P1m_07	IO_SDIO_CLKI	P1u_00
IO_SPI1_IO2	P19_00	IO_IS_DATA5	P1m_08	IO_I2S0_BCK	P1v_00
IO_SPI1_IO3	P19_01	IO_IS_DATA6	P1m_09	IO_I2S0_LRCK	P1v_01
IO_SPI2_CS_X	P00_00	IO_IS_DATA7	P1m_10	IO_I2S0_DATA_IN	P1v_02
IO_SPI2_SCK	P00_01	IO_UART2_TXD	P1n_00	IO_I2S0_DATA_OUT	P1v_03
IO_SPI2_MOSI	P01_00	IO_UART2_RXD	P1n_01	IO_I2S1_BCK	P1w_00
IO_SPI2_MISO	P01_01	IO_UART2_CTS	P1n_02	IO_I2S1_LRCK	P1w_01
IO_HIF_IRQ_OUT	P02_00	IO_UART2_RTS	P1n_03	IO_I2S1_DATA_IN	P1w_02
IO_HIF_GPIO0	P03_00	IO_SPI4_CS_X	P1o_00	IO_I2S1_DATA_OUT	P1w_03
IO_SEN_IRQ_IN	P1e_00	IO_SPI4_SCK	P1o_01	IO_MCLK	P1x_00
IO_SPI3_CS0_X	P1f_00	IO_SPI4_MOSI	P1o_02	IO_PDM_CLK	P1y_00
IO_SPI3_CS1_X	P1g_00	IO_SPI4_MISO	P1o_03	IO_PDM_IN	P1y_01
IO_SPI3_CS2_X	P1h_00	IO_EMMC_CLK	P1p_00	IO_PDM_OUT	P1y_02
IO_SPI3_SCK	P1i_00	IO_EMMC_CMD	P1p_01	IO_USB_VBUSINT	P1z_00
IO_SPI3_MOSI	P1i_01	IO_EMMC_DATA0	P1p_02	-	-
IO_SPI3_MISO	P1i_02	IO_EMMC_DATA1	P1p_03	-	-

3.1.4.2.4 I2S Output Control Register

This register performs Output Enable setting when pin P1v_{00,01} and pin P1w_{00,01} are used as I2S I/F.

I2S is operated in master mode or slave mode. When you use I2S in master mode, set it Output Enable to use P1v_{00,01} and pin P1w_{00,01} as output pin. When you use it in slave mode, set it Output Disable to use them as input pin.

Table I/O Configuration-16 Overview of Registers for Selecting Output Function of I2S

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04101474	IOOEN_APP	Reserved	-	[31:8]	-	-
		I2S1_LRCK	RW	[5]	1	0: Output Enable, 1: Output Disable
		I2S1_BCK	RW	[4]	1	0: Output Enable, 1: Output Disable
		Reserved	-	[3:2]	-	-
		I2S0_LRCK	RW	[1]	1	0: Output Enable, 1: Output Disable
		I2S0_BCK	RW	[0]	1	0: Output Enable, 1: Output Disable

3.1.4.2.5 PDM_CLK Selection Register

This register selects output signals when pin P1y_00 is used as PDM_CLK output.

Table I/O Configuration-17 Overview of Register for Selecting PDM_CLK Output Function

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04101470	AUDIO_IF_SEL	Reserved	-	[31:5]	-	-
		PDM_CLK_SEL	RW	[4]	0	selects PDM_CLK output 0: selects OFS_CLK 1: selects MCK_DMIC
		Reserved	-	[3:0]	-	-

3.1.4.2.6 SDIO Input Control Register

This register sets input values to IP (SDIO) inside the LSI when pin P1s_{00,01} is not used as SDIO function (when GPIO mode is selected). For function details, refer to “3.1.4.3.31 SDIO.”

Table I/O Configuration-18 Overview of Registers for Selecting Input Value to SDIO

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04101478	IOFIX_APP	Reserved	-	[31:2]	-	-
		SDIO_WP	RW	[1]	1	input value to SDIO_WP when SDIO function is not used
		SDIO_CD	RW	[0]	1	input value to SDIO_CD when SDIO function is not used

3.1.4.3 Function Details

To each pin, Pin Multiplexer can assign a role selecting from up to four options. Multiple roles cannot be played at a time. You can assign roles by setting IOCSYS_IMOD0, 1, IOCAPP_IMOD and IO_*.

Figure I/O Configuration-9 shows pin P1r_02 as examples of assigning roles. Pin P1r_02 can be assigned one role from three options of GPIO, SDIO_DATA0, and SPI5_MOSI.

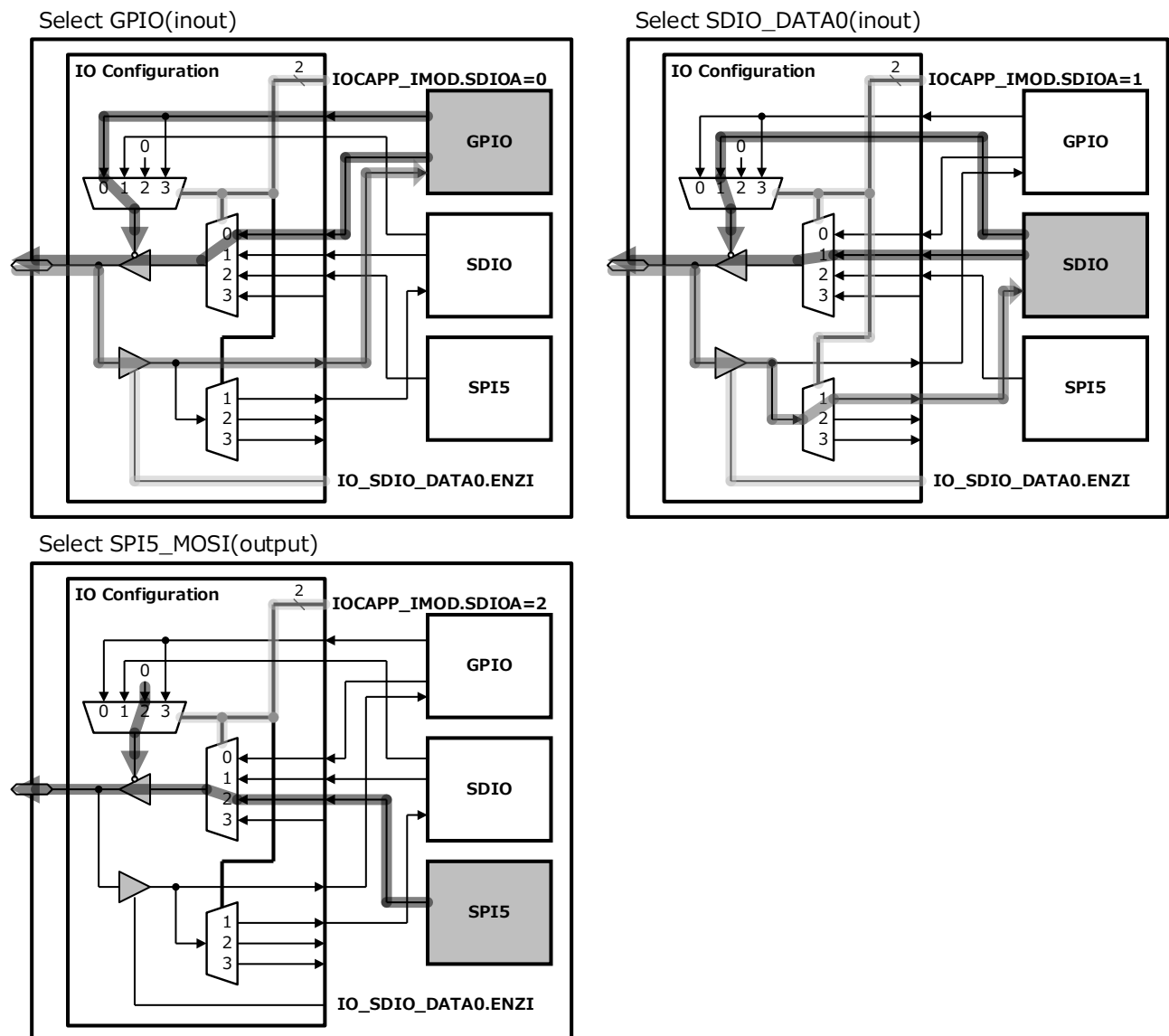


Figure I/O Configuration-9 Examples of Assigning Roles to the Pin (P1r_02)

3.1.4.3.1 I2C4

The following are settings that pin P10_{00,01} is assigned I2C (for PMIC) role.

- **IO_I2C_BCK.ENZI=1**
- **IO_I2C_BDT.ENZI=1**
- **IOCSYS_IOMD0.I2C4=1**

3.1.4.3.2 PMIC_INT

The following are settings that pin P11_00 is assigned PMIC_INT role.

- **IO_PMIC_INT.ENZI=1**
- **IOCSYS_IOMD0.PMIC_INT=1**

Note:

Before receiving PMIC_INT, by using the register of RTC{0,1}, set External Alarm Output Select Signal to External Interrupt (RTC{0,1}_RTC_CTL.SYNC_SEL=2). Figure I/O Configuration-10 shows the signal routes.

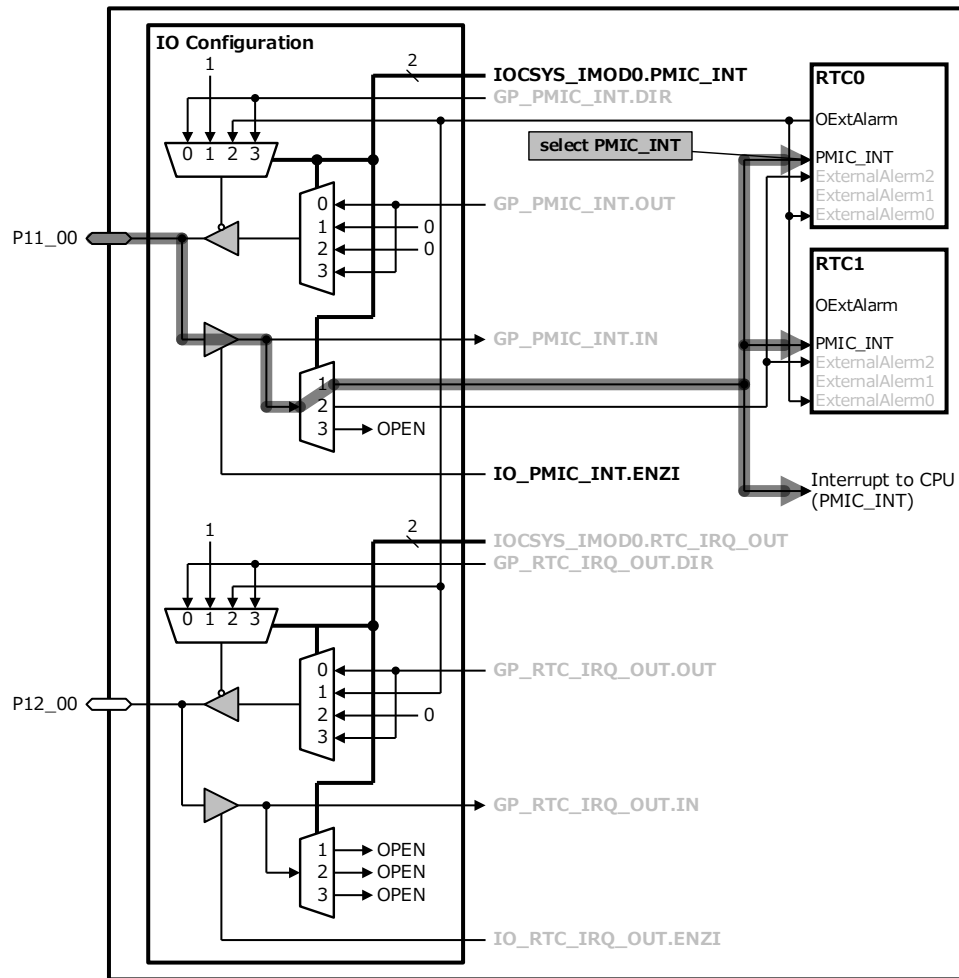


Figure I/O Configuration-10 PMIC_INT Signal Routes (MODE=1)

3.1.4.3.3 PMIC_INT with RTC_IRQ_OUT (Open Drain)

In this mode, the pin P11_00 is used bidirectionally as RTC_IRQ_OUT output role, and as PMIC_INT (for RTC synchronization) input role. By using pins of both CXD5602 and PMIC connected to CXD5602 as Open Drain, the above two roles can be compatible without any dynamic I/O control.

The following are settings that pin P11_00 is used as PMIC_INT input and RTC_IRQ_OUT output.

- IO_PMIC_INT.ENZI=1
- IOCSYS IOMD0.PMIC INT=2

Note:

Before receiving PMIC_INT, by using the register of RTC{0,1}, set External Alarm Output Select Signal to External Interrupt (**RTC{0,1}.RTC_CTL.SYNC_SEL=2**). Figure I/O Configuration-11 shows the signal routes.

Besides, when you want to use PMIC_INT as CPU interrupt, select pin P11_00 using GPIO External Interrupt selection (Section 3.2.4.3 GPIO External Interrupt) function.

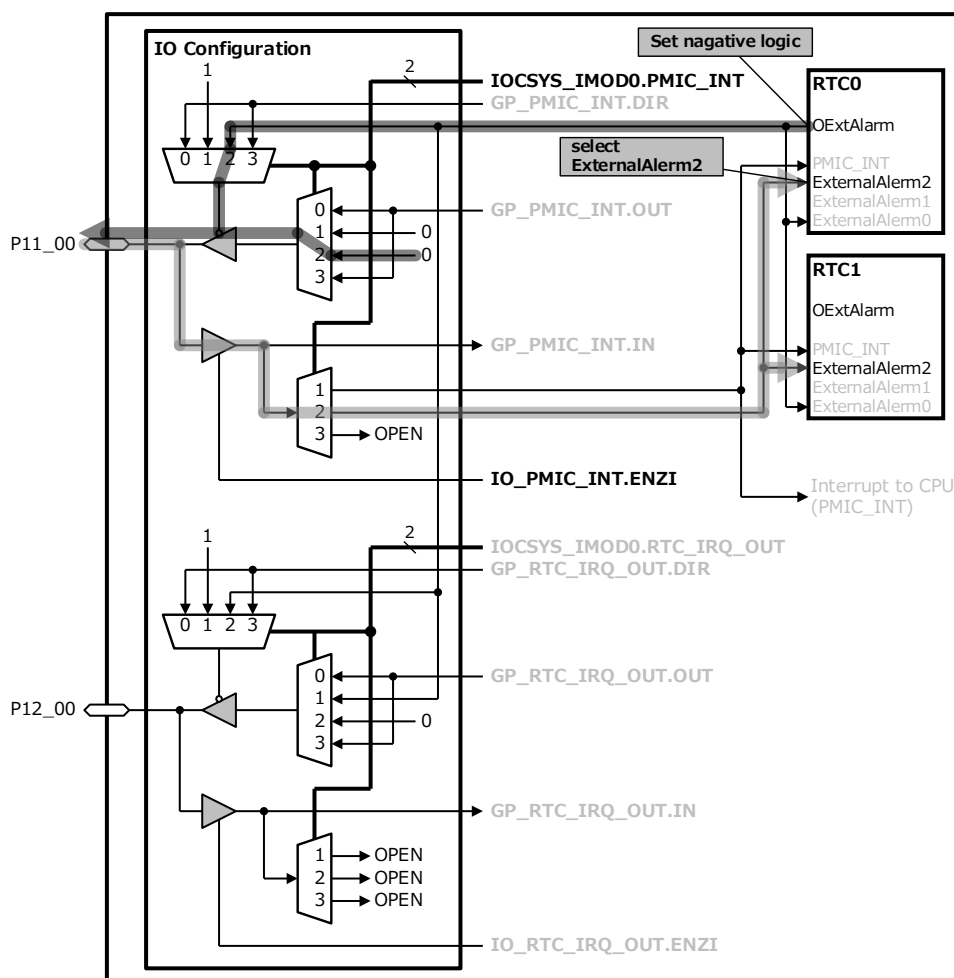


Figure I/O Configuration-11 PMIC_INT Signal Routes (MODE=2 Open Drain)

3.1.4.3.4 RTC_IRQ_OUT

The following is a setting that pin P12_00 is assigned RTC_IRQ_OUT role.

- **IOCSYS_IOMD0.RTC_IRQ_OUT=1**

3.1.4.3.5 RTC_IRQ_OUT(Open Drain)

The following is a setting that pin P12_00 is assigned RTC_IRQ_OUT role (Open Drain). The pin becomes to operate as Open Drain. By using the register of RTC0, set the External Alarm Output Select Signal to negative logic (RTC0_RTC_CTL.EXTALM_POL=1).

- **IOCSYS_IOMD0.RTC_IRQ_OUT=2**

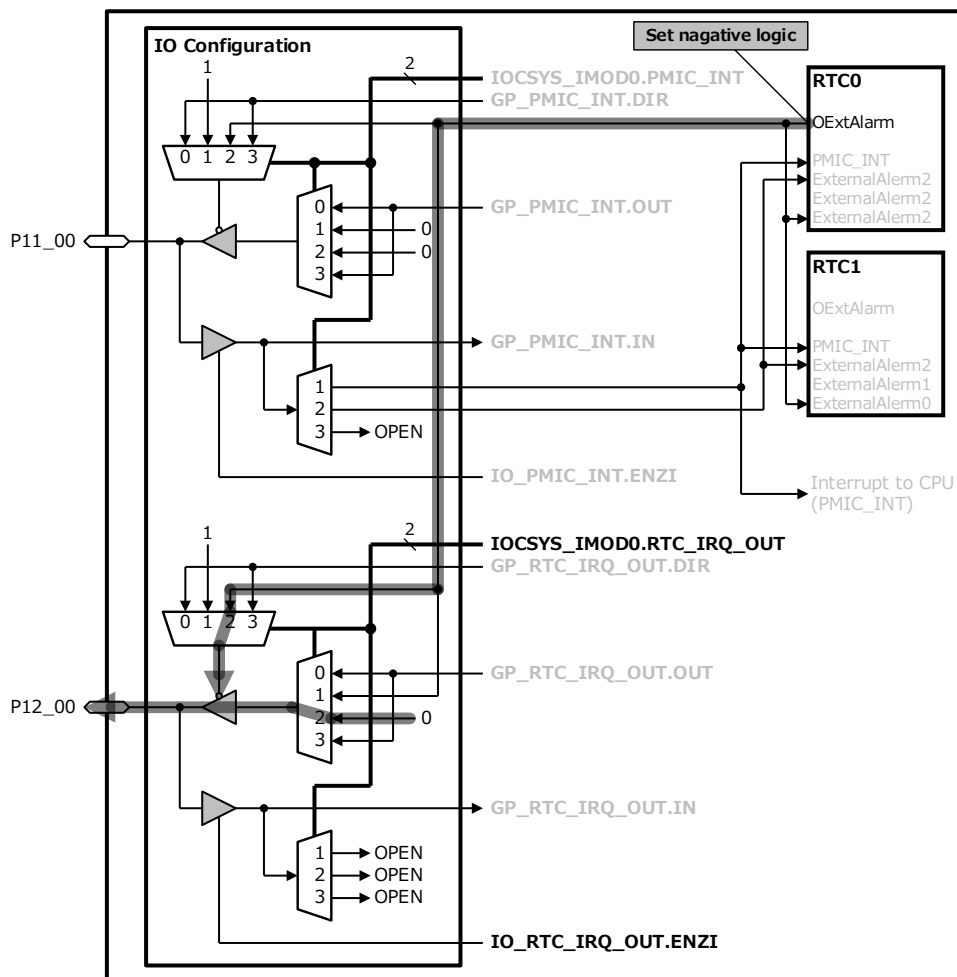


Figure I/O Configuration-12 RTC_IRQ_OUT Signal Routes (MODE=2 Open Drain)

3.1.4.3.6 AP_CLK

The following are settings that pin P13_00 is assigned AP_CLK role.

- **IO_AP_CLK.ENZI=1**
- **IOCSYS_IOMD0.AP_CLK=1**

3.1.4.3.7 PMU_WDT

The following is a setting that pin P13_00 is assigned PMU_WDT role.

- **IOCSYS_IOMD0.AP_CLK=2**

3.1.4.3.8 PMU_WDT (Open Drain)

The following is a setting that pin P13_00 is assigned PMU_WDT (Open Drain) role. The pin becomes to operate as Open Drain and outputs in negative logic.

- **IOCSYS_IOMD0.AP_CLK=3**

3.1.4.3.9 GNSS_1PPS_OUT

The following is a setting that pin P14_00 is assigned GNSS_1PPS_OUT role.

- **IOCSYS_IOMD0.GNSS_1PPS_OUT=1**

The following is a setting that pin P02_00 is assigned GNSS_1PPS_OUT role.

- **IOCSYS_IOMD1.HIFIRQ=3**

3.1.4.3.10 CPU_WDT

The following is a setting that pin P14_00 is assigned CPU_WDT role.

- **IOCSYS_IOMD0.GNSS_1PPS_OUT=2**

3.1.4.3.11 CPU_WDT (Open Drain)

The following is a setting that pin P14_00 is assigned CPU_WDT (Open Drain) role. The pin becomes to operate as Open Drain and outputs in negative logic.

- **IOCSYS_IOMD0.GNSS_1PPS_OUT=3**

3.1.4.3.12 UART1

The following are settings that pin P16_{00,01} are assigned UART role.

- **IO_SPI0_SCK.ENZI=1**
- **IOCSYS_IOMD0.SPI0A=1**

3.1.4.3.13 I2C2

The following are settings that pin P17_{00,01} are assigned I2C role.

- **IO_SPI0_MOSI.ENZI=1**
- **IO_SPI0_MISO.ENZI=1**
- **IOCSYS_IOMD0.SPI0B=1**

3.1.4.3.14 SPI0

The following are settings that pin P16_{00,01} and P17_{00,01} are assigned SPI role.

- **IO_SPI0_MISO.ENZI=1**
- **IOCSYS_IOMD0.SPI0A=2**
- **IOCSYS_IOMD0.SPI0B=2**

A function for pin P16_{00,01} are selected by **IOCSYS_IOMD0.SPI0A**.

A function for pin P17_{00,01} are selected by **IOCSYS_IOMD0.SPI0B**.

The following are settings that pin P18_{00,01,02,03} are assigned SPI role.

- **IO_SPI1_IO1.ENZI=1**
- **IOCSYS_IOMD0.SPI1A=2**

Note: SPI0 must not be assigned to both of the two pins.

3.1.4.3.15 SPI1

The following are settings that pin P18_{00,01,02,03} and pin P19_{00,01} are assigned SPI (for accessing Flash memory) role.

- **IO_SPI1_IO0.ENZI=1**
- **IO_SPI1_IO1.ENZI=1**
- **IO_SPI1_IO2.ENZI=1**
- **IO_SPI1_IO3.ENZI=1**
- **IOCSYS_IOMD0.SPI1A=1**
- **IOCSYS_IOMD0.SPI1B=1**

3.1.4.3.16 SPI2

If the pin SYSTEM0 is Low and the pin SYSTEM1 is High when POR is released, pin P00_{00,01} and pin P01_{00,01} are assigned SPI role automatically. For this reason, usually SPI2 role cannot be set by registers.

The following are settings to release roles assigned automatically by pin SYSTEM0 and pin SYSTEM1, and to newly assign pin P00_{00,01} and pin P01_{00,01} SPI role for debugging.

- **DBG_HOSTIF_SEL.LATCH_OFF=1**
- **IO_SPI2_CS_X.ENZI=1**
- **IO_SPI2_SCK.ENZI=1**
- **IO_SPI2_MOSI.ENZI=1**
- **IOCSYS_IOMD0.SPI2A=1**
- **IOCSYS_IOMD0.SPI2B=1**

3.1.4.3.17 UART0

If the pin SYSTEM0 is High and the pin SYSTEM1 is Low when POR is released, pin P00_{00,01} are assigned UART role automatically. For this reason, usually UART0 role cannot be set by registers.

The following is a setting that pin P01_{00,01} are used as URAT0_CTS or UART0_RTS.

- **IOCSYS_IOMD0.SPI2B=2**

The following are settings to release roles assigned automatically by pin SYSTEM0 and pin SYSTEM1, and to newly assign pin P00_{00,01} and pin P01_{00,01} UART role for debugging.

- **DBG_HOSTIF_SEL.LATCH_OFF=1**
- **IO_SPI2_SCK.ENZI=1** (RXD input)
- **IO_SPI2_MOSI.ENZI=1** (CTS input)
- **IOCSYS_IOMD0.SPI2A=2**
- **IOCSYS_IOMD0.SPI2B=2**

3.1.4.3.18 I2C3

If the pin SYSTEM0 is Low and the pin SYSTEM1 is Low when POR is released, pin P00_{00,01} are assigned I2C role automatically. For this reason, usually I2C3 role cannot be set by registers.

The following are settings to release roles assigned automatically by pin SYSTEM0 and pin SYSTEM1, and to newly assign pin P00_{00,01} I2C role for debugging.

- **DBG_HOSTIF_SEL.LATCH_OFF=1**
- **IO_SPI2_CS_X.ENZI=1**
- **IO_SPI2_SCK.ENZI=1**
- **IOCSYS_IOMD0.SPI2A=3**

3.1.4.3.19 HIF_IRQ_OUT

The following is a setting that pin P02_00 is assigned HIF_IRQ_OUT role.

- **IOCSYS_IOMD0.HIFIRQ=1**

3.1.4.3.20 HIF_IRQ_OUT (Open Drain)

The following is a setting that pin P02_00 is assigned HIF_IRQ_OUT role. The pin becomes to operate as Open Drain and outputs in negative logic.

- **IOCSYS_IOMD0.HIFIRQ=2**

3.1.4.3.21 GPS_EXTLD

The following are settings that pin P03_00 is assigned GPS_EXTLD role.

- **IO_HIF_GPIO0.ENZI=1**
- **IOCSYS_IOMD0.HIFEXT=3**

3.1.4.3.22 SEN_IRQ_IN

The following are settings that pin P1e_00 is assigned SEN_IRQ_IN role.

- **IO_SEN_IRQ_IN.ENZI=1**
- **IOCSYS_IOMD1.SEN_IRQ_IN=1**

3.1.4.3.23 SPI3

The following are settings that pin P1f_00, pin P1g_00, pin P1h_00, and pin P1i_{00,01,02} are assigned SPI role.

- **IO_SPI3_MISO.ENZI=1**
- **IOCSYS_IOMD1.SPI3_CS0_X=1**
- **IOCSYS_IOMD1.SPI3_CS1_X=1**
- **IOCSYS_IOMD1.SPI3_CS2_X=1**
- **IOCSYS_IOMD1.SPI3=1**

3.1.4.3.24 I2C0

The following are settings that pin P1j_{00,01} is assigned I2C role.

- **IO_I2C0_BCK.ENZI=1**
- **IO_I2C0_BDT.ENZI=1**
- **IOCSYS_IOMD1.I2C0=1**

3.1.4.3.25 I2C1

The following are settings that pin P1l_{00,01} are assigned I2C role.

- **IO_PWM2.ENZI=1**
- **IO_PWM3.ENZI=1**
- **IOCSYS_IOMD1.PWMB=2**

3.1.4.3.26 PWM

The following are settings that pin P1k_{00,01} and pin P1l_{00,01} are assigned PWM role.

- **IOCSYS_IOMD1.PWMA=1**
- **IOCSYS_IOMD1.PWMB=1**

3.1.4.3.27 Image Sensor

The following are settings that pin P1m_{00,01,02,03,04,05,06,07,08,09,10} are assigned Image Sensor role.

- **IO_IS_CLK.ENZI=1**
- **IO_IS_VSYNC.ENZI=1**
- **IO_IS_HSYNC.ENZI=1**
- **IO_IS_DATA{0~7}.ENZI=1**
- **IOCAPP_IOMD.IS=1**

3.1.4.3.28 UART2(APP_UART)

The following are settings that pin P1n_{00,01,02,03} are assigned UART role.

- **IO_UART2_RXD.ENZI=1**
- **IO_UART2_CTS.ENZI=1**
- **IOCAPP_IOMD.UART2=1**

3.1.4.3.29 SPI4(APP_SPI)

The following are settings that pin P1o_{00,01,02,03} are assigned SPI role.

- **IO_SPI4_MISO.ENZI=1**
- **IOCAPP_IOMD.SPI4=1**

3.1.4.3.30 EMMC

The following are settings that pin P1p{00,01,02,03} and pin P1q_{00,01} are assigned EMMC role.

- **IO_EMMC_CMD.ENZI=1**
- **IO_EMMC_DATA{0~3}.ENZI=1**
- **IOCAPP_IOMD.EMMCA=1**
- **IOCAPP_IOMD.EMMCB=1**

3.1.4.3.31 SDIO

The following are settings that pin P1r_{00,01,02,03,04,05}, pin P1s{00,01}, pin P1t_{00,01,02}, and pin P1u_00 are assigned SDIO role.

- **IO_SIDO_CLK.ENZI=1**
- **IO_SIDO_CMD.ENZI=1**
- **IO_SIDO_DATA{0~3}.ENZI=1**
- **IO_SIDO_CD.ENZI=1**
- **IO_SIDO_WP.ENZI=1**
- **IO_SIDO_CLKI.ENZI=1**
- **IOCAPP_IOMD.SDIOA=1**
- **IOCAPP_IOMD.SDIOB=1**
- **IOCAPP_IOMD.SDIOC=1**
- **IOCAPP_IOMD.SDIOD=1**

Figure I/O Configuration-13 shows connecting diagram of SDIO input clock.

SDIO IP uses either clock turned inside IOCELL or clock turned outside the LSI.

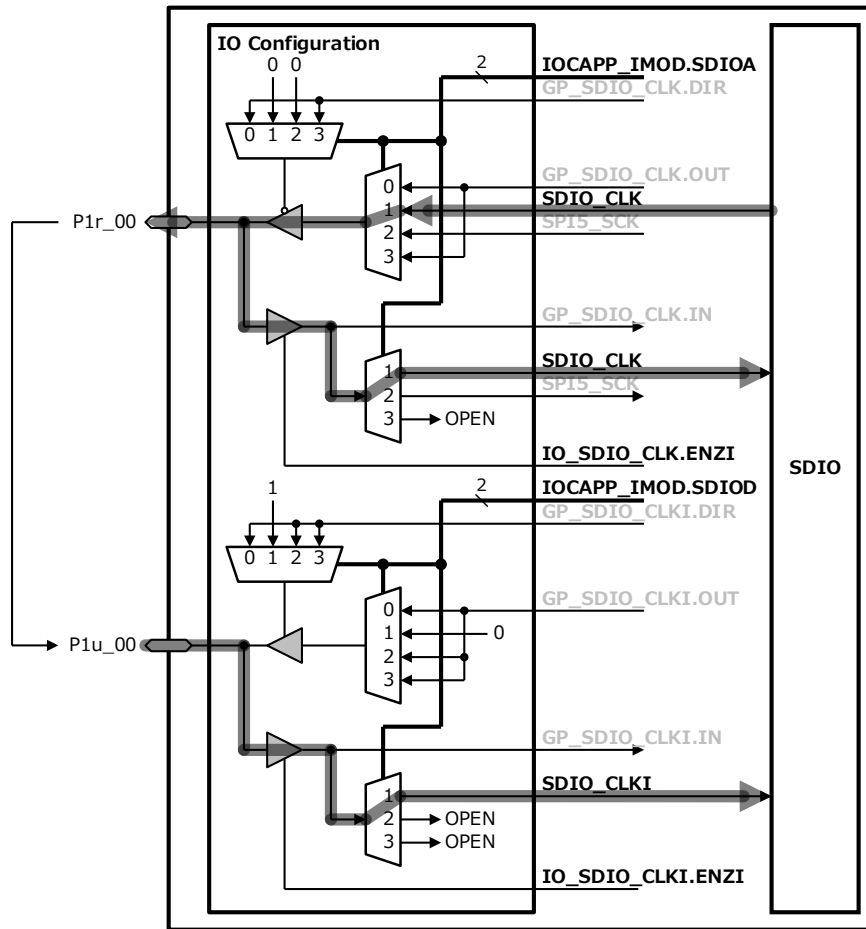


Figure I/O Configuration-13 SDIO CLK Input Schematic

While pin P1s_00 and pin P1s_01 are assigned GPIO role, CD/WP signal of internal IP (SDIO) can be set by using IOFIX_APP. Figure I/O Configuration-14 shows connecting diagram of CD/WP signal to SDIO IP.

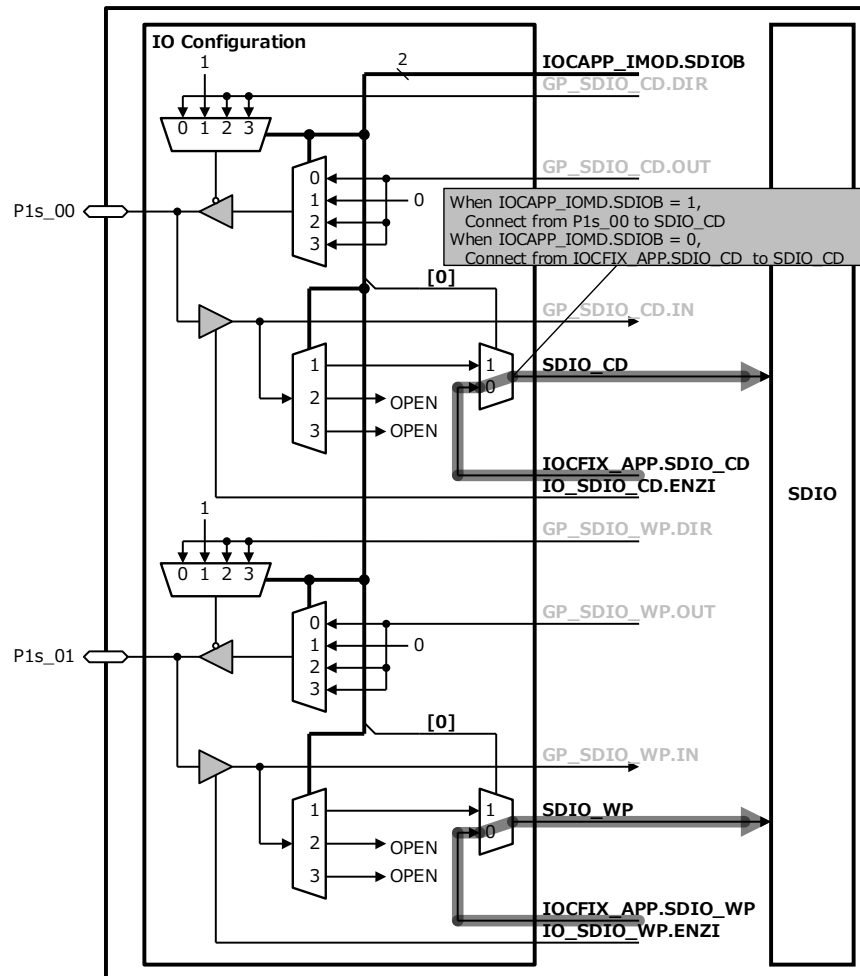


Figure I/O Configuration-14 SDIO WP/CD Input Control Register Schematic

3.1.4.3.32 I2S0

When you use a pin as I2S role, you need to select I2S role by using IOCAPP_IOMD, as well as decide in which mode I2S role should be played, master or slave. According to the decision, you need to set IOOEN_APP adequately.

The following are settings that pin P1v_{00,01,02,03} are used as the I2S master.

- **IO_I2S0_BCK.ENZI=0** (Input Disable)
- **IO_I2S0_LRCK.ENZI=0** (Input Disable)
- **IO_I2S0_DATA_IN.ENZI=1**(Input Enable)
- **IOCAPP_IOMD.I2S0=1**
- **IO_IOOEN_APP.I2S0_BCK=0** (Output Enable)
- **IO_IOOEN_APP.I2S0_LRCK=0** (Output Enable)

The following are settings that pin P1v_{00,01,02,03} are used as the I2S slave.

- **IO_IOOEN_APP.I2S0_BCK=1** (Output Disable)
- **IO_IOOEN_APP.I2S0_LRCK=1** (Output Disable)
- **IO_I2S0_BCK.ENZI=1** (Input Enable)
- **IO_I2S0_LRCK.ENZI=1** (Input Enable)
- **IO_I2S0_DATA_IN.ENZI=1** (Input Enable)
- **IOCAPP_IOMD.I2S0=1**

3.1.4.3.33 I2S1

When you use a pin as I2S role, you need to select I2S role by using IOCAPP_IOMD, as well as decide in which mode I2S role should be played, master or slave. According to the decision, you need to set IOOEN_APP adequately.

The following are settings that pin P1w_{00,01,02,03} are assigned the I2S master.

- **IO_I2S1_BCK.ENZI=0** (Input Disable)
- **IO_I2S1_LRCK.ENZI=0** (Input Disable)
- **IO_I2S1_DATA_IN.ENZI=1**(Input Enable)
- **IOCAPP_IOMD.I2S1=1**
- **IO_IOOEN_APP.I2S1_BCK=0** (Output Enable)
- **IO_IOOEN_APP.I2S1_LRCK=0** (Output Enable)

The following are settings that pin P1w_{00,01,02,03} are assigned the I2S slave.

- **IO_IOOEN_APP.I2S1_BCK=1** (Output Disable)
- **IO_IOOEN_APP.I2S1_LRCK=1** (Output Disable)
- **IO_I2S1_BCK.ENZI=1** (Input Enable)
- **IO_I2S1_LRCK.ENZI=1** (Input Enable)
- **IO_I2S1_DATA_IN.ENZI=1** (Input Enable)
- **IOCAPP_IOMD.I2S1=1**

3.1.4.3.34 MCLK

The following are settings that pin P1x_00 is assigned Master Clock (MCLK) role.

- **IO_MCLK.ENZI=1** (Input Enable)
- **IOCAPP_IOMD.MCLK=1**

3.1.4.3.35 PDM

The following are settings that pin P1y_{00,01,02} are assigned PDM_OUT role (OFS_CLK output).

- **IO_PDM_IN.ENZI=1** (Input Enable)
- **AUDIO_IF_SEL.PDM_CLK_SEL=0**
- **IOCAPP_IOMD.PDM=1**

The following are settings that pin P1y_{00,01,02} are assigned PDM_OUT role (MCK_DMIC output).

- **IO_PDM_IN.ENZI=1** (Input Enable)
- **AUDIO_IF_SEL.PDM_CLK_SEL=1**
- **IOCAPP_IOMD.PDM=1**

3.1.4.3.36 USB_VBUSINT

The following are settings that pin P1z_00 is assigned USB_VBUSINT input role.

- **IO_USB_VBUSINT.ENZI=1**(Input Enable)
- **IOCAPP_IOMD.USBVBUS=1**

3.1.4.3.37 SPI5

The following are settings that pin P1p_{00,01,02,03} are assigned SPI role.

- **IO_EMMC_DATA1.ENZI=1**(Input Enable)
- **IOCAPP_IOMD.EMMCA=2**

The following are settings that pin P1r_{00,01,02,03} are assigned SPI role. In this setting, pin P1r_{04,05} can be used as GPIO role.

- **IO_SDIO_DATA1.ENZI=1**(Input Enable)
- **IOCAPP_IOMD.SDIOA=2**
-

Note: SPI5 must not be assigned to both of the two pins.

3.2 General Purpose Input/Output (GPIO)

3.2.1 Outlines and Features

In the chapter of GPIO, GPIO control, detection control, and pin selection for interrupt are explained.

3.2.2 Function List

Table General Purpose Input/Output (GPIO)-19 Function List

No	Function Name	Description
1	GPIO Control	controls I/O pins to switch between input and output
2	I/O Pin Selection	selects I/O pins used for interrupts
3	External Interrupt Option	selects an interrupt option for outputting to SYSCPU and DSP
4	Event Detection Control	controls “Event Detection” that can be selected as an option described in the No. 3 above

3.2.3 Function Specification Outlines

3.2.3.1 Function Block Diagrams

Figure General Purpose Input/Output (GPIO)-15 shows entire functions of GPIO and Figure General Purpose Input/Output (GPIO)-16 shows Event Detect block inside GPIO function.

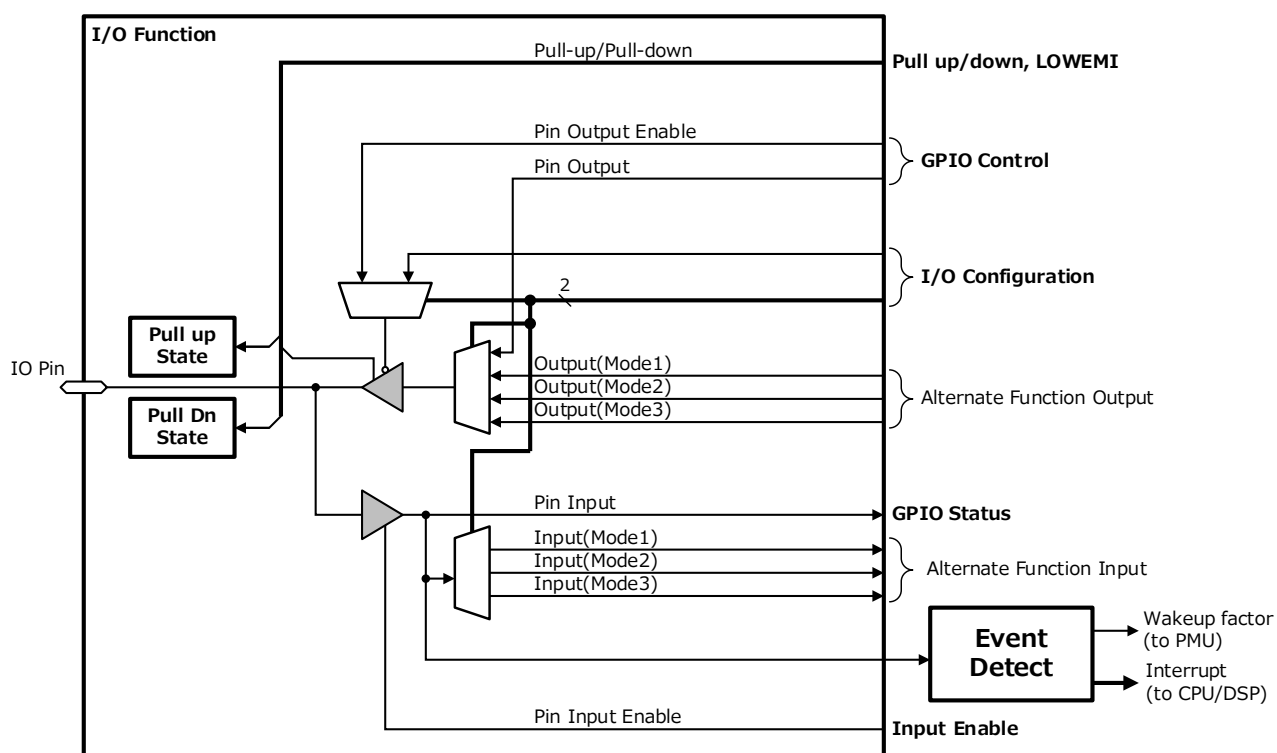


Figure General Purpose Input/Output (GPIO)-15 GPIO Overview Block Diagram

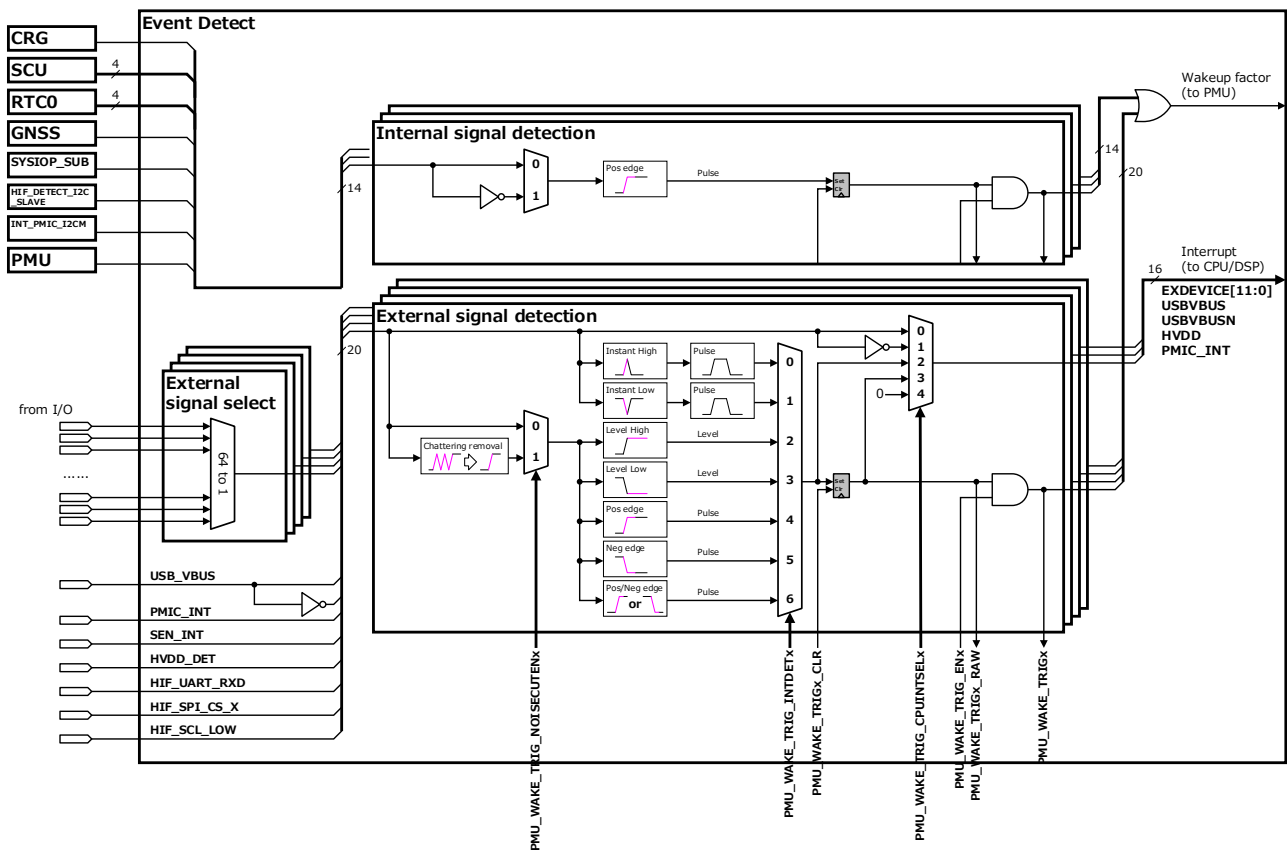


Figure General Purpose Input/Output (GPIO)-16 Diagram of GPIO Event Detect Block

3.2.4 Detailed Function and Control Specification

3.2.4.1 GPIO Control

GPIO Control can be performed when I/O pins are set as GPIO mode. The GPIO mode can be set by using Pin Multiplexer register **IOCSYS_IOMD{0,1}** or **IOCAPP_IOMD{0,1}**. For details for setting GPIO mode, refer to Section 3.1.4 (Pin Multiplexer). Table General Purpose Input/Output (GPIO)-20 shows GPIO control registers.

Table General Purpose Input/Output (GPIO)-20 GPIO Control Register

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04102000 0x04102188	GP_* (1*)	Reserved	RO	[31:17]	0	Reserved
		DIR	RW	[16]	1	OutputEnable control in GPIO mode 0: OutputEnable, 1: OutputDisable
		Reserved	RO	[15:9]	0	Reserved
		OUT	RW	[8]	0	OutputData control in GPIO mode
		Reserved	RO	[7:1]	0	Reserved
		IN	RO	[0]	0	I/O pin value

(1*): A register is prepared for each I/O pin. For correspondence of I/O pins to registers, refer to Table General Purpose Input/Output (GPIO)-21.

- **GP_*.DIR**: Control of OutputEnable
Set the register OutputEnable when you use GPIO as output, set it OutputDisable when you use GPIO as input.
- **GP_*.IN**: Confirmation of I/O pin value
By setting **IO_*.ENZI** = 1 (refer to 3.1 in the chapter of IO Configuration), the I/O pin value can be read. The value can be read not only under GPIO output control, but also under other than GPIO controls.
- **GP_*.OUT**: Control of OutputData
0/1 is output to an I/O pin according to the control register setting.

Table General Purpose Input/Output (GPIO)-21 Correspondence of GPIO Control Registers to I/O Pins

Register Name	Pin Name	Register Name	Pin Name	Register Name	Pin Name
GP_I2C4_BCK	P10_00	GP_I2C0_BCK	P1j_00	GP_EMMC_DATA2	P1q_00
GP_I2C4_BDT	P10_01	GP_I2C0_BDT	P1j_01	GP_EMMC_DATA3	P1q_01
GP_PMIC_INT	P11_00	GP_PWM0	P1k_00	GP_SDIO_CLK	P1r_00
GP_RTC_IRQ_OUT	P12_00	GP_PWM1	P1k_01	GP_SDIO_CMD	P1r_01
GP_AP_CLK	P13_00	GP_PWM2	P1l_00	GP_SDIO_DATA0	P1r_02
GP_GNSS_1PPS_OUT	P14_00	GP_PWM3	P1l_01	GP_SDIO_DATA1	P1r_03
GP_SPI0_CS_X	P16_00	GP_IS_CLK	P1m_00	GP_SDIO_DATA2	P1r_04
GP_SPI0_SCK	P16_01	GP_IS_VSYNC	P1m_01	GP_SDIO_DATA3	P1r_05
GP_SPI0_MOSI	P17_00	GP_IS_HSYNC	P1m_02	GP_SDIO_CD	P1s_00
GP_SPI0_MISO	P17_01	GP_IS_DATA0	P1m_03	GP_SDIO_WP	P1s_01
GP_SPI1_CS_X	P18_00	GP_IS_DATA1	P1m_04	GP_SDIO_CMDDIR	P1t_00
GP_SPI1_SCK	P18_01	GP_IS_DATA2	P1m_05	GP_SDIO_DIR0	P1t_01
GP_SPI1_IO0	P18_02	GP_IS_DATA3	P1m_06	GP_SDIO_DIR1_3	P1t_02
GP_SPI1_IO1	P18_03	GP_IS_DATA4	P1m_07	GP_SDIO_CLKI	P1u_00
GP_SPI1_IO2	P19_00	GP_IS_DATA5	P1m_08	GP_I2S0_BCK	P1v_00
GP_SPI1_IO3	P19_01	GP_IS_DATA6	P1m_09	GP_I2S0_LRCK	P1v_01
GP_SPI2_CS_X	P00_00	GP_IS_DATA7	P1m_10	GP_I2S0_DATA_IN	P1v_02
GP_SPI2_SCK	P00_01	GP_UART2_TXD	P1n_00	GP_I2S0_DATA_OUT	P1v_03
GP_SPI2_MOSI	P01_00	GP_UART2_RXD	P1n_01	GP_I2S1_BCK	P1w_00
GP_SPI2_MISO	P01_01	GP_UART2_CTS	P1n_02	GP_I2S1_LRCK	P1w_01
GP_HIF_IRQ_OUT	P02_00	GP_UART2_RTS	P1n_03	GP_I2S1_DATA_IN	P1w_02
GP_HIF_GPIO0	P03_00	GP_SPI4_CS_X	P1o_00	GP_I2S1_DATA_OUT	P1w_03
GP_SEN_IRQ_IN	P1e_00	GP_SPI4_SCK	P1o_01	GP_MCLK	P1x_00
GP_SPI3_CS0_X	P1f_00	GP_SPI4_MOSI	P1o_02	GP_PDM_CLK	P1y_00
GP_SPI3_CS1_X	P1g_00	GP_SPI4_MISO	P1o_03	GP_PDM_IN	P1y_01
GP_SPI3_CS2_X	P1h_00	GP_EMMC_CLK	P1p_00	GP_PDM_OUT	P1y_02
GP_SPI3_SCK	P1i_00	GP_EMMC_CMD	P1p_01	GP_USB_VBUSINT	P1z_00
GP_SPI3_MOSI	P1i_01	GP_EMMC_DATA0	P1p_02	-	-
GP_SPI3_MISO	P1i_02	GP_EMMC_DATA1	P1p_03	-	-

GPIO Output Control

0/1 can be output to an I/O pin according to the control register setting. The status that a control register value is directly output to an I/O pin is called GPIO Output Control.

Settings in GPIO Output Control are described below.

- **GP_*.DIR** = 0 (OutputEnable)
- **{IOCSYS/IOCAPP}_IOMD{0/1}.*** = 0
- **GP_*.OUT** = any value

Figure General Purpose Input/Output (GPIO)-17 shows a visualized function controlled by GPIO parameter that is set by GPIO output control register.

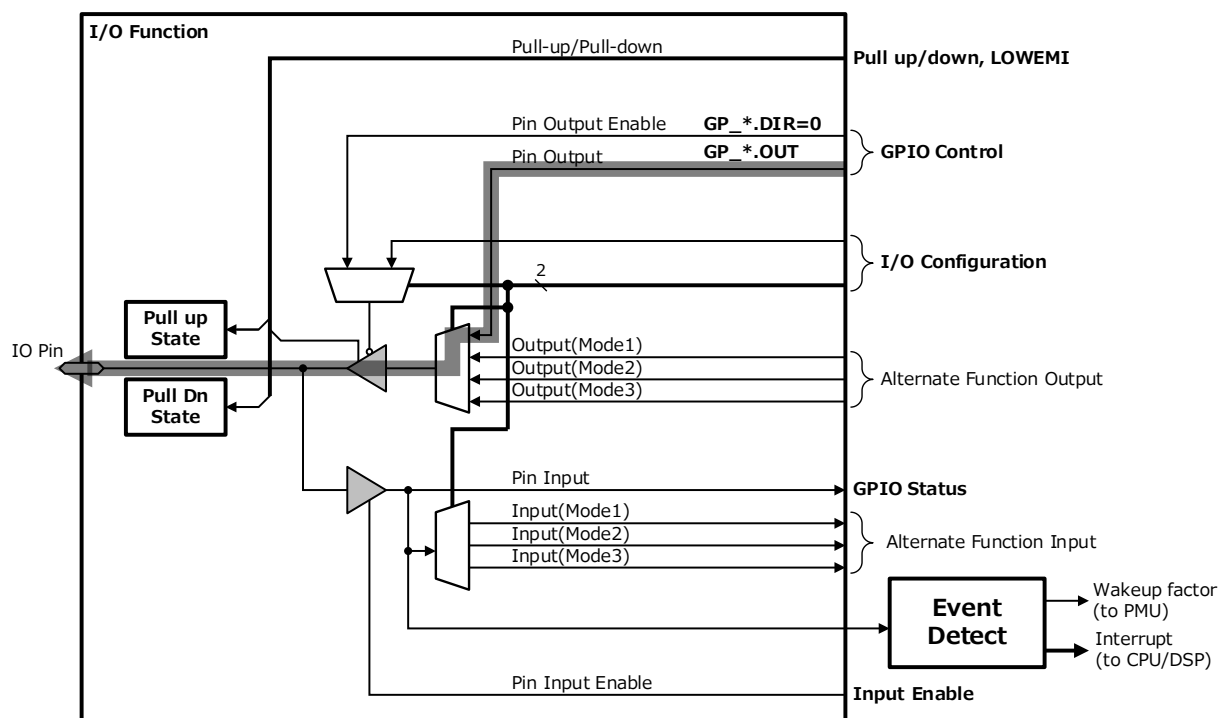


Figure General Purpose Input/Output (GPIO)-17 Output Signal Route in the I/O Function Controlled by GPIO Parameter

For example, the settings that pin P10_00 is assigned GPIO output control function are described below.

- **GP_I2C4_BCK.DIR** = 0 (OutputDisable)
- **IOCSYS_IOMD0.I2C4** = 0
- **GP_I2C4_BCK.OUT** = (1/0)

GPIO Input Control

Values that are input to I/O pins can be read out as the status registers. As for the inputs, the status registers can be read out without any special settings. This function is called “input control” in contrast to output control but actually the “input control” does not control input. The input control is particularly called GPIO input control when it is used as GPIO.

Settings in GPIO input control are described below.

- **IO_*.ENZI** = 1 (InputEnable)
- **GP_*.DIR** = 1 (OutputDisable)
- **IOCSYS_IOMD{0,1}.*** = 0 (SYS Group) or **IOCAPP_IOMD{0,1}.*** = 0 (APP Group)
- Confirm the input value by reading **GP_*.IN**.

Figure General Purpose Input/Output (GPIO)-18 shows a visualized function controlled by GPIO parameter that is set by GPIO input control register.

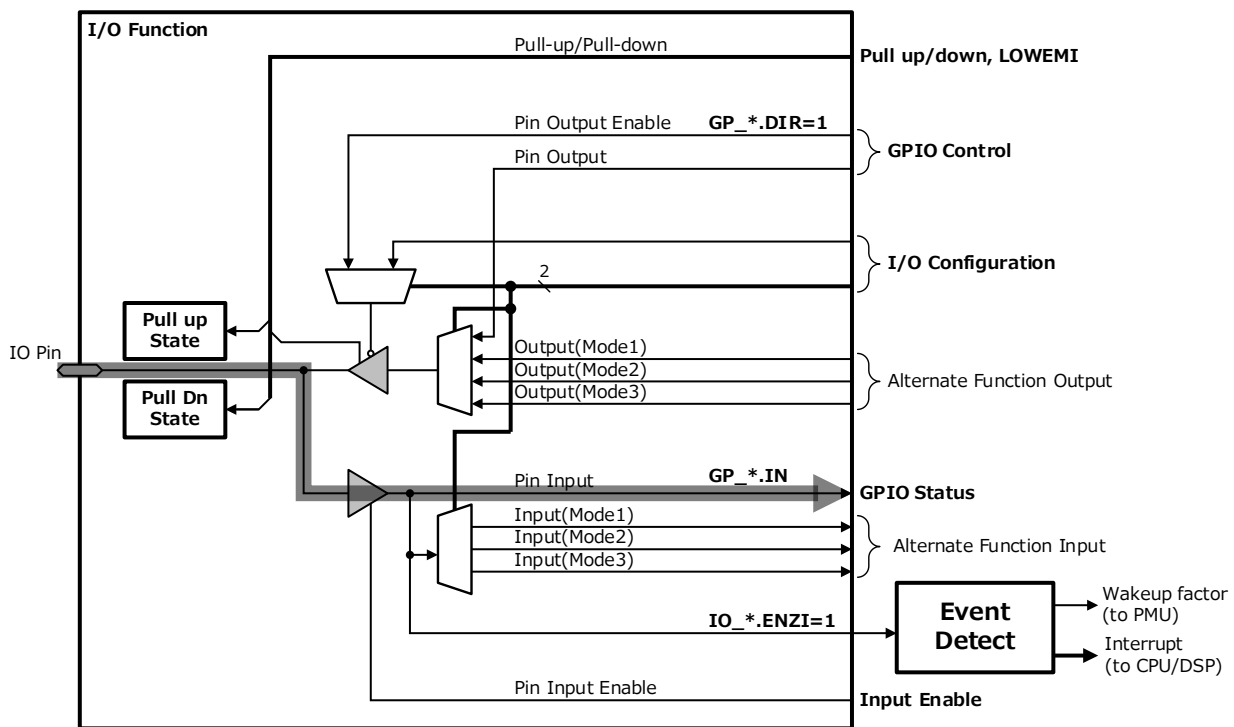


Figure General Purpose Input/Output (GPIO)-18 Input Signal Route in the I/O Function Controlled by GPIO Parameter

For example, the settings that pin P10_00 is assigned GPIO input control function are described below.

- **IO_I2C4_BCK.ENZI** = 1 (InputEnable)
- **GP_I2C4_BCK.DIR** = 1 (OutputDisable)
- **IOCSYS_IOMD0.I2C4** = 0
- Confirm the input value by reading **GP_I2C4_BCK.IN**.

3.2.4.2 I/O Pin Selection

In the chapter of I/O Pin Selection, how to select pins used as external interrupts is explained. I/O pins used as interrupts are classified into two groups: SYS group and APP group. You can select six pins each from both SYS group and APP group. Table General Purpose Input/Output (GPIO)-23 shows I/O pins belonging to SYS group, and Table General Purpose Input/Output (GPIO)-25 shows I/O pins belonging to APP group. Figure General Purpose Input/Output (GPIO)-19 shows the function in the Event Detect Block, which is explained in this section.

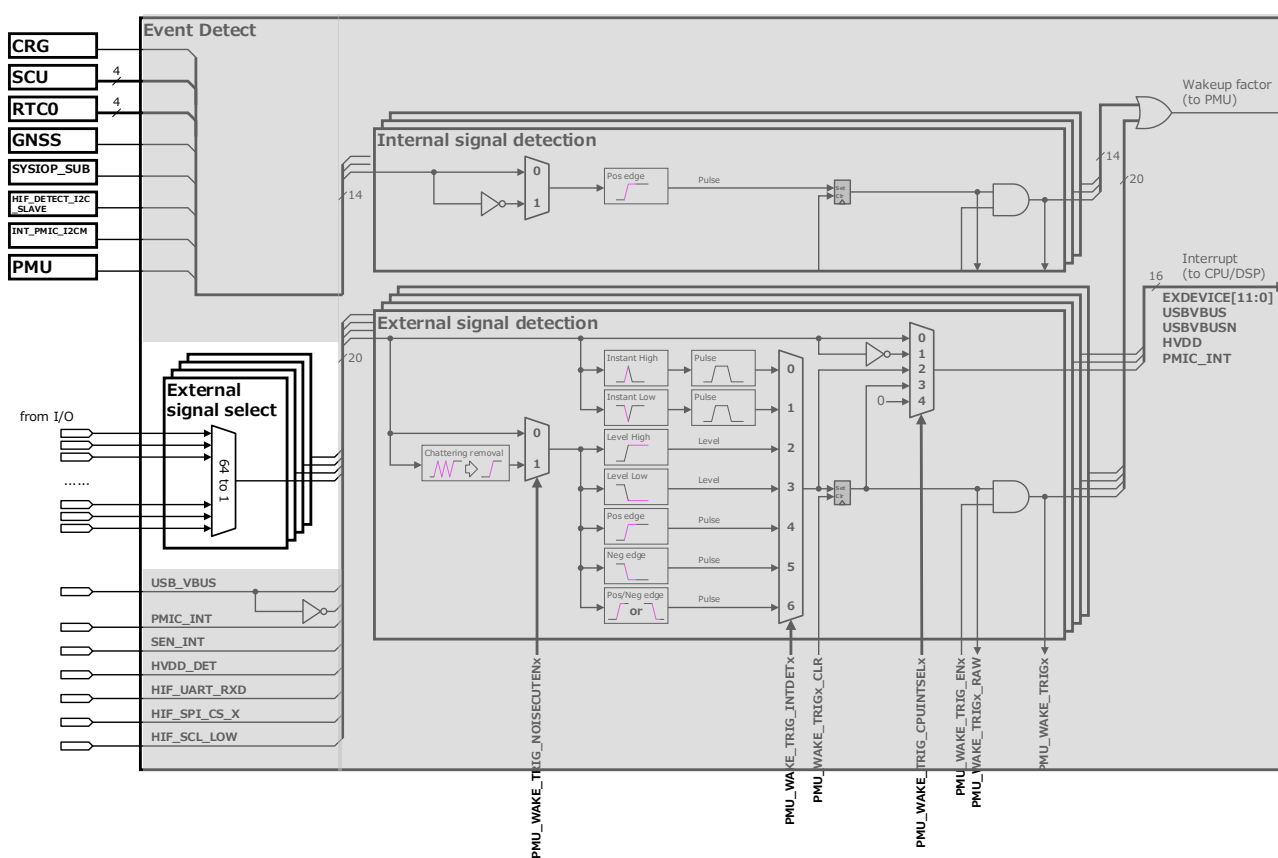


Figure General Purpose Input/Output (GPIO)-19 GPIO Pin Selection

Table General Purpose Input/Output (GPIO)-22 and Table General Purpose Input/Output (GPIO)-24 show registers that select I/O pins, Table General Purpose Input/Output (GPIO)-23 and Table General Purpose Input/Output (GPIO)-25 show selectable I/O pins. Initial value of a register is set as 63. In this case, no I/O pin is selected and an input value to the circuit for detecting interrupts or events is tied to “0”.

As for the selected external interrupt I/O pin, the Input Enable needs to be valid by setting 1 on the register **IO_*.ENZI**.

Table General Purpose Input/Output (GPIO)-22 IO Pin Selection (SYS Group)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041007B0	IOCSYS_INTSEL0	Reserved	RO	[31:30]	0	Reserved
		SEL3	RW	[29:24]	63	assigns an I/O pin to an external signal (SYSGPI3)
		Reserved	RO	[23:22]	0	Reserved
		SEL2	RW	[21:16]	63	assigns an I/O pin to an external signal (SYSGPI2)
		Reserved	RO	[15:14]	0	Reserved
		SEL1	RW	[13:8]	63	assigns an I/O pin to an external signal (SYSGPI1)
		Reserved	RO	[7:6]	0	Reserved
		SEL0	RW	[5:0]	63	assigns an I/O pin to an external signal (SYSGPI0)
0x041007B4	IOCSYS_INTSEL1	Reserved	RO	[31:14]	0	Reserved
		SEL5	RW	[13:8]	63	assigns an I/O pin to an external signal (SYSGPI5)
		Reserved	RO	[7:6]	0	Reserved
		SEL4	RW	[5:0]	63	assigns an I/O pin to an external signal (SYSGPI4)

Table General Purpose Input/Output (GPIO)-23 Correspondence of I/O Pins to Setting Values (SYS Group)

Selected Pin Name	Setting Value		Selected Pin Name	Setting Value		Selected Pin Name	Setting Value		Selected Pin Name	Setting Value
P10_00	0		P16_00	16		—	32		P1L_01	48
P10_01	1		P16_01	17		—	33		—	49
P11_00	2		P17_00	18		—	34		—	50
P12_00	3		P17_01	19		—	35		—	51
P13_00	4		P18_00	20		P1e_00	36		—	52
P14_00	5		P18_01	21		P1f_00	37		—	53
—	6		P18_02	22		P1g_00	38		—	54
—	7		P18_03	23		P1h_00	39		—	55
—	8		P19_00	24		P1i_00	40		—	56
—	9		P19_01	25		P1i_01	41		—	57
—	10		P00_00	26		P1i_02	42		—	58
—	11		P00_01	27		P1j_00	43		—	59
—	12		P01_00	28		P1j_01	44		—	60
—	13		P01_01	29		P1k_00	45		—	61
—	14		P02_00	30		P1k_01	46		—	62
—	15		P03_00	31		P1l_00	47		— (default)	63

Table General Purpose Input/Output (GPIO)-24 I/O Pin Selection (APP Group)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04101490	IOCAPP_INTSEL0	Reserved	RO	[31:30]	0	Reserved
		SEL3	RW	[29:24]	63	assigns an I/O pin to an external signal (APPGPI3)
		Reserved	RO	[23:22]	0	Reserved
		SEL2	RW	[21:16]	63	assigns an I/O pin to an external signal (APPGPI2)
		Reserved	RO	[15:14]	0	Reserved
		SEL1	RW	[13:8]	63	assigns an I/O pin to an external signal (APPGPI1)
		Reserved	RO	[7:6]	0	Reserved
		SEL0	RW	[5:0]	63	assigns an I/O pin to an external signal (APPGPI0)
0x04101494	IOCAPP_INTSEL1	Reserved	RO	[31:14]	0	Reserved
		SEL5	RW	[13:8]	63	assigns an I/O pin to an external signal (APPGPI5)
		Reserved	RO	[7:6]	0	Reserved
		SEL4	RW	[5:0]	63	assigns an I/O pin to an external signal (APPGPI4)

Table General Purpose Input/Output (GPIO)-25 Correspondence of I/O Pins to Setting Values (APP Group)

Selected Name	Pin	Setting Value		Selected Name	Pin	Setting Value		Selected Name	Pin	Setting Value		Selected Name	Pin	Setting Value
P1m_00		0		P1o_01		16		P1s_01		32		P1y_02		48
P1m_01		1		P1o_02		17		P1t_00		33		P1z_00		49
P1m_02		2		P1o_03		18		P1t_01		34		—		50
P1m_03		3		P1p_00		19		P1t_02		35		—		51
P1m_04		4		P1p_01		20		P1u_00		36		—		52
P1m_05		5		P1p_02		21		P1v_00		37		—		53
P1m_06		6		P1p_03		22		P1v_01		38		—		54
P1m_07		7		P1q_00		23		P1v_02		39		—		55
P1m_08		8		P1q_01		24		P1v_03		40		—		56
P1m_09		9		P1r_00		25		P1w_00		41		—		57
P1m_10		10		P1r_01		26		P1w_01		42		—		58
P1n_00		11		P1r_02		27		P1w_02		43		—		59
P1n_01		12		P1r_03		28		P1w_03		44		—		60
P1n_02		13		P1r_04		29		P1x_00		45		—		61
P1n_03		14		P1r_05		30		P1y_00		46		—		62
P1o_00		15		P1s_00		31		P1y_01		47		— (default)		63

3.2.4.3 External Interrupt

Selected I/O pins described in the section 3.2.4.2 and some other pins (refer to Table General Purpose Input/Output (GPIO)-27) can be communicated to SYSCPU and DSP as external interrupts with no changes. Besides, not only I/O pins' values themselves can be communicated to SYSCPU and DSP, but information that an event has been detected (refer to 3.2.4.4) can be as well.

Figure General Purpose Input/Output (GPIO)-20 shows the function in the Event Detect Block, which is explained in this section.

Output Selection

- 0: The value of the I/O pin is communicated as an interrupt signal with no changes.
- 1: The inverted value of the I/O pin is communicated as an interrupt signal.
- 2: The result of the event detection is communicated as an interrupt signal with no changes.
- 3: When an event is detected, the register is asserted and communicated as a latched interrupt signal.
- 4-7: The output value is tied to "0".

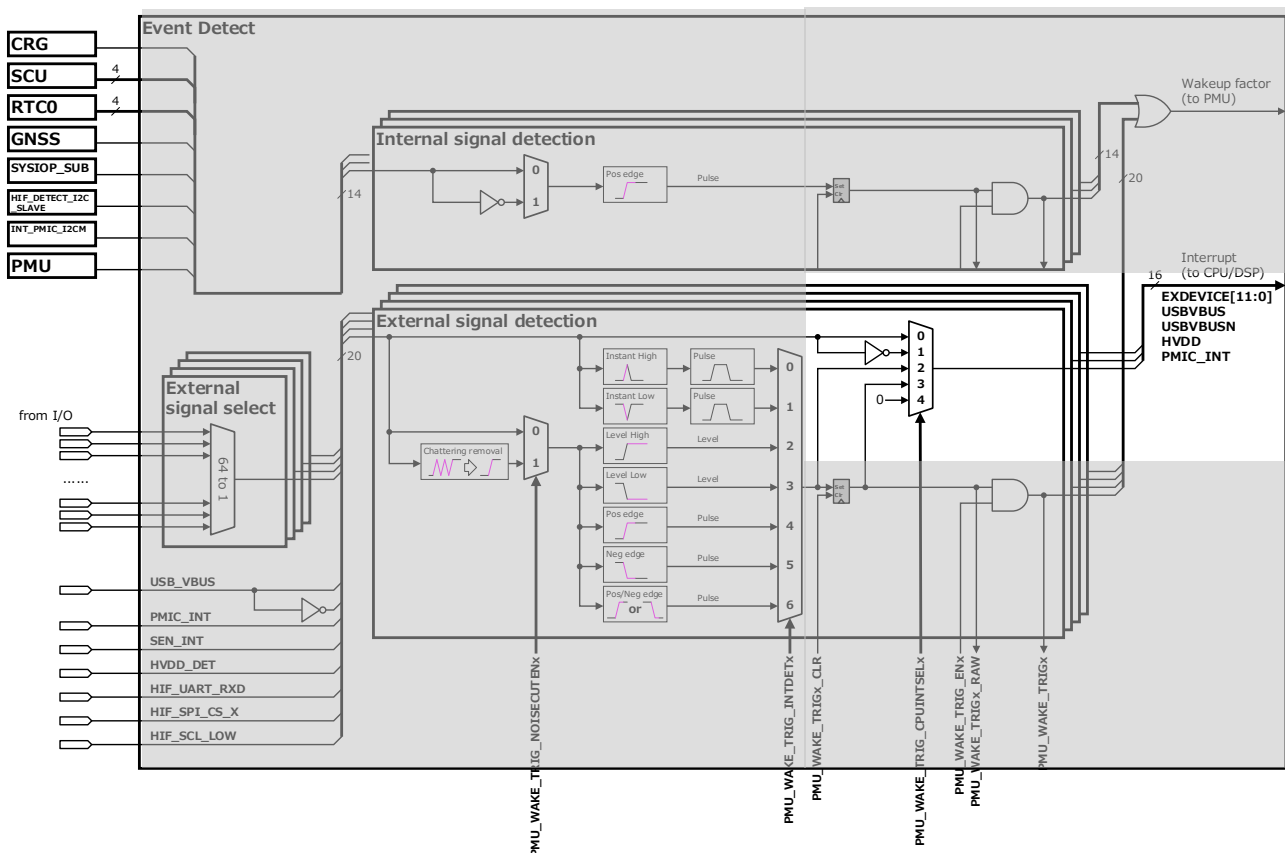


Figure General Purpose Input/Output (GPIO)-20 External Interrupt Selection

Table General Purpose Input/Output (GPIO)-26 shows control registers for processing external interrupt signals.

Table General Purpose Input/Output (GPIO)-26 External Interrupt Selection

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100468	PMU_WAKE_TRIG_CPUINTSEL0	Reserved	RO	[31]	0	Reserved
		SYSGPI3	RW	[30:28]	0	Interrupt options for outputting to SYSCPU and DSP 0: value of I/O pin 1: inverted value of I/O pin 2: result of the event detection 3: If the status is changed to “event not detected”, the former status “event detected” is latched. 4-7: The output value is tied to “0”.
		Reserved	RO	[27]	0	Reserved
		SYSGPI2	RW	[26:24]	0	Refer to SYSGPI3
		Reserved	RO	[23]	0	Reserved
		SYSGPI1	RW	[22:20]	0	Refer to SYSGPI3
		Reserved	RO	[19]	0	Reserved
		SYSGPI0	RW	[18:16]	0	Refer to SYSGPI3
		Reserved	RO	[15]	0	Reserved
		HVDD_DET	RW	[14:12]	0	Refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		HIF_UART_RXD	RW	[10:8]	0	Refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		HIF_SPI_CS_X	RW	[6:4]	0	Refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		HIF_SCL_LOW	RW	[2:0]	0	Refer to SYSGPI3
0x0410046C	PMU_WAKE_TRIG_CPUINTSEL1	Reserved	RO	[31]	0	Reserved
		APPGPI5	RW	[30:28]	0	Refer to SYSGPI3
		Reserved	RO	[27]	0	Reserved
		APPGPI4	RW	[26:24]	0	Refer to SYSGPI3
		Reserved	RO	[23]	0	Reserved
		APPGPI3	RW	[22:20]	0	Refer to SYSGPI3
		Reserved	RO	[19]	0	Reserved

		APPGPI2	RW	[18:16]	0	Refer to SYSGPI3
		Reserved	RO	[15]	0	Reserved
		APPGPI1	RW	[14:12]	0	Refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		APPGPI0	RW	[10:8]	0	Refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		SYSGPI5	RW	[6:4]	0	Refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		SYSGPI4	RW	[2:0]	0	Refer to SYSGPI3
0x04100470	PMU_WAKE_TRIG_ CPUINTSEL2	Reserved	RO	[31:15]	0	Reserved
		USB_VBUS	RW	[14:12]	0	Refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		USB_VBUS_X	RW	[10:8]	0	Refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		PMIC_INT	RW	[6:4]	0	Refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		SEN_INT	RW	[2:0]	0	Refer to SYSGPI3

3.2.4.4 Event Detection Control

Event detection asserts when it detects that a signal meets conditions set for detection. It keeps the status until the control register clears the status. Event Detection Control can perform edge detection, level detection, and instant detection of external signals from I/O pins. Detected events can be used as interrupts.

Figure General Purpose Input/Output (GPIO)-21 shows the function in the Event Detect Block, which is explained in this section.

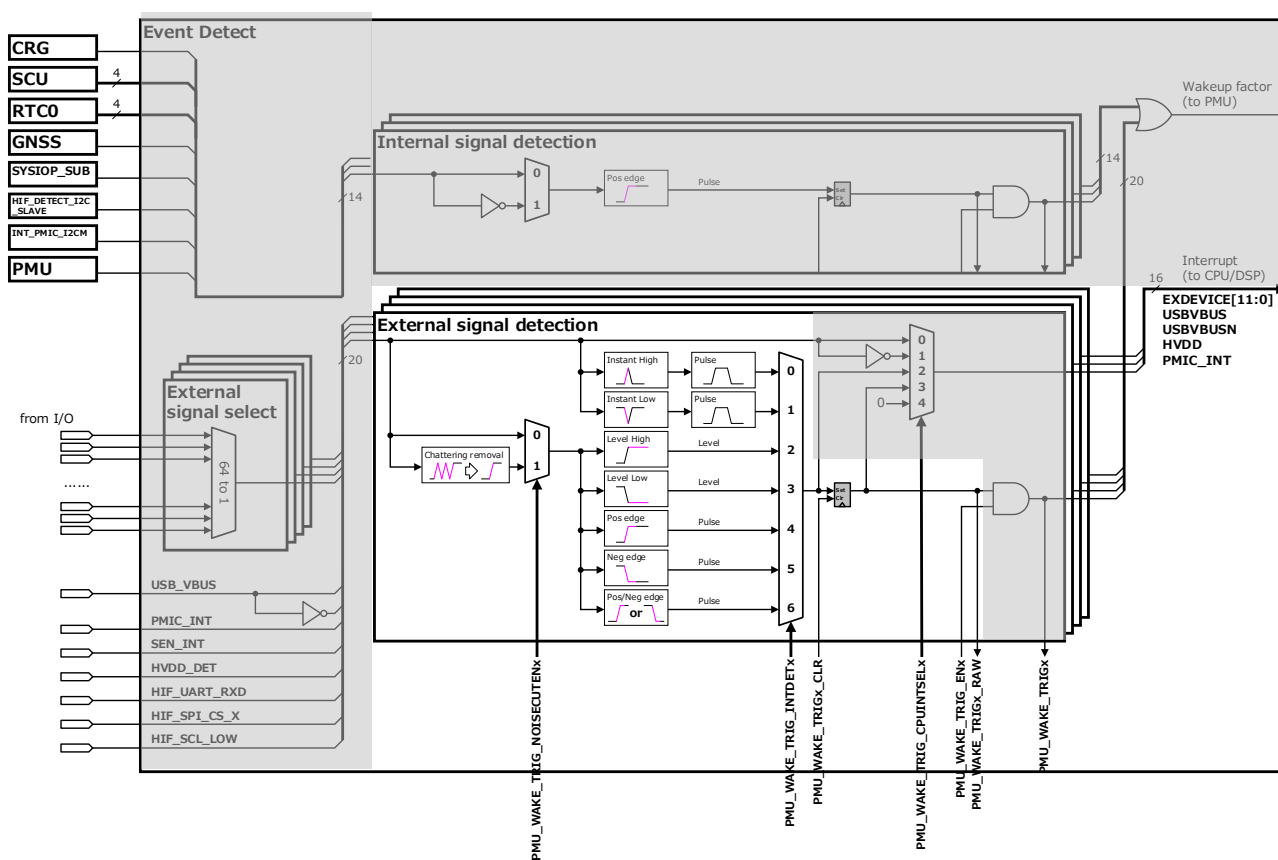


Figure General Purpose Input/Output (GPIO)-21 Event Detection Control

Table General Purpose Input/Output (GPIO)-27 shows I/O pins that can be used for event detection. As for I/O pins that can be used for interrupt (refer to 3.2.4.2), bit-field names of interrupt factor registers are described in the “Interrupt Factor” field of the table. For interrupt factors, refer to Chapter 3.3 (interrupt).

Table General Purpose Input/Output (GPIO)-27 I/O Pins That Can be Used for Event Detection

Pin Name	Bit Field Name of Event Detection Register ^(1*)	I/O Pin Description	Interrupt Factor
P1z_00	USB_VBUS	detects connection or disconnection of USB (in positive logic) Both positive and negative logics are prepared to detect both connection and disconnection of USB.	USBVBUS
P1z_00	USB_VBUS_X	detects connection or disconnection of USB (in negative logic)	USBVBUSN
P11_00	PMIC_INT	detects interrupts that are output from CXD5247 basically connects alarm interrupts of CXD5247	PMIC_INT
P1e_00	SEN_INT	detects interrupts (SEN_IRQ_IN) that are output from sensors Interrupts from external sensor devices connected to SCU are assumed.	-
refer to Table General Purpose Input/Out put (GPIO)-2 5	APPGPI5	I/O pin selected by IOCAPP_INTSEL1.SEL5	EXDEVICE[11]
	APPGPI4	I/O pin selected by IOCAPP_INTSEL1.SEL4	EXDEVICE[10]
	APPGPI3	I/O pin selected by IOCAPP_INTSEL0.SEL3	EXDEVICE[9]
	APPGPI2	I/O pin selected by IOCAPP_INTSEL0.SEL2	EXDEVICE[8]
	APPGPI1	I/O pin selected by IOCAPP_INTSEL0.SEL1	EXDEVICE[7]
	APPGPI0	I/O pin selected by IOCAPP_INTSEL0.SEL0	EXDEVICE[6]
refer to Table General Purpose Input/Out put (GPIO)-2 3	SYSGPI5	I/O pin selected by IOCSYS_INTSEL1.SEL5	EXDEVICE[5]
	SYSGPI4	I/O pin selected by IOCSYS_INTSEL1.SEL4	EXDEVICE[4]
	SYSGPI3	I/O pin selected by IOCSYS_INTSEL0.SEL3	EXDEVICE[3]
	SYSGPI2	I/O pin selected by IOCSYS_INTSEL0.SEL2	EXDEVICE[2]
	SYSGPI1	I/O pin selected by IOCSYS_INTSEL0.SEL1	EXDEVICE[1]
	SYSGPI0	I/O pin selected by IOCSYS_INTSEL0.SEL0	EXDEVICE[0]
-	HVDD_DET	detects status change of IO power supply of HOST I/F	HVDD
P00_01	HIF_UART_RXD	detects UART0_RXD = L	-

		detects UART communication from external HOST devices when HOST I/F is UART	
P00_00	HIF_SPI_CS_X	detects SPI2_CS_X = L detects SPI communications from external HOST when HOST I/F is SPI	-
P00_00	HIF_SCL_LOW	detects I2C3_BCK = L detects I2C communications from external HOST devices when HOST I/F is I2C	-

^(1*) Applicable Registers

- PMU_WAKE_TRIG_NOISECUTEN0
- PMU_WAKE_TRIG_INTDET0
- PMU_WAKE_TRIG_INTDET1
- PMU_WAKE_TRIG_INTDET2
- PMU_WAKE_TRIG_EN0
- PMU_WAKE_TRIG0_RAW
- PMU_WAKE_TRIG0
- PMU_WAKE_TRIG0_CLR

3.2.4.4.1 How to Detect Events (External Signal)

There are seven ways of detecting events by an external signal from I/O pin. You can select one from them by using a register for each I/O pin.

Selection of the way of detecting events (PMU_WAKE_TRIG_INTDET*)

(0) Instant High Detection

(1) Instant Low Detection

(2) Level High Detection

(3) Level Low Detection

(4) Rising Edge Detection

(5) Falling Edge Detection

(6) Both Edge Detection

(7) Both Edge Detection (This function removes information of event detection that is made when CXD5602 is reset and then the reset is released while the status of the I/O pin is High. That is because the input value of the I/O pin is not actually changed.)

When you select (6), right after the reset is released when the status of the I/O pin is High, an event is detected.

If you want to eliminate this determination, use (7).

When you select (2) to (7), if you set debounce function (PMU_WAKE_TRIG_NOISECUTEN0) as effective, you can remove signal changes of two cycles of RTC Clock or less.

Figure General Purpose Input/Output (GPIO)-22 shows event detection timings of (0) to (5) of the above seven ways.

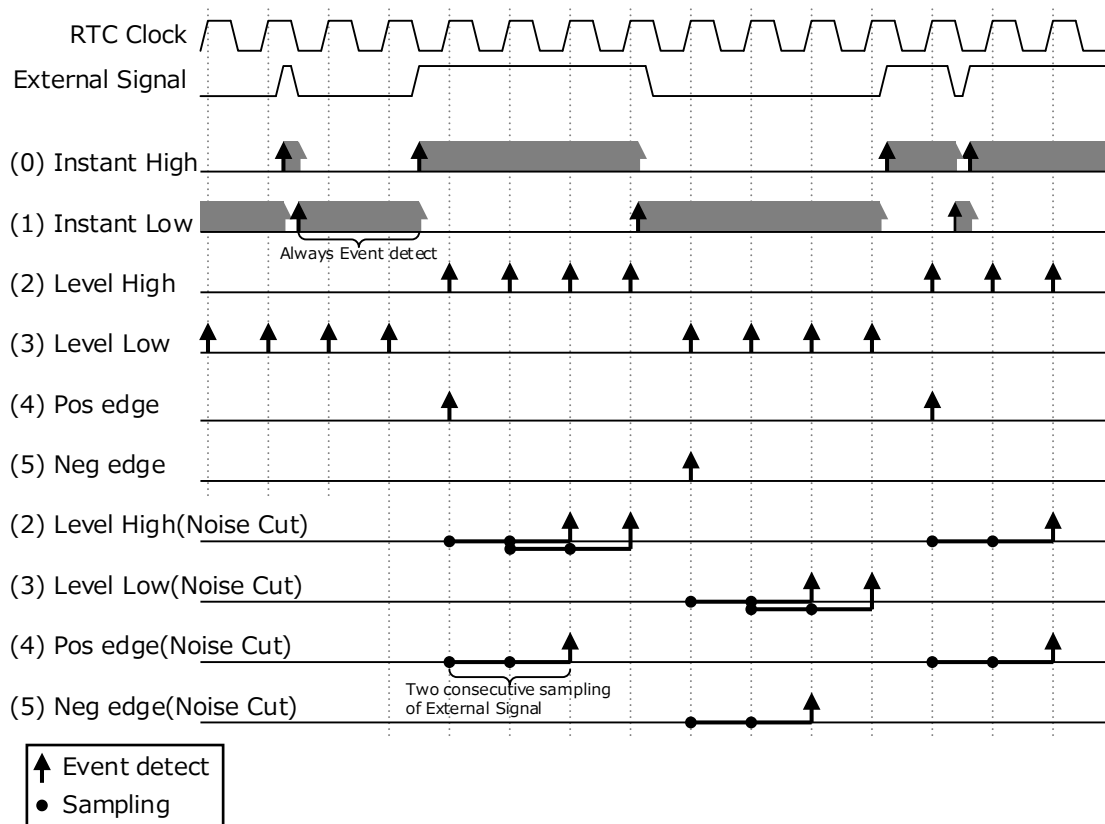


Figure General Purpose Input/Output (GPIO)-22 Event Detection Timing Diagram

Table General Purpose Input/Output (GPIO)-28 shows registers for setting Event Detection of I/O pins.

Table General Purpose Input/Output (GPIO)-28 Event Detection Setting for I/O Pins

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100464	PMU_WAKE_TRIG_NOISECUTEN0	USB_VBUS	RW	[31]	0	Debounce
		USB_VBUS_X	RW	[30]	0	1: eliminates noise
		PMIC_INT	RW	[29]	0	0: does not eliminate noise
		SEN_INT	RW	[28]	0	
		APPGPI5	RW	[27]	0	
		APPGPI4	RW	[26]	0	
		APPGPI3	RW	[25]	0	
		APPGPI2	RW	[24]	0	
		APPGPI1	RW	[23]	0	
		APPGPI0	RW	[22]	0	
		SYSGPI5	RW	[21]	0	
		SYSGPI4	RW	[20]	0	

		SYSGPI3	RW	[19]	0	
		SYSGPI2	RW	[18]	0	
		SYSGPI1	RW	[17]	0	
		SYSGPI0	RW	[16]	0	
		HVDD_DET	RW	[15]	0	
		HIF_UART_RXD	RW	[14]	0	
		HIF_SPI_CS_X	RW	[13]	0	
		HIF_SCL_LOW	RW	[12]	0	
		Reserved	RO	[11:0]	0	Reserved
0x04100474	PMU_WAKE_TRIG_ INTDET0	Reserved	RO	[31]	0	Reserved
		SYSGPI3	RW	[30:28]	0	Selection of the way of detecting events 0: Instant H, 1: Instant L, 2: Level H, 3: Level L, 4: Rising edge, 5: Falling edge, 6: Both Edges, 7: Both Edges (removes the response at the start-up)
		Reserved	RO	[27]	0	Reserved
		SYSGPI2	RW	[26:24]	0	refer to SYSGPI3
		Reserved	RO	[23]	0	Reserved
		SYSGPI1	RW	[22:20]	0	refer to SYSGPI3
		Reserved	RO	[19]	0	Reserved
		SYSGPI0	RW	[18:16]	0	refer to SYSGPI3
		Reserved	RO	[15]	0	Reserved
		HVDD_DET	RW	[14:12]	0	refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		HIF_UART_RXD	RW	[10:8]	0	refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		HIF_SPI_CS_X	RW	[6:4]	0	refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		HIF_SCL_LOW	RW	[2:0]	0	refer to SYSGPI3
0x04100478	PMU_WAKE_TRIG_ INTDET1	Reserved	RW	[31]	0	Reserved
		APPGPI5	RW	[30:28]	0	refer to SYSGPI3
		Reserved	RO	[27]	0	Reserved

		APPGPI4	RW	[26:24]	0	refer to SYSGPI3
		Reserved	RO	[23]	0	Reserved
		APPGPI3	RW	[22:20]	0	refer to SYSGPI3
		Reserved	RO	[19]	0	Reserved
		APPGPI2	RW	[18:16]	0	refer to SYSGPI3
		Reserved	RO	[15]	0	Reserved
		APPGPI1	RW	[14:12]	0	refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		APPGPI0	RW	[10:8]	0	refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		SYSGPI5	RW	[6:4]	0	refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		SYSGPI4	RW	[2:0]	0	refer to SYSGPI3
0x0410047C	PMU_WAKE_TRIG_ INTDET2	Reserved	RO	[31:15]	0	Reserved
		USB_VBUS	RW	[14:12]	0	refer to SYSGPI3
		Reserved	RO	[11]	0	Reserved
		USB_VBUS_X	RW	[10:8]	0	refer to SYSGPI3
		Reserved	RO	[7]	0	Reserved
		PMIC_INT	RW	[6:4]	0	refer to SYSGPI3
		Reserved	RO	[3]	0	Reserved
		SEN_INT	RW	[2:0]	0	refer to SYSGPI3

3.2.4.4.2 Status of Event Detection

When an event is detected, a status register for event detection becomes High and keeps the status even if the event ends. Table General Purpose Input/Output (GPIO)-29 shows status registers for event detection.

Table General Purpose Input/Output (GPIO)-29 Status of Event Detection

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103440	PMU_WAKE_TRIG0	USB_VBUS	RO	[31]	0	Status of Event Detection 1: event is detected 0: event is not detected
		USB_VBUS_X	RO	[30]	0	
		PMIC_INT	RO	[29]	0	
		SEN_INT	RO	[28]	0	
		APPGPI5	RO	[27]	0	
		APPGPI4	RO	[26]	0	
		APPGPI3	RO	[25]	0	
		APPGPI2	RO	[24]	0	
		APPGPI1	RO	[23]	0	
		APPGPI0	RO	[22]	0	
		SYSGPI5	RO	[21]	0	
		SYSGPI4	RO	[20]	0	
		SYSGPI3	RO	[19]	0	
		SYSGPI2	RO	[18]	0	
		SYSGPI1	RO	[17]	0	
		SYSGPI0	RO	[16]	0	
		HVDD_DET	RO	[15]	0	
		HIF_UART_RXD	RO	[14]	0	
		HIF_SPI_CS_X	RO	[13]	0	
		HIF_SCL_LOW	RO	[12]	0	
		HIF_DETECT_I2C_SLAVE	RO	[11]	0	
		INT_SYSIOPSUB	RO	[10]	0	
		INT_GNSS	RO	[9]	0	
		PMU_RTCALMERR	RO	[8]	0	
		PMU_RTCALM2	RO	[7]	0	
		PMU_RTCALM1	RO	[6]	0	
		PMU_RTCALM0	RO	[5]	0	
		SCU_INT3	RO	[4]	0	
		SCU_INT2	RO	[3]	0	

		SCU_INT1	RO	[2]	0	
		SCU_INT0	RO	[1]	0	
		CRG_INT	RO	[0]	0	
0x04103444	PMU_WAKE_TRIG1	Reserved	RO	[31:2]	0	Reserved
		INT_PMIC_I2CM	RO	[1]	0	Status of Event Detection
		UNEXP_PMU	RO	[0]	0	1: event is detected 0: event is not detected

3.2.4.4.3 Clear of Event Detection

Held statuses of Event Detection can be cleared by registers. If you write “1” on the register, clearing process will begin. When the process is completed, the value returns to “0” automatically. You need not write “0”.

Table General Purpose Input/Output (GPIO)-30 shows registers to clear the status of the Event Detections.

Table General Purpose Input/Output (GPIO)-30 Registers to Clear the Status of the Event Detections

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103430	PMU_WAKE_TRIG0_CLR	USB_VBUS	RW	[31]	0	Held statuses of Event Detection can be cleared by writing “1”.
		USB_VBUS_X	RW	[30]	0	
		PMIC_INT	RW	[29]	0	
		SEN_INT	RW	[28]	0	
		APPGPI5	RW	[27]	0	
		APPGPI4	RW	[26]	0	
		APPGPI3	RW	[25]	0	
		APPGPI2	RW	[24]	0	
		APPGPI1	RW	[23]	0	
		APPGPI0	RW	[22]	0	
		SYSGPI5	RW	[21]	0	
		SYSGPI4	RW	[20]	0	
		SYSGPI3	RW	[19]	0	
		SYSGPI2	RW	[18]	0	
		SYSGPI1	RW	[17]	0	
		SYSGPI0	RW	[16]	0	
		HVDD_DET	RW	[15]	0	
		HIF_UART_RXD	RW	[14]	0	
		HIF_SPI_CS_X	RW	[13]	0	
		HIF_SCL_LOW	RW	[12]	0	
		HIF_DETECT_I2C_SLAVE	RW	[11]	0	

3.2.4.4.4 Flow of Controlling Event Detection when used as Interrupt

[illegible]

Flow of Setting Event Detection

– 108/1010 –

interrupts INT_EN*, refer to 3.3.2 (Chapter of Interrupt).

1. Mask an interrupt.

INT_EN0.EXDEVICE[0] = 0

2. Set the Event Detection (Pin Multiplexer, I/O pin selection, and way of detecting events).
3. Clear status register of Event Detection (to avoid errors caused by the result of the previous event detection).

PMU_WAKE_TRIG0_CLR.SYSGPIO = 1

4. Wait for the completion of clearing the status register of Event Detection.

Confirm that **PMU_WAKE_TRIG0_CLR.SYSGPIO = 0**.

5. Cancel interrupt masking.

INT_EN0.EXDEVICE = 1

Flow of Clearing Event Detection

For example, the flow of clearing an interrupt (EXDEVICE[0]) is described below.

1. Detect an event detection as an interrupt.

2. Mask an interrupt.

INT_EN0.EXDEVICE[0] = 0

3. Clear the status register of Event Detection.

PMU_WAKE_TRIG0_CLR.SYSGPIO = 1

4. Wait for the completion of clearing the status register of Event Detection.

Confirm that **PMU_WAKE_TRIG0_CLR.SYSGPIO** equals 0.

5. Cancel interrupt masking (only when you want to detect an interrupt again)

INT_EN0.EXDEVICE[0] = 1

Restriction on Clearing Events

Clearing process to clear a held event is performed when 1 is set on any bit of PMU_WAKE_TRIG0_CLR. You cannot start a new clearing while the former one is still in process. That is, if you set 1 on other bit of PMU_WAKE_TRIG0_CLR while the former clearing is still in process, you must wait for the new clearing until the former one ends. However, if you set 1 on multiple bits at a time, multiple clearing processing can be performed in parallel.

For example, if you set 1 on PMU_WAKE_TRIG0_CLR and then set 2 or 3 on it, clearing processing of SCU_INT0 cannot start until clearing process of CRG_INT ends.

If you set 3 on PMU_WAKE_TRIG0_CLR, clearing processing of both CRG_INT and SCU_INT0 can be performed in parallel.

Time Interval for a Signal to be Able to Detect an Event Again

Once a signal from I/O pin (external signal) is received to detect an event, the same one from I/O pin will ignore further events until the detected event is cleared. Table General Purpose Input/Output (GPIO)-31 shows time intervals from event detection to the next event detection through the flow of clearing the result of event detection.

Figure General Purpose Input/Output (GPIO)-24 shows the timing diagram.

(A) in the table means the time from when an external signal is asserted to when an event detection is held. The time depends on debounce setting. (B) means the time from when the clearing of event detection is executed to when the clearing is completed.

Table General Purpose Input/Output (GPIO)-31 Time Interval for a Signal to be Able to Detect an Event Again

(1*)

Way of detecting events PMU_WAKE_TRI G_INTDET*	Debounce PMU_WAKE_TRI G_NOISECUTEN 0	(A) Time of Detecting an Event (Cycle of RTC Clock)	(B) Time of Clearing Event Detection (Cycle of RTC Clock)	(A) + (B) Time Interval between Event Detections again (Cycle of RTC Clock)
0, 1: Instant Detection	Don't care (constantly without elimination)	2 ~ 3	7 ~ 8	10 ~ 11
4 - 7: Edge Detection	0: No	2 ~ 3	7 ~ 8	10 ~ 11
	1: Yes	4 ~ 5	7 ~ 8	12 ~ 13

(1*) The time intervals in the table are those which are assumed when the following conditions are met.

- After an interrupt is detected, SYSCPU or DSP instantly masks the interrupt and clears the event.
- The clock frequency of one of SYSCPU or DSP that performs the processing described in the above condition must be adequately higher than that of RTC Clock. This restriction does not apply to the other that does not perform the processing.
- When you execute the clearing of the event detection of (B), no clearing of other event detection is in process.

(If you start a new clearing process when the former clearing of event detection is still in process, the latter process must wait until the present process is completed. For this reason, the period of (B) extends.)

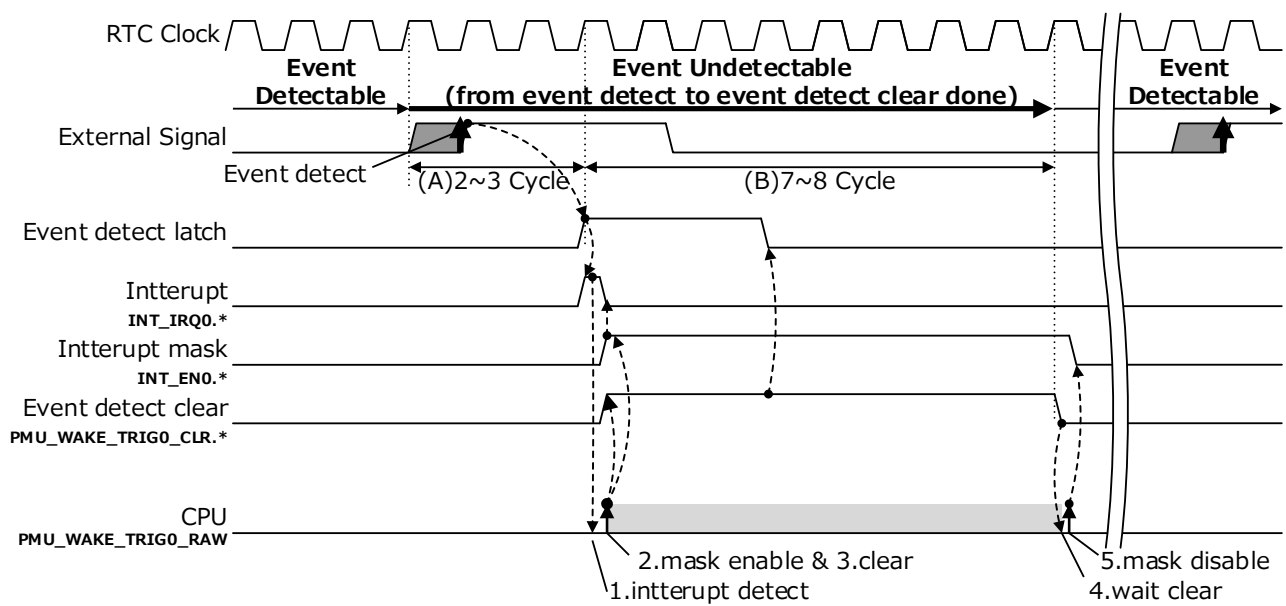


Figure General Purpose Input/Output (GPIO)-24 Time Interval for a Signal to be able to Detect an Event Again
(PMU_WAKE_TRIG_NOISECUTEN0:0)

3.3 Interrupt

3.3.1 Overview and Features

The LSI has individual interrupt controllers for the SYSIOP, GNSS, and APP.

The 128 bit interrupt factors are connected to the CPUs of each SYSIOP, GNSS, and APP.

Interrupt requests are divided into two main categories: one is internal interrupt generated from each CPU core or Peripheral, and another is external interrupt from I/O.

As external interrupts, signals from I/O can be used without any change, and results of event detection by GPIO can be used as well.

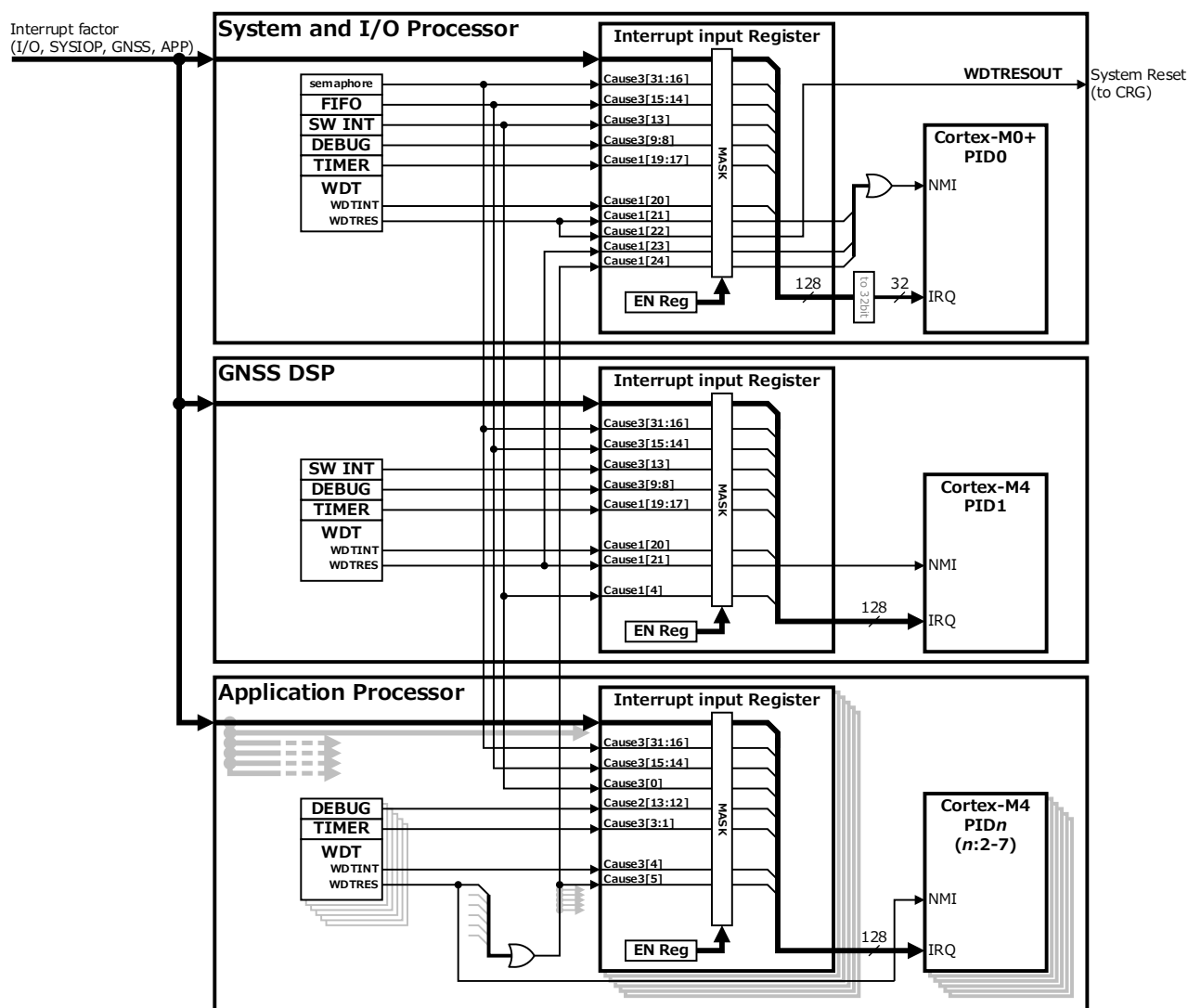


Figure Interrupt-25 Interrupt Connection Diagram

Interrupt request from Watchdog Timer, WDTINT (bit[20]) is connected to IRQ of Processor 0, and reset signal from Watchdog Timer, WDTRES (bit[21]) is connected to Non-Maskable Interrupt (NMI) of Processor 0 (PID0 in Figure Interrupt-25).

WDTRES (bit[23]) of GNSS and WDTRES (bit[23]) of APP are ORed with WDTINT(bit[20]), and the result is provided to NMI of Processor 0. In the meantime, WDTRESOUT (bit[22]) is not connected to IRQ or NMI of Processor 0, but connected to System Reset of CRG, therefore, System Reset can be performed regardless of the status of Processor 0.

3.3.2 Register Descriptions

3.3.2.1 Interrupt Registers of Application Processor

Table Interrupt-32 shows list of interrupt registers of Application Processor.

Table Interrupt-32 List of Interrupt Registers of Application Processor

Address	Register	Type	Initial	Description
0xE0045000	INT_CAUSE0	RO	-	Interrupt factor indicates the status of the interrupt The initial value of the register depends on that of connected block.
0xE0045004	INT_CAUSE1	RO	-	
0xE0045008	INT_CAUSE2	RO	-	
0xE004500C	INT_CAUSE3	RO	-	
0xE0045010	INT_EN0	RW	0x00000000	Interrupt enable When bit value is "1", interrupt is requested to processor (enabled), and when bit value is "0", interrupt is not requested (disabled).
0xE0045014	INT_EN1	RW	0x00000000	
0xE0045018	INT_EN2	RW	0x00000000	
0xE004501C	INT_EN3	RW	0x00000000	
0xE0045020	INT_INV0	RW	0x00000000	Inverted polarity Writing "1" enables to invert the polarity of the interrupt of the corresponding bit.
0xE0045024	INT_INV1	RW	0x00000000	
0xE0045028	INT_INV2	RW	0x00000000	
0xE004502C	INT_INV3	RW	0x00000000	
0xE0045030	INT_IRQ0	RO	0x00000000	Interruption request means ANDed value between interrupt factor (INT_CAUSE) and interrupt enable (INT_EN), and indicates the status of signal actually provided to processor
0xE0045034	INT_IRQ1	RO	0x00000000	
0xE0045038	INT_IRQ2	RO	0x00000000	
0xE004503C	INT_IRQ3	RO	0x00000000	

Table Interrupt-33 Interrupt Factor Registers of Application Processor

Address	Register	Bit Field	Type	Bit	Initial	Description
0xE0045000	INT_CAUSE0	EXDEVICE	RO	[31:20]	-	Interrupt request from external device (from GPIO)

		SCU	RO	[19:16]	-	Interrupt request from SCU
		HOSTIFC	RO	[15:13]	-	Interrupt request from Host I/F
		UART	RO	[12]	-	Interrupt request from UART0
		UARTDBG	RO	[11]	-	Interrupt request from UART1
		RTC_INT	RO	[10]	-	ORed value between the following: - Interrupt request from RTC1_Misc - Interrupt request from RTC0_Misc
		RTC1A2	RO	[9]	-	Interrupt request from RTC1 OAlarm2
		RTC1A1	RO	[8]	-	Interrupt request from RTC1 OAlarm0
		RTC1A0	RO	[7]	-	Interrupt request from RTC1 OAlarm0
		RTC0A2	RO	[6]	-	Interrupt request from RTC0 OAlarm2
		RTC0A1	RO	[5]	-	Interrupt request from RTC0 OAlarm1
		RTC0A0	RO	[4]	-	Interrupt request from RTC0 OAlarm0
		Reserved	RO	[3]	-	Reserved
		HVDD	RO	[2]	-	Interrupt request from VDD_IO_HOST status
		CRG	RO	[1]	-	Interrupt request from CRG
		PMU	RO	[0]	-	Interrupt request from PMU
0xE0045004	INT_CAUSE1	SDMAC	RO	[31:0]	-	Interrupt request from SDMAC
0xE0045008	INT_CAUSE2	SPH	RO	[31:16]	-	Interrupt request from semaphore regarding communication between CPUs
		FIFOFROM	RO	[15]	-	Interrupt request from receive FIFO regarding communication between CPUs
		FIFOTO	RO	[14]	-	Interrupt request from transmit FIFO regarding communication between CPUs
		DEBUG	RO	[13:12]	-	Interrupt request from debug block (APP)
		I2CMCOM	RO	[11]	-	Interrupt request from I2C2
		SPIMCOM	RO	[10]	-	Interrupt request from SPI0
		USBVBUSN	RO	[9]	-	Inverted polarity of interrupt request from external device (USB_VBUSINT)
		USBVBUS	RO	[8]	-	Interrupt request from external device (USB_VBUSINT)
		CRYPTO_CLEFIA	RO	[7:6]	-	Interrupt request from Crypto (Clefia)
		SYSUBDMAC	RO	[5:4]	-	Interrupt request from SYSUBDMAC
		SYDMAC	RO	[3:2]	-	Interrupt request from SYDMAC
0xE004500C	INT_CAUSE3	HDMAC	RO	[1:0]	-	Interrupt request from HDMAC
		PMIC_INT	RO	[31]	-	Interrupt request from external device (PMIC)

		SFC	RO	[30]	-	Interrupt request from SPI Flash controller
		GNSSOR	RO	[29]	-	ORed value of GNSS Receiver interrupts
		Reserved	RO	[28]	-	Reserved
		CRYPTO_AES_MST	RO	[27:26]	-	Interrupt request from Crypto (AES) BusMaster
		CRYPTO_AES_CORE	RO	[25:24]	-	Interrupt request from Crypto (AES) AES
		ADMAC	RO	[23:22]	-	Interrupt request from ADMAC
		PERUSB	RO	[21:20]	-	Interrupt request from USB
		PERSDIF	RO	[19]	-	Interrupt request from SDIO
		PEREMMC	RO	[18]	-	Interrupt request from eMMC
		IMGSSP	RO	[17]	-	Interrupt request from SPI4
		IMGVSYNC	RO	[16]	-	Interrupt request from Imaging vsync
		IMGUART	RO	[15]	-	Interrupt request from UART2
		IMGDMAC	RO	[14]	-	Interrupt request from IDMAC
		IMGWSSP	RO	[13]	-	Interrupt request from SPI5
		IMGCIS	RO	[12]	-	Interrupt request from CIS I/F
		IMGROT	RO	[11]	-	Interrupt request from Imaging rotation
		IMG2D	RO	[10]	-	Interrupt request from 2D Graphics
		AUDCODEC	RO	[9]	-	Interrupt request from AudioDSP
		AUDI2S1	RO	[8]	-	Interrupt request from I2S1
		AUDI2S0	RO	[7]	-	Interrupt request from I2S0
		AUDMIC	RO	[6]	-	Interrupt request from PDM
		WDTRES	RO	[5]	-	Interrupt request from Watchdog RES (APP)
		WDTINT	RO	[4]	-	Interrupt request from Watchdog Timer (APP)
		TIMER	RO	[3:1]	-	Interrupt request from TIMER (APP)
		SWINT	RO	[0]	-	Software interrupt request (APP)

3.4 PMU (Power Management Unit)

3.4.1 Features and Overview

The Power Management Unit (referred to as “PMU” hereinafter) is the block that performs overall power supply control of the CXD5602.

The CXD5602 has a large power domain, which is divided into 11 domains. It performs ON control of necessary power domains only, while performing OFF control of the unnecessary ones, thereby reducing the power consumption.

The 11 power domains comprise a layer structure as shown in Figure PMU (Power Management Unit)-26. The lower-layer power domains cannot be turned ON when the upper-layer power supplies are OFF. Furthermore, PWD_GNSS can be turned ON only when both PWD_GNSS_ITP and PWD_SYSIOP are ON.

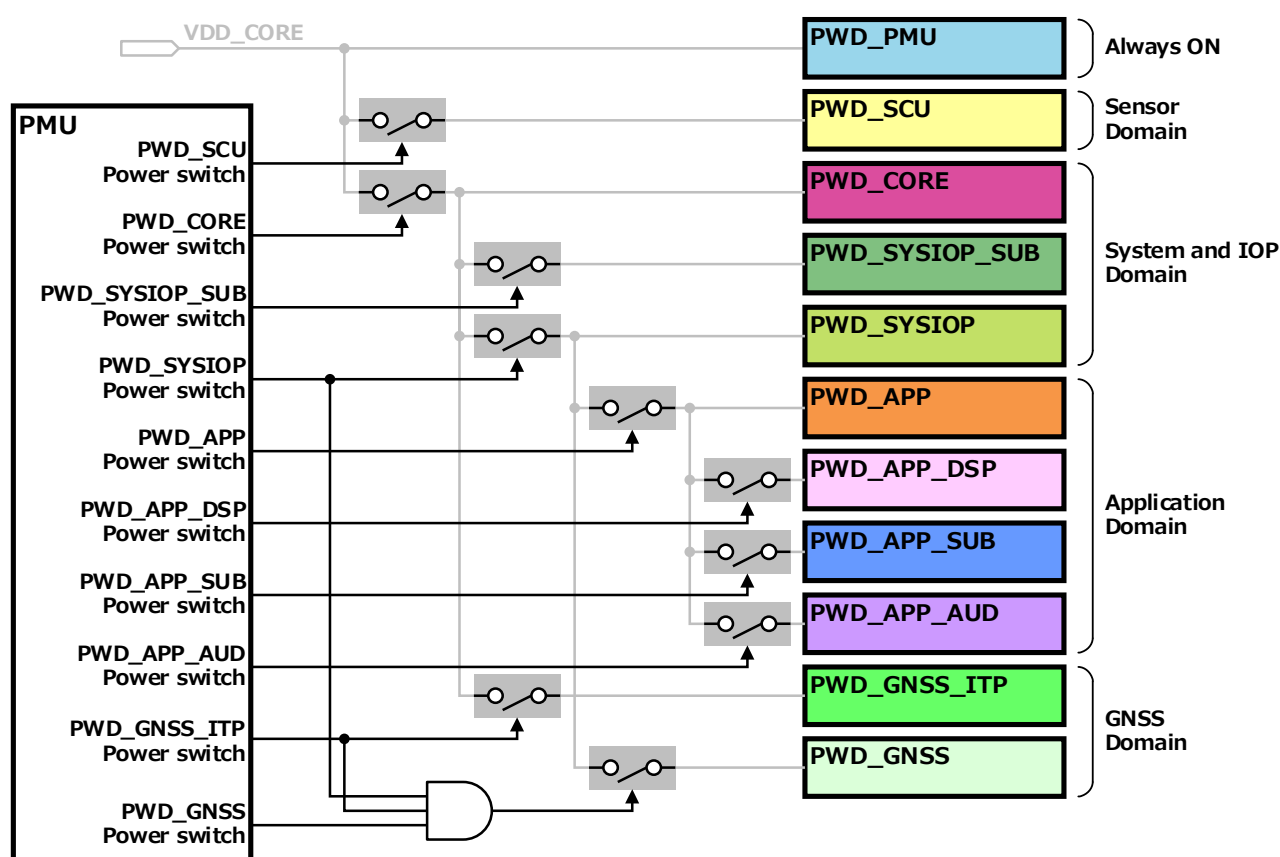


Figure PMU (Power Management Unit)-26 PMU and the Power Domain Layers

3.4.1.1 Individual Power Supply Control within the Power Domains

The SRAM or analog circuits such as the ADC within the power domains enable individual power supply control.

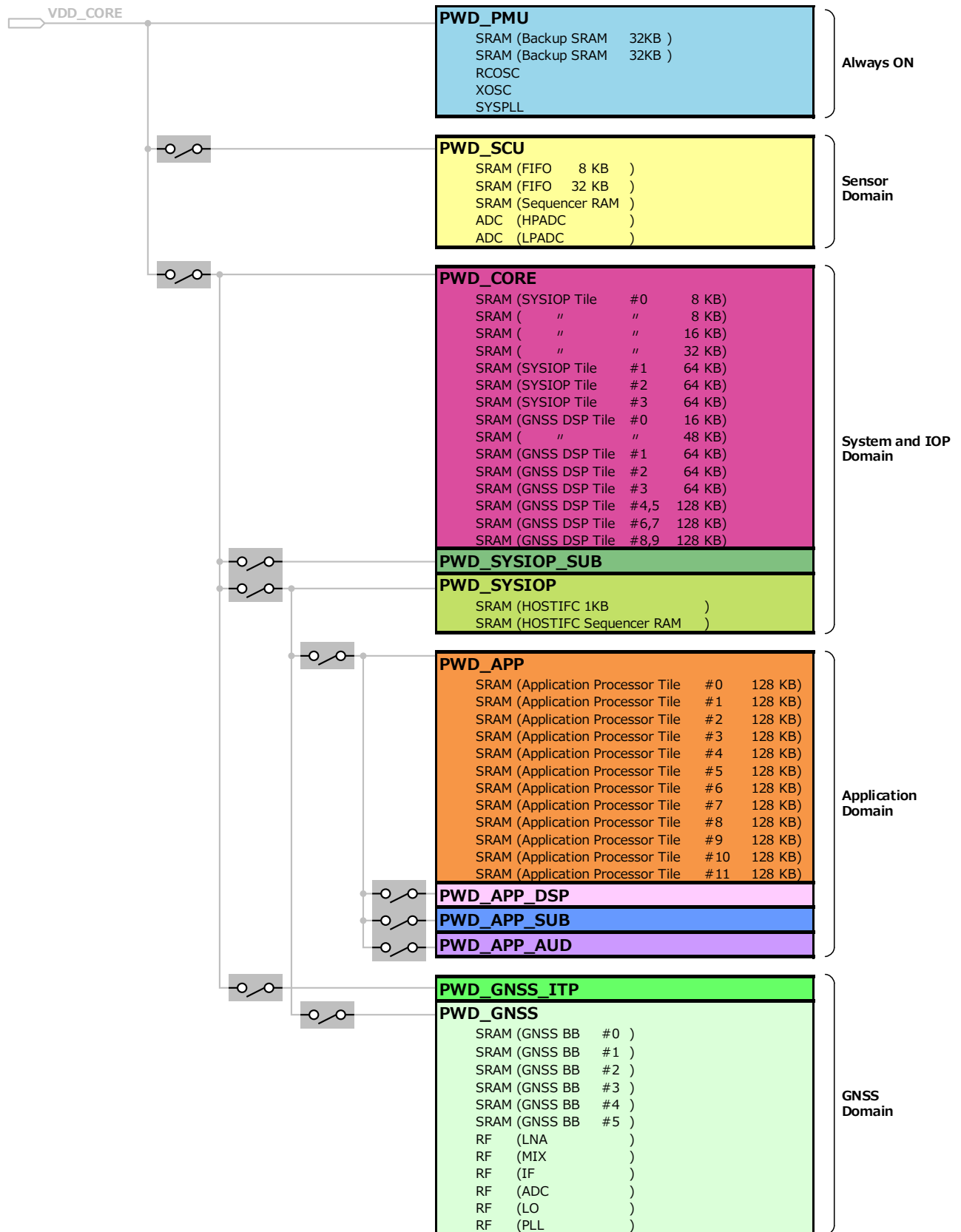


Figure PMU (Power Management Unit)-27 Individual Power Supply Control within the Power Domains

Using the PWD_APP of Figure PMU (Power Management Unit)-27 as an example, Figure PMU (Power Management Unit)-28 explains how individual power supply control is performed within the power domains. The PWD_APP has a total of 1.5 Mbytes of SRAM as main memory for the Application Processor. It comprises 12 logic tiles in 128 Kbyte units, and each one can control the power supply individually. The power supply of the main memory's upper layer is PWD_APP. When PWD_APP is ON, the main memory for the Application Processor can be turned ON.

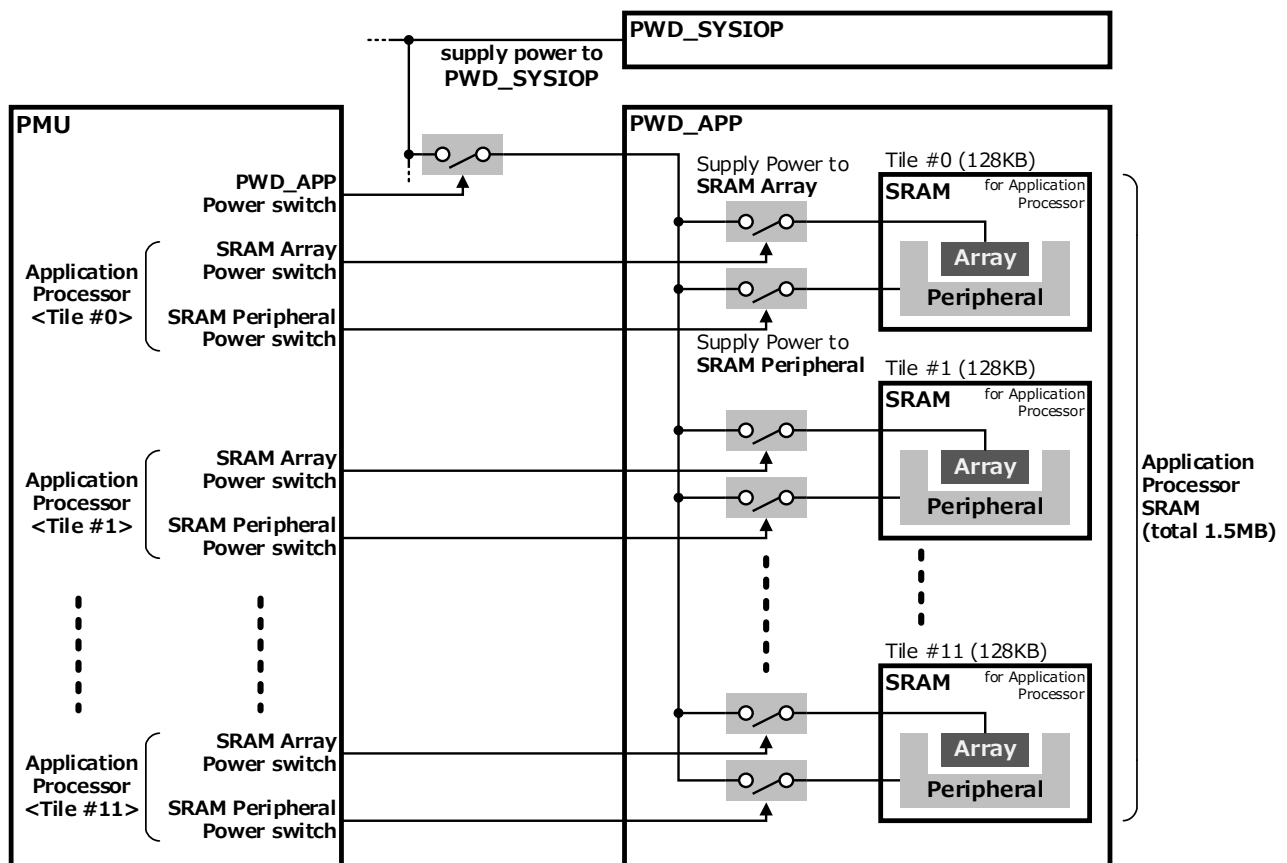


Figure PMU (Power Management Unit)-28 Power Supply Control within the Power Domain (PWD_APP Main Memory)

There are three modes for power supply control of the SRAMs.

- On mode
 - The power supply of the SRAM memory array and peripheral circuitry are ON, and R/W access to the SRAM is possible.
- Retention mode
 - A mode in which only the power supply of the SRAM memory array is ON, and the power supply of the peripheral circuitry is turned OFF. In Retention mode, the SRAM cannot be accessed, but the data within the SRAM is retained. By turning on (ON mode) the power supply of the peripheral circuitry of

the SRAM once again, the data within the SRAM can be accessed. Retention mode enables reduction of the leakage power and recovery of high speed of peripheral circuitry for SRAMs that are temporarily not used.

- ShutDown mode
 - A mode that turns OFF both the power supplies of the SRAM memory array and peripheral circuitry. This mode consumes less power than the Retention mode, but the data in the SRAM is not retained.

3.4.1.2 Power Supply States

The following describes the main power supply states.

Table PMU (Power Management Unit)-34 Power Supply States

	Power supply states	Description
1	Power Off	Both the CXD5602 (referred to as “the LSI” hereinafter) and the CXD5247 are OFF.
2	Deep Sleep	The LSI is OFF and the CXD5247 is ON. In this state, the RTC of the CXD5247 is counting, and time information can be obtained from the CXD5247 after the LSI is started.
3	Reset	In this state, the LSI and CXD5247 are both ON, and the LSI is being reset.
4	Normal	The LSI and CXD5247 are both ON, and the System Control (PWD_SYSIOP) turns ON, enabling power supply control of each Domain.

The state begins from “Power OFF,” and after the CXD5247 starts, power is supplied to the LSI and a reset is enabled, changing the state to “Reset.” After releasing the reset of the LSI, the System Control of the System and IOP Domain is automatically started, and the state enters “Normal.” In the “Normal” state, the power supply control of each feature’s Domain can be controlled. By issuing the Deep Sleep command to the CXD5247, the state changes to “Deep Sleep.” When events of the CXD5247 occur, such as the timer or interrupts, the state changes to “Reset” and then to “Normal.”

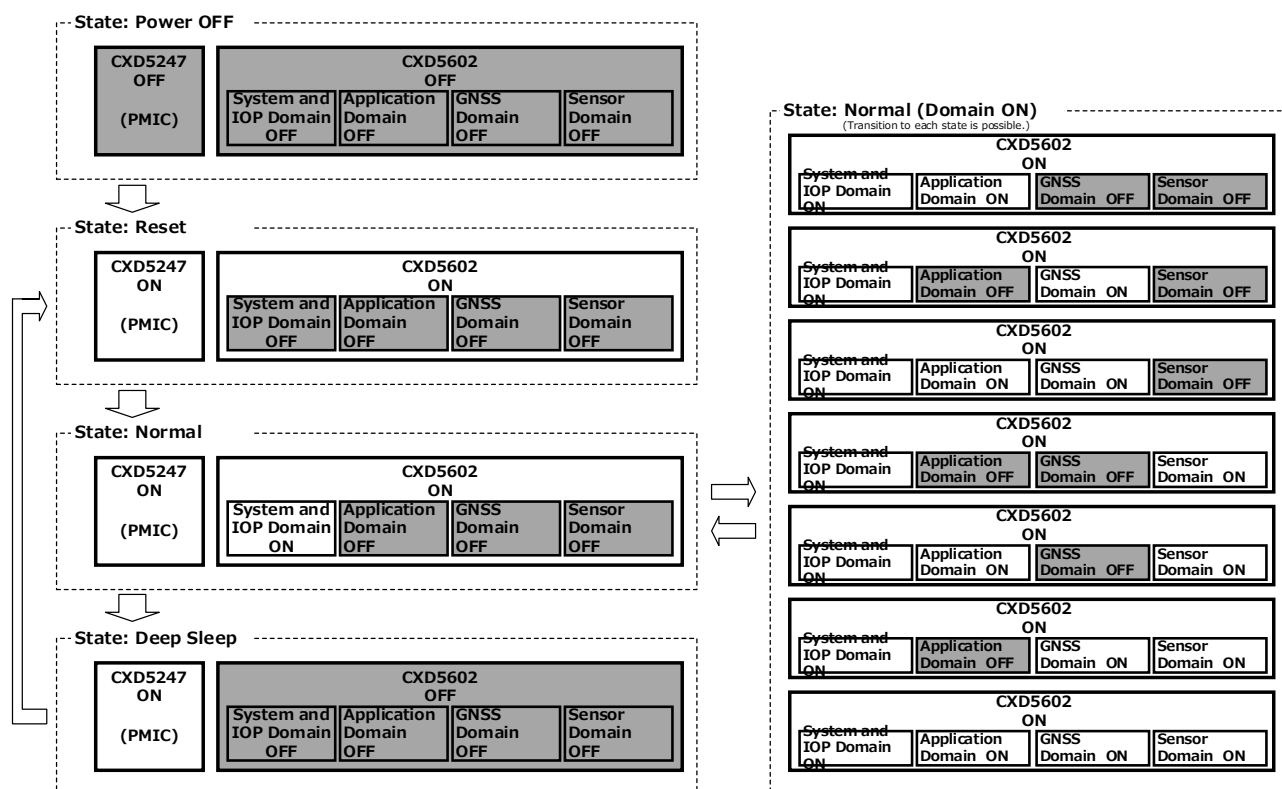


Figure PMU (Power Management Unit)-29 Changes of Power Supply States

Details of the Power Supply Settings of the Power Supply States

The following table shows the relation between “Reset” states of the power supply, and the setting of the power supply immediately after the state changes from “Reset” to “Normal” state.

Table PMU (Power Management Unit)-35 The Setting of the Power Supply in “Reset” State and After Changing to “Normal” State

Domain name	Power name	“Reset” state	Immediately after changing from “Reset” to “Normal” state
Always ON	PWD_PMU	ON	ON
	SRAM (Backup SRAM 32 KByte)	ON	ON
	SRAM (Backup SRAM 32 KByte)	ON	ON
	RCOSC	ON	ON
	XOSC	OFF	OFF
	SYSPLL	OFF	OFF
Sensor Domain	PWD_SCU	OFF	OFF
	SRAM (FIFO 32 KByte)	OFF	OFF
	SRAM (FIFO 8 KByte)	OFF	OFF
	SRAM (Sequencer RAM)	OFF	OFF

	ADC (HPADC)	OFF	OFF
	ADC (LPADC)	OFF	OFF
System and IOP Domain	PWD_CORE	OFF	ON
	SRAM (SYSIOP Tile #0 8 KByte)	OFF	ON
	SRAM (SYSIOP Tile #0 8 KByte)	OFF	ON
	SRAM (SYSIOP Tile #0 16 KByte)	OFF	ON
	SRAM (SYSIOP Tile #0 32 KByte)	OFF	ON
	SRAM (SYSIOP Tile #1 64 KByte)	OFF	ON
	SRAM (SYSIOP Tile #2 64 KByte)	OFF	ON
	SRAM (SYSIOP Tile #3 64 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #0 16 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #0 48 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #1 64 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #2 64 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #3 64 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #4,5 128 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #6,7 128 KByte)	OFF	ON
	SRAM (GNSS DSP Tile #8,9 128 KByte)	OFF	ON
	PWD_SYSIOP_SUB	OFF	ON
	PWD_SYSIOP	OFF	ON
	SRAM (HOSTIFC 1KByte)	OFF	ON
	SRAM (HOSTIFC Sequencer RAM)	OFF	ON
Application Domain	PWD_APP	OFF	OFF
	SRAM (Application Processor Tile #0 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #1 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #2 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #3 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #4 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #5 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #6 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #7 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #8 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #9 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #10 128 KByte)	OFF	OFF
	SRAM (Application Processor Tile #11 128 KByte)	OFF	OFF
	PWD_APP_DSP	OFF	OFF
	PWD_APP_SUB	OFF	OFF
	PWD_APP_AUD	OFF	OFF

GNSS Domain	PWD_GNSS_ITP	OFF	OFF
	PWD_GNSS	OFF	OFF
	SRAM (GNSS BB#0)	OFF	OFF
	SRAM (GNSS BB#1)	OFF	OFF
	SRAM (GNSS BB#2)	OFF	OFF
	SRAM (GNSS BB#3)	OFF	OFF
	SRAM (GNSS BB#4)	OFF	OFF
	SRAM (GNSS BB#5)	OFF	OFF
	RF (LNA)	OFF	OFF
	RF (MIX)	OFF	OFF
	RF (IF)	OFF	OFF
	RF (ADC)	OFF	OFF
	RF (LO)	OFF	OFF
	RF (PLL)	OFF	OFF

3.4.1.3 Block Diagram

Figure PMU (Power Management Unit)-30 shows the block diagram of the PMU, which is mainly comprised of three blocks.

- AHB IF

This is the control register of the PMU. After setting the power supply control of the power domain, analog circuit, and SRAM, setting the power supply control request **PMU_PW_CTL** starts the power supply control. The status of the power switch can be confirmed by reading the control register.

- Check Register Value

In response to the power supply control request, this checks whether or not there are errors in the power supply control register settings (**PWD_CTL**, ***_RAMMODE_SEL**, **ANA_PW_CTL**). Power supply control is executed only when the register settings are correct, and not performed when they are incorrect. For example, when a power supply of the upper layer (**PWD_APP**) is OFF, and a power supply of the lower layer (**PWD_APP_DSP**) receives a setting request to turn it ON, this is judged as an incorrect setting and power supply control is not performed.

- Power Control Sequencer

This sequencer identifies the upper and lower layers of the power supply and automatically controls the order of the power supply switch control. When the power supply is controlled from OFF to ON, the operation begins from the power supply in the upper layer. Conversely, when the power supply is controlled from ON to OFF, the operation begins from the power supply in the lower layer. In this way, using only 1 power supply control request, power supply control of the power supply in the upper layer (**PWD_APP**) and power supply control of the power supply in the lower layer (**PWD_APP_DSP**) can be done together. For example, when issuing a power supply control request to turn ON both the upper

layer and lower layer, the Power Control Sequencer first turns ON the power supply of the upper layer (PWD_APP) and then turns ON the power supply of the lower layer (PWD_APP_DSP). The CPU can recognize the completion of power supply control by the interrupt.

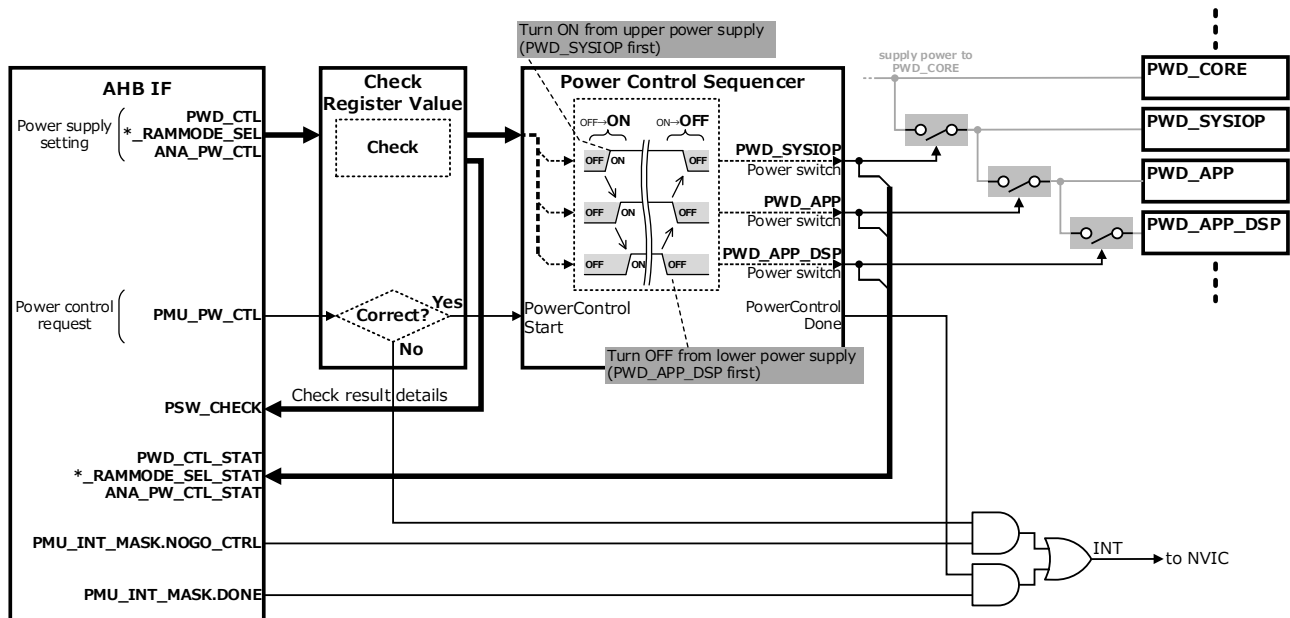


Figure PMU (Power Management Unit)-30 Overall Block Diagram of the PMU

3.4.1.4 Clock and Reset

Clock

Figure PMU (Power Management Unit)-31 shows a system diagram of the PMU's clock.

- **AHB IF**
Operates using the ck_ahb_gear clock which is synchronized with the System and I/O Processor.
- **Check Register Value, Power Control Sequencer**
Operates using the RCOSC or RTC_CLK_IN. When power is supplied, the RCOSC turns ON and the initial value of the control register (RORTC_STAT_CLK_SEL2) selects RCOSC as the operation clock of the PMU. Before turning OFF the power switch of the RCOSC, make sure to switch the operation clock of the PMU to the RTC_CLK_IN.

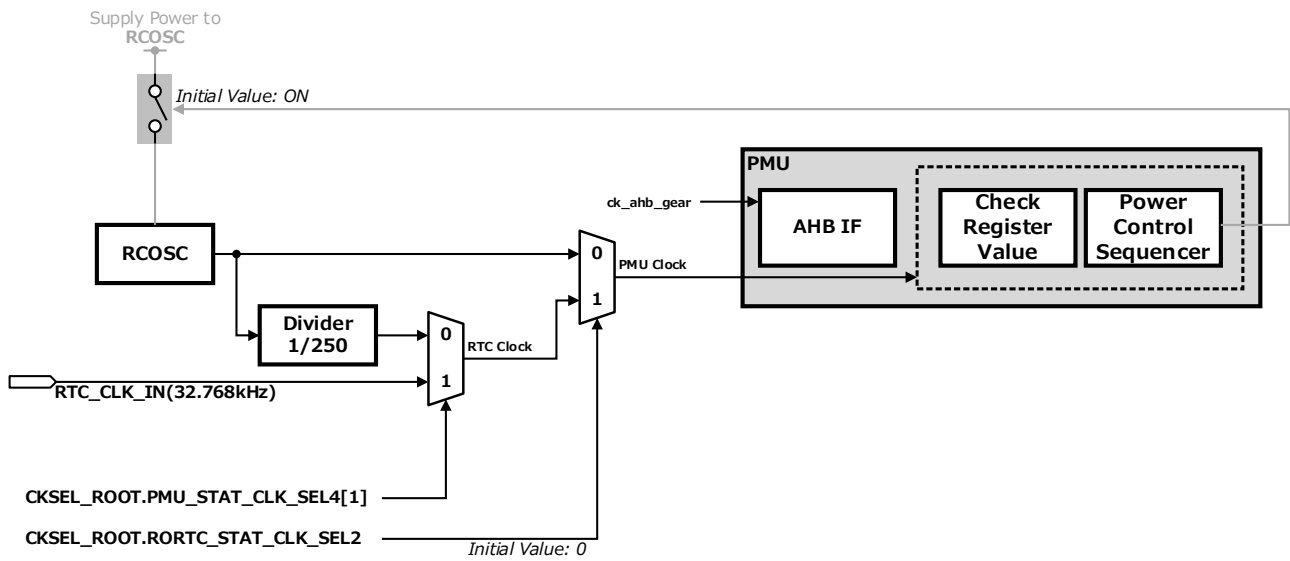


Figure PMU (Power Management Unit)-31 PMU Clock System

Reset

The PMU is reset by full reset of the CXD5602 (external reset (RST_X) or RCOSC POR or WDT reset), by automatic release. Reset cannot be applied to the PMU alone.

3.4.2 Register List

Table PMU (Power Management Unit)-36 shows a list of registers related to each feature of the PMU.

Table PMU (Power Management Unit)-36 PMU Register List

Address	Register Name	Type	Description	Initial Value
0x04100000	PWD_CTL	RW	Power supply control setting (Power domain)	0x00000000
0x04100004	ANA_PW_CTL	RW	Power supply control setting (Analog circuit)	0x00000001
0x04100008	ANA_EN_CTL	RW	XOSC control setting	0x0F1901F7
0x04100010	SYSCPU_RAMMODE_SEL	RW	Power supply control setting (SRAM for System and I/O Processor)	0x00003FFF
0x04100014	Reserved	RO	Reserved	0x00000000
0x04100018	TOP_SCU_RAMMODE_SEL	RW	Power supply control setting (SRAM for SCU)	0x000F0000
0x0410001C	HOSTIFC_RAMMODE_SEL	RW	Power supply control setting (SRAM for HOSTIFC)	0x0000000F
0x04100020 0x0410002C	Reserved	RW	Reserved	-
0x04100030	PMU_PW_CTL	WO	Power supply control request	0x00000000
0x04100040	PMU_INT_STAT	RO	Interrupt status	0x00000000
0x04100044	PMU_RAW_INT_STAT	RO	Pre-masked interrupt status	0x00000000
0x04100048	PMU_INT_CLR	WO	Interrupt clear	0x00000000
0x0410004C	PMU_INT_MASK	RW	Interrupt mask	0x00000F10
0x04100070 0x04100104	Reserved	RW	Reserved	-
0x04100200	PWD_STAT	RO	Power supply status (Power domain)	0x00000000
0x04100204	Reserved	RO	Reserved	0x00000000
0x04100208	ANA_PW_STAT	RO	Power supply status (Analog circuit)	0x00000000
0x0410020C	SYSCPU_RAMMODE_STAT	RO	Power supply status (SRAM for System and I/O Processor)	0x00003FFF
0x04100214	TOP_SCU_RAMMODE_STAT	RO	Power supply status (SRAM for SCU)	0x00000F00
0x04100218	HOSTIFC_RAMMODE_STAT	RO	Power supply status (SRAM for HOSTIFC)	0x00000000
0x0410021C	PMU_HW_STAT	RO	Power supply control status	0x3F3F0000
0x04100400 0x04100450	Reserved	RO	Reserved	-
0x04100C00	GNSSDSP_RAMMODE_SEL	RW	Power supply setting (SRAM for GNSS DSP)	0x0000FFFF

0x04100C40	GNSSDSP_RAMMODE_STAT	RO	Power supply status (SRAM for GNSS DSP)	0x0000FFFF
0x04103000	PSW_CHECK	RO	Power supply setting check	0x00000000
0x04103004 0x04103034	Reserved	RW	Reserved	-
0x04103C00	GNSS_RAMMODE_SEL	RW	Power supply setting (SRAM for GNSS)	0x00000000
0x04103C30	GNSS_RAMMODE_STAT	RO	Power supply status (SRAM for GNSS)	0x00000000
0x04104400	APPDSP_RAMMODE_SEL0	RW	Power supply setting (SRAM0 for Application Processor)	0x00000000
0x04104404	APPDSP_RAMMODE_SEL1	RW	Power supply setting (SRAM1 for Application Processor)	0x00000000
0x04104420	APPDSP_RAMMODE_STAT0	RO	Power supply status (SRAM0 for Application Processor)	0x00000000
0x04104424	APPDSP_RAMMODE_STAT1	RO	Power supply status (SRAM1 for Application Processor)	0x00000000

3.4.3 Register Descriptions

3.4.3.1 Register Settings

Within the power supply control register (PWD_CTL, *_RAMMODE_SEL, ANA_PW_CTL), there is a Write Enable for each power supply. Power supply control is enabled only for power supplies with Write Enable set to “1”, allowing the control of the desired power supply without performing read-modify-write.

When making the settings for power supply control, make sure to use Word access to simultaneously perform write operations to the bits of Write Enable and each power supply's setting (ON/OFF). Do not use Byte or half word access.

3.4.3.2 Power Supply Control (Power Domain)

Table PMU (Power Management Unit)-37 and Table PMU (Power Management Unit)-38 show the registers related to power supply control of the power domains. For the control method, refer to the control flow described in Section 3.4.4.1.

Table PMU (Power Management Unit)-37 Power Supply Control Settings (Power Domain)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100000	PWD_CTL	WEN	RO	[31]	0	Reserved
			WO	[30]	0	Write Enable (PWD_APP_AUD)
			WO	[29]	0	Write Enable (PWD_GNSS)
			WO	[28]	0	Write Enable (PWD_GNSS_ITP)
			RO	[27]	0	Reserved
			WO	[26]	0	Write Enable (PWD_APP_SUB)
			WO	[25]	0	Write Enable (PWD_APP_DSP)
			WO	[24]	0	Write Enable (PWD_APP)
			RO	[23]	0	Reserved
			WO	[22]	0	Write Enable (PWD_SYSIOP_SUB)
			WO	[21]	0	Write Enable (PWD_SYSIOP)
			WO	[20]	0	Write Enable (PWD_CORE)
			RO	[19:17]	0	Reserved
			WO	[16]	0	Write Enable (PWD_SCU)
		Reserved	RO	[15]	0	Reserved
		PWD_APP_AUD	RW	[14]	0	Power supply control setting 1: ON, 0: OFF
		PWD_GNSS	RW	[13]	0	
		PWD_GNSS_ITP	RW	[12]	0	

		Reserved	RO	[11]	0	Reserved
		PWD_APP_SUB	RW	[10]	0	Power supply control setting 1: ON, 0: OFF
		PWD_APP_DSP	RW	[9]	0	
		PWD_APP	RW	[8]	0	
		Reserved	RO	[7]	0	Reserved
		PWD_SYSIOP_SUB	RW	[6]	1	Power supply control setting 1: ON, 0: OFF
		PWD_SYSIOP	RW	[5]	1	
		PWD_CORE	RW	[4]	1	
		Reserved	RO	[3:1]	0	Reserved
		PWD_SCU	RW	[0]	0	Power supply control setting 1: ON, 0: OFF

Note:

The power supplies that are controlled are only the ones to which “1” has been written to their corresponding Write Enables.

Table PMU (Power Management Unit)-38 Power Supply Status (Power Domain)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100200	PWD_STAT	Reserved	RO	[31:15]	0	Reserved
		PWD_APP_AUD	RO	[14]	0	Power supply status 1: ON, 0: OFF
		PWD_GNSS	RO	[13]	0	
		PWD_GNSS_ITP	RO	[12]	0	
		Reserved	RO	[11]	0	Reserved
		PWD_APP_SUB	RO	[10]	0	Power supply status 1: ON, 0: OFF
		PWD_APP_DSP	RO	[9]	0	
		PWD_APP	RO	[8]	0	
		Reserved	RO	[7]	0	Reserved
		PWD_SYSIOP_SUB	RO	[6]	0	Power supply status 1: ON, 0: OFF
		PWD_SYSIOP	RO	[5]	0	
		PWD_CORE	RO	[4]	0	
		Reserved	RO	[3:1]		Reserved
		PWD_SCU	RO	[0]	0	Power supply status 1: ON, 0: OFF

3.4.3.3 Power Supply Control (SRAM)

Table PMU (Power Management Unit)-39 and Table PMU (Power Management Unit)-40 show the registers related to power supply control of the SRAM. For the power supply control method, refer to the control flow described in Section 3.4.4.1.

Table PMU (Power Management Unit)-39 Power Supply Control Settings (SRAM)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100010	SYSCPU_RAMM ODE_SEL	Reserved	RO	[31]	0	Reserved
		WEN	WO	[30]	0	Write Enable (RAM3_64KB)
				[29]	0	Write Enable (RAM2_64KB)
				[28]	0	Write Enable (RAM1_64KB)
				[27]	0	Write Enable (RAM0_32KB)
				[26]	0	Write Enable (RAM0_16KB)
				[25]	0	Write Enable (RAM0_8KB_1)
				[24]	0	Write Enable (RAM0_8KB_0)
		Reserved	RO	[23:14]	0	Reserved
		RAM3_64KB	RW	[13:12]	2'b11	Power supply control settings 2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		RAM2_64KB	RW	[11:10]	2'b11	
		RAM1_64KB	RW	[9:8]	2'b11	
		RAM0_32KB	RW	[7:6]	2'b11	
		RAM0_16KB	RW	[5:4]	2'b11	
		RAM0_8KB_1	RW	[3:2]	2'b11	
		RAM0_8KB_0	RW	[1:0]	2'b11	
0x04100018	TOP_SCU_RAM MODE_SEL	Reserved	RO	[31:20]	0	Reserved
		WEN	WO	[25]	0	Write Enable (BKMEM_MODESEL1)
			WO	[24]	0	Write Enable (BKMEM_MODESEL0)
		Reserved	RO	[23:20]	0	Reserved
		BKRAM_MODESEL1	RW	[19:18]	2'b11	Power supply control settings 2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		BKRAM_MODESEL0	RW	[17:16]	2'b11	
		Reserved	RO	[15:13]	0	Reserved
		WEN	WO	[12]	0	Write Enable (SCUSEQ)
		Reserved	RO	[11:10]	0	Reserved
		WEN	WO	[9]	0	Write Enable (SCU_FIFO1)
				[8]	0	Write Enable (SCU_FIFO0)

		Reserved	RO	[7:6]	0	Reserved
		SCUSEQ	RW	[5:4]	2'b00	Power supply control settings
		SCU_FIFO1	RW	[3:2]	2'b00	2'b11: On mode
		SCU_FIFO0	RW	[1:0]	2'b00	2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
0x0410001C	HOSTIFC_RAM MODE_SEL	Reserved	RO	[31:4]	0	Reserved
		WEN	WO	[25]	0	Write Enable (SEQ)
				[24]	0	Write Enable (RAM_1KB)
		Reserved	RO	[23:4]	0	Reserved
		SEQ	RW	[3:2]	2'b11	Power supply control settings
		RAM_1KB	RW	[1:0]	2'b11	2'b11: On mode
		RCOSC	RW	[0]	0	2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
0x04100C00	GNSSDSP_RAM MODE_SEL	WEN	WO	[31]	0	Write Enable (RAM89_128KB)
				[30]	0	Write Enable (RAM67_128KB)
				[29]	0	Write Enable (RAM45_128KB)
				[28]	0	Write Enable (RAM3_64KB)
				[27]	0	Write Enable (RAM2_64KB)
				[26]	0	Write Enable (RAM1_64KB)
				[25]	0	Write Enable (RAM0_48KB)
				[24]	0	Write Enable (RAM0_16KB)
		Reserved	RO	[23:16]	0	Reserved
		RAM89_128KB	RW	[15:14]	2'b11	Power supply control settings
		RAM67_128KB	RW	[13:12]	2'b11	2'b11: On mode
		RAM45_128KB	RW	[11:10]	2'b11	2'b01: Retention mode
		RAM3_64KB	RW	[9:8]	2'b11	2'b00: ShutDown mode
		RAM2_64KB	RW	[7:6]	2'b11	2'b10: Prohibited setting
		RAM1_64KB	RW	[5:4]	2'b11	
		RAM0_48KB	RW	[3:2]	2'b11	
		RAM0_16KB	RW	[1:0]	2'b11	
0x04104424	APPDSP_RAMM ODE_SEL0	Reserved	RO	[31:30]	0	Reserved
		WEN	WO	[29]	0	Write Enable (RAM5)
				[28]	0	Write Enable (RAM4)
				[27]	0	Write Enable (RAM3)
				[26]	0	Write Enable (RAM2)
				[25]	0	Write Enable (RAM1)

				[24]	0	Write Enable (RAM0)
		Reserved	RO	[23:12]	0	Reserved
		RAM5	RW	[11:10]	2'b00	Power supply control settings 2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		RAM4	RW	[9:8]	2'b00	
		RAM3	RW	[7:6]	2'b00	
		RAM2	RW	[5:4]	2'b00	
		RAM1	RW	[3:2]	2'b00	
		RAM0	RW	[1:0]	2'b00	
0x04104424	APPDSP_RAMM ODE_SEL1	Reserved	RO	[31:30]	0	Reserved
		WEN	WO	[29]	0	Write Enable (RAMB)
				[28]	0	Write Enable (RAMA)
				[27]	0	Write Enable (RAM9)
				[26]	0	Write Enable (RAM8)
				[25]	0	Write Enable (RAM7)
				[24]	0	Write Enable (RAM6)
		Reserved	RO	[23:12]	0	Reserved
		RAMB	RW	[11:10]	2'b00	Power supply control settings 2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		RAMA	RW	[9:8]	2'b00	
		RAM9	RW	[7:6]	2'b00	
		RAM8	RW	[5:4]	2'b00	
		RAM7	RW	[3:2]	2'b00	
		RAM6	RW	[1:0]	2'b00	

Table PMU (Power Management Unit)-40 Power Supply Status (SRAM)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0410020C	SYSCPU_RAMM ODE_STAT	Reserved	RO	[31:14]	0	Reserved
		RAM3_64KB	RO	[13:12]	2'b11	Power supply control settings 2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		RAM2_64KB	RO	[11:10]	2'b11	
		RAM1_64KB	RO	[9:8]	2'b11	
		RAM0_32KB	RO	[7:6]	2'b11	
		RAM0_16KB	RO	[5:4]	2'b11	
		RAM0_8KB_1	RO	[3:2]	2'b11	
		RAM0_8KB_0	RO	[1:0]	2'b11	
0x04100214	TOP_SCU_RAM MODE_STAT	Reserved	RO	[31:20]	0	Reserved
		BKRAM1	RO	[19:18]	2'b11	Power supply status

		BKRAM0	RO	[17:16]	2'b11	2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
		Reserved	RO	[15:6]	0	Reserved
		SCUSEQ	RO	[5:4]	2'b00	Power supply status
		SCU_FIFO1	RO	[3:2]	2'b00	2'b11: On mode
		SCU_FIFO0	RO	[1:0]	2'b00	2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited setting
0x04100218	HOSTIFC_RAM MODE_STAT	Reserved	RO	[31:4]	0	Reserved
		SEQ	RO	[3:2]	2'b00	Power supply status
		RAM_1KB	RO	[1:0]	2'b00	2'b11: On mode 2'b01: Retention mode 2'b00: ShutDown mode 2'b10: Prohibited status
0x04100C40	GNSSDSP_RAM MODE_STAT	Reserved	RO	[31:16]	0	Reserved
		RAM89_128KB	RO	[15:14]	2'b11	Power supply status
		RAM67_128KB	RO	[13:12]	2'b11	2'b11: On mode
		RAM45_128KB	RO	[11:10]	2'b11	2'b01: Retention mode
		RAM3_64KB	RO	[9:8]	2'b11	2'b00: ShutDown mode
		RAM2_64KB	RO	[7:6]	2'b11	2'b10: Prohibited setting
		RAM1_64KB	RO	[5:4]	2'b11	
		RAM0_48KB	RO	[3:2]	2'b11	
		RAM0_16KB	RO	[1:0]	2'b11	
0x04104420	APPDSP_RAMM ODE_STAT0	Reserved	RO	[31:12]	0	Reserved
		RAM5	RO	[11:10]	2'b00	Power supply status
		RAM4	RO	[9:8]	2'b00	2'b11: On mode
		RAM3	RO	[7:6]	2'b00	2'b01: Retention mode
		RAM2	RO	[5:4]	2'b00	2'b00: ShutDown mode
		RAM1	RO	[3:2]	2'b00	2'b10: Prohibited setting
		RAM0	RO	[1:0]	2'b00	
0x04104424	APPDSP_RAMM ODE_STAT1	Reserved	RO	[31:12]	0	Reserved
		RAMB	RO	[11:10]	2'b00	Power supply status
		RAMA	RO	[9:8]	2'b00	2'b11: On mode
		RAM9	RO	[7:6]	2'b00	2'b01: Retention mode
		RAM8	RO	[5:4]	2'b00	2'b00: ShutDown mode
		RAM7	RO	[3:2]	2'b00	2'b10: Prohibited setting

		RAM6	RO	[1:0]	2'b00	

3.4.3.4 Power Supply Control (Analog Circuit)

Table PMU (Power Management Unit)-41 and Table PMU (Power Management Unit)-42 show the registers related to power supply control of the analog circuit. For the power supply control method, refer to the control flow described from Section 3.4.4.1.1 to Section 3.4.4.1.6.

Table PMU (Power Management Unit)-41 Power Supply Control Settings (Analog Circuit)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100004	ANA_PW_CTL	WEN	RO	[31:30]	0	Reserved
			WO	[29]	0	Write Enable (LPADC)
			WO	[28]	0	Write Enable (HPADC)
			RO	[27:26]	0	Reserved
			WO	[25]	0	Write Enable (RF_PLL)
			WO	[24]	0	Write Enable (RF_LO)
			WO	[23]	0	Write Enable (RF_ADC)
			WO	[22]	0	Write Enable (RF_IF)
			WO	[21]	0	Write Enable (RF_MIX)
			WO	[20]	0	Write Enable (RF_LNA)
			RO	[19]	0	Reserved
			WO	[18]	0	Write Enable (SYSPLL)
			WO	[17]	0	Write Enable (XOSC)
			WO	[16]	0	Write Enable (RCOSC)
		Reserved	RO	[15:14]	0	Reserved
		LPADC	RW	[13]	0	Power supply control setting 1: ON, 0: OFF
		HPADC	RW	[12]	0	
		Reserved	RO	[11:10]	0	Reserved
		RF_PLL	RW	[9]	0	Power supply control setting 1: ON, 0: OFF
		RF_LO	RW	[8]	0	
		RF_ADC	RW	[7]	0	
		RF_IF	RW	[6]	0	
		RF_MIX	RW	[5]	0	
		RF_LNA	RW	[4]	0	
		Reserved	RO	[3]	0	Reserved
		SYSPLL	RW	[2]	0	Power supply control setting 1: ON, 0: OFF
		XOSC	RW	[1]	0	
		RCOSC	RW	[0]	0	

0x04100008	ANA_EN_CTL	Reserved	RO	[31:26]	0	Reserved
		ON_XO_OSC_EN_SET	RW	[25]	1	XOSC oscillator Enable
		OFF_XO_OSC_EN_CLR	RW	[24]	1	
		Reserved	RO	[23:21]	0	Reserved
		ON_XO_OSCOUT_EN_SET	RW	[20]	1	XOSC oscillator output Enable
		OFF_XO_OSCOUT_EN_CLR	RW	[19]	1	
		ON_XO_EXT_EN_SET	RW	[18]	0	XOSC external clock operation Enable
		OFF_XO_EXT_EN_CLR	RW	[17]	0	
		Reserved	RO	[16:0]	0x1F7	Reserved
0x04100584	XOSC_CTRL2	Reserved	RW	[31:24]	0	Reserved (Do not change the initial value)
		IXO_LV_I_VAL3	RW	[23:16]	0	Oscillator current adjustment
		IXO_LV_I_VAL1	RW	[15:8]	0	Oscillator current adjustment
		Reserved	RW	[7:0]	0	Reserved (Do not change the initial value)

Table PMU (Power Management Unit)-42 Power Supply Status (Analog Circuit)

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100208	ANA_PW_STAT	Reserved	RO	[31:14]	0	Reserved
		LPADC	RO	[13]	0	Power supply status 1: ON, 0: OFF
		HPADC	RO	[12]	0	
		Reserved	RO	[11:10]	0	Reserved
		RF_PLL	RO	[9]	0	Power supply status 1: ON, 0: OFF
		RF_LO	RO	[8]	0	
		RF_ADC	RO	[7]	0	
		RF_IF	RO	[6]	0	
		RF_MIX	RO	[5]	0	
		RF_LNA	RO	[4]	0	
		Reserved	RO	[3]	0	Reserved
		SYSPLL	RO	[2]	0	Power supply status 1: ON, 0: OFF
		XOSC	RO	[1]	0	

		RCOSC	RO	[0]	0	

3.4.3.5 Power Supply Control Request

Table PMU (Power Management Unit)-43 shows the power supply control request registers. By writing “1” to PMU_PW_CTL.POWER_CTRL_ON, power supply control starts according to the value of the power supply control setting register (PWD_CTL, *_RAMMODE_SEL, ANA_PW_CTL).

Table PMU (Power Management Unit)-43 Power Supply Control Request

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100030	PMU_PW_CTL	Reserved	RO	[31:1]	0	Reserved
		POWER_CTRL_ON	WO	[0]	0	Power supply control request 1: Power supply control execution
0x0410021C	PMU_HW_STAT	Reserved	RO	[31:1]	-	Reserved
		POWER_CTRL_STAT	RO	[0]	0	Power supply control status 1: Power supply is being controlled 0: Power supply is not yet controlled

3.4.3.6 Interrupt

The PMU has two types of interrupts, each of which allows the control of status read, clear, and mask. The two interrupts (PMU_INT_STAT[1:0]) are ORed and sent to the CPU/DSP as INT_CAUSE0.PMU. For details, refer to Section 3.3.2. The following describes the details of the two interrupts. Table PMU (Power Management Unit)-44 shows a register list of the interrupts.

Interrupt

- **DONE** : Completion of power supply control
When power supply control is completed, this changes to “1”.
- **NOGO_CTRL** : Error in power supply setting
When a power supply control request is made with an incorrect setting of the power supply control register (**PWD_CTL**, ***_RAMMODE_SEL**, **ANA_PW_CTL**), this changes to “1”. At this time, the power supply control is not performed. The reason for the error can be checked by **PSW_CHECK**. For details, refer to Section 3.4.3.7.

Table PMU (Power Management Unit)-44 Interrupt

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100040	PMU_INT_STAT	Reserved	RO	[31:2]	-	Reserved
		NOGO_CTRL	RO	[1]	0	Interrupt request

		DONE	RO	[0]	0	Indicates the status after the interrupt factor is masked by the interrupt mask register.
0x04100044	PMU_RAW_INT_STAT	Reserved	RO	[31:2]	-	Reserved
		NOGO_CTRL	RO	[1]	0	Interrupt factor
		DONE	RO	[0]	0	1: Interrupt exists 0: No interrupt
0x04100048	PMU_INT_CLR	Reserved	WO	[31:2]	0	Reserved The API may change the value. Perform read-modify-write when writing values to NOGO_CTRL and DONE.
		NOGO_CTRL	WO	[1]	0	Interrupt clear
		DONE	WO	[0]	0	1: Clear
0x0410004C	PMU_INT_MASK	Reserved	RW	[31:2]	30'h 3C4	Reserved The API may change the value. Perform read-modify-write when writing values to NOGO_CTRL and DONE.
		NOGO_CTRL	RW	[1]	0	Interrupt mask
		DONE	RW	[0]	0	Processor notification setting of the interrupt factor 0: Notify 1: Do not notify

3.4.3.7 Power Supply Setting Check

During a power supply control request, the PMU checks whether or not there is an incorrect setting in the power supply setting. When there is an incorrect setting, the corresponding bit within the PSW_CHECK becomes “1” and power supply control is not performed.

Table PMU (Power Management Unit)-45 shows the registers of PSW_CHECK. Table PMU (Power Management Unit)-46 shows the content checked by PSW_CHECK.

Table PMU (Power Management Unit)-45 Power Supply Setting Check

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103000	PSW_CHECK	STATE	RO	[31:0]	0	Incorrect setting 1: Incorrect setting exists 0: No incorrect setting

Table PMU (Power Management Unit)-46 Power Supply Setting Check Items

PSW_CHECK Bit ^(1*)	Category	Content checked
[31]	Power supply control	“RCOSC power supply and PMU clock source check” When turning OFF the RCOSC, make sure to change the operation clock of the PMU from RCOSC to RTC_CLK_IN beforehand. When changing the operation clock of the PMU to RCOSC, turn ON the RCOSC beforehand. - You want to set the operation clock of the PMU to a clock other than RCOSC Refer to Section 3.4.4.1.1 for the RCOSC OFF control flow. - You want to turn ON the RCOSC Refer to Section 3.4.4.1.1 for the RCOSC ON control flow.
[21]	GNSS	“Power supply setting check (Power domain and SRAM) of GNSS Domain” When PWD_GNSS is ON, turn ON at least one of the SRAMs for GNSS DSP. When turning OFF all SRAMs for GNSS DSP, make sure to turn OFF PWD_GNSS too. - To turn ON the PWD_GNSS and SRAM for GNSSDP: PWD_CTL=0x20002000 GNSSDSP_RAMMODE_SEL=0xFF00FFFF & SRAM for GNSS DSP power supply setting - To turn OFF the PWD_GNSS and SRAM for GNSSDP: PWD_CTL=0x20000000 GNSSDSP_RAMMODE_SEL=0xFF000000
[18]		“Power supply setting check (RF and XOSC) of the GNSS Domain” When turning ON the RF, also turn ON the XOSC. When turning OFF the XOSC, also turn OFF the RF. - To turn ON the XOSC and RF: ANA_PW_CTL=0x00020002 (0x03F03F0 & RF power supply setting) - To turn OFF the XOSC and RF: ANA_PW_CTL=0x03F20000
[17]		“Power supply setting check (Power domain) of the GNSS Domain” When turning ON the PWD_GNSS, also turn ON the PWD_GNSS_ITP. When turning OFF the PWD_GNSS_ITP, also turn OFF the PWD_GNSS. - To turn ON the PWD_GNSS and PWD_GNSS_ITP: PWD_CTL=0x30003000 - To turn OFF the PWD_GNSS and PWD_GNSS_ITP: PWD_CTL=0x30000000

[16]		“Power supply setting check (RF and SRAM) of the GNSS Domain” When turning ON the SRAM for GNSS or RF, also turn ON the PWD_GNSS. When turning OFF the PWD_GNSS, also turn OFF the SRAM for GNSS and RF. - To turn ON the PWD_GNSS and SRAM for GNSS, RF: PWD_CTL=0x30003000 ANA_PW_CTL=0x00020002 (0x03F03F0 & RF power supply setting) GNSS_RAMMODE_SEL=0x3F000FFF - To turn OFF the PWD_GNSS and SRAM for GNSS, RF: PWD_CTL=0x20000000 GNSS_RAMMODE_SEL=0x3F000000 ANA_PW_CTL=0x03F00000
[12]	SCU	“Power supply setting check of the Sensor Domain” When turning ON the SRAM for SCU, HPADC, or LPADC, also turn ON the PWD_SCU. When turning OFF the PWD_SCU, also turn OFF the SRAM for SCU, HPADC, and LPADC. - To turn ON the PWD_SCU, SRAM for SCU, HPADC, and LPADC: PWD_CTL=0x00010001 ANA_PW_CTL=0x30003000 & (HPADC and LPADC power supply setting) TOP_SCU_RAMMODE_SEL=0x0000133F & SRAM for SCU power supply setting - To turn OFF the PWD_SCU, SRAM for SCU, HPADC, and LPADC: PWD_CTL=0x00010001 ANA_PW_CTL=0x30000000 TOP_SCU_RAMMODE_SEL=0x00001300
[9]	CPU	“Power supply setting check of the Application Domain” When turning ON power supply layers lower than the PWD_APP, also turn ON the PWD_APP. When turning OFF the PWD_APP, also turn OFF the power supply layers lower than the PWD_APP. Note: The layers lower than PWD_APP are as follows: PWD_APP_AUD, PWD_APP_SUB, PWD_APP_DSP, SRAM for Application Processor - To turn ON the power supply layers lower than the PWD_APP: PWD_CTL=0x01000100 (0x46004600 & PWD_APP_(AUD/SUB/DSP) power supply setting) APPDSP_RAMMODE_SEL0=0x3F000FFF APPDSP_RAMMODE_SEL1=0x3F000FFF - To turn OFF the PWD_APP: PWD_CTL=0x47000000 APPDSP_RAMMODE_SEL0=0x3F000000 APPDSP_RAMMODE_SEL1=0x3F000000
[4]	Analog circuit	“Power supply setting check of the XOSC and SYSPLL”

		When turning ON the SYSPLL, also turn ON the XOSC. When turning OFF the XOSC, also turn OFF the SYSPLL. - To turn ON the XOSC ON, SYSPLL: ANA_PW_CTL=0x00060006 - To turn OFF the XOSC OFF, SYSPLL: ANA_PW_CTL=0x00060000

(1*) The Bits not listed are Reserved.

3.4.4 Power Supply Control Flow

3.4.4.1 Basic Flow of Power Supply Control

The following describes the basic flow of power supply control. Make sure to control the power domain and SRAM in accordance with the basic flow of power supply control. In the case of Analog circuits, individual settings are required for each analog circuit before and after the basic flow of power supply control. For details on the control flow including individual settings, refer to Section 3.4.4.1.1 through Section 3.4.4.1.6.

1. Power supply control On/Off (/Retention) settings

PWD_CTL=0x40004000 (Example: PWD_APP_AUD=ON)

Refer to Table PMU (Power Management Unit)-47 and make the register settings of the desired power supply. For the setting restrictions, refer to the power supply control restrictions. For an actual example of power supply control, refer to Section 3.4.5.1.

Table PMU (Power Management Unit)-47 Power Supply Control Setting Values

Domain name	Power name	Register name	Off Control Setting Value	On Control Setting Value	Retention Control Setting Value
Always ON	PWD_PMU	—	—	—	—
	SRAM (Backup SRAM 32 KByte)	TOP_SCU_RAMMODE_SEL	0x01000000	0x01030000	0x01010000
	SRAM (Backup SRAM 32 KByte)	TOP_SCU_RAMMODE_SEL	0x02000000	0x020C0000	0x02040000
	RCOSC	ANA_PW_CTL	0x00010000	0x00010001	—
	XOSC	ANA_PW_CTL	0x00020000	0x00020002	—
	SYSPLL	ANA_PW_CTL	0x00040000	0x00040004	—
Sensor Domain	PWD_SCU	PWD_CTL	0x00010000	0x00010001	—
	SRAM (FIFO 8 KByte)	TOP_SCU_RAMMODE_SEL	0x00000100	0x00000103	0x00000101

	SRAM (FIFO 32 KByte)	TOP_SCU_RAMMODE_SEL	0x00000200	0x0000020C	0x00000204
	SRAM (Sequencer RAM)	TOP_SCU_RAMMODE_SEL	0x00001000	0x00001030	0x00001010
	ADC (HPADC)	ANA_PW_CTL	0x10000000	0x10001000	—
	ADC (LPADC)	ANA_PW_CTL	0x20000000	0x20002000	—
System and IOP Domain	PWD_CORE	PWD_CTL	0x00100000	0x00100010	—
	SRAM (SYSIOP Tile #0 8 KByte)	SYSCPU_RAMMODE_SEL	0x01000000	0x01000003	0x01000001
	SRAM (SYSIOP Tile #0 8 KByte)	SYSCPU_RAMMODE_SEL	0x02000000	0x0200000C	0x02000004
	SRAM (SYSIOP Tile #0 16 KByte)	SYSCPU_RAMMODE_SEL	0x04000000	0x04000030	0x04000010
	SRAM (SYSIOP Tile #0 32 KByte)	SYSCPU_RAMMODE_SEL	0x08000000	0x080000C0	0x08000040
	SRAM (SYSIOP Tile #1 64 KByte)	SYSCPU_RAMMODE_SEL	0x10000000	0x10000300	0x10000100
	SRAM (SYSIOP Tile #2 64 KByte)	SYSCPU_RAMMODE_SEL	0x20000000	0x20000C00	0x20000400
	SRAM (SYSIOP Tile #3 64 KByte)	SYSCPU_RAMMODE_SEL	0x40000000	0x40003000	0x40001000
	SRAM (GNSS DSP Tile #0 16 KByte)	GNSSDSP_RAMMODE_SEL	0x01000000	0x01000003	0x01000001
	SRAM (GNSS DSP Tile #0 48 KByte)	GNSSDSP_RAMMODE_SEL	0x02000000	0x0200000C	0x02000004
	SRAM (GNSS DSP Tile #1 64KByte)	GNSSDSP_RAMMODE_SEL	0x04000000	0x04000030	0x04000010
	SRAM (GNSS DSP Tile #2 64 KByte)	GNSSDSP_RAMMODE_SEL	0x08000000	0x080000C0	0x08000040
	SRAM (GNSS DSP Tile #3 64 KByte)	GNSSDSP_RAMMODE_SEL	0x10000000	0x10000300	0x10000100
	SRAM (GNSS DSP Tile #4,5 128 KByte)	GNSSDSP_RAMMODE_SEL	0x20000000	0x20000C00	0x20000400

	SRAM (GNSS DSP Tile #6,7 128 KByte)	GNSSDSP_RAMMODE_SEL	0x40000000	0x40003000	0x40001000
	SRAM (GNSS DSP Tile #8,9 128KByte)	GNSSDSP_RAMMODE_SEL	0x80000000	0x8000C000	0x80004000
	PWD_SYSIOP_SUB	PWD_CTL	0x00400000	0x00400040	—
	PWD_SYSIOP	PWD_CTL	0x00200000	0x00200020	—
	SRAM (HOSTIFC 1 KByte)	HOSTIFC_RAMMODE_SEL	0x01000000	0x01000003	0x01000001
	SRAM (HOSTIFC Sequencer RAM)	HOSTIFC_RAMMODE_SEL	0x02000000	0x0200000C	0x02000004
Applicati on Domain	PWD_APP	PWD_CTL	0x01000000	0x01000100	—
	SRAM (Application Processor Tile #0 128 KByte)	APPDSP_RAMMODE_SEL0	0x01000000	0x01000003	0x01000001
	SRAM (Application Processor Tile #1 128 KByte)	APPDSP_RAMMODE_SEL0	0x02000000	0x0200000C	0x02000004
	SRAM (Application Processor Tile #2 128 KByte)	APPDSP_RAMMODE_SEL0	0x04000000	0x04000030	0x04000010
	SRAM (Application Processor Tile #3 128 KByte)	APPDSP_RAMMODE_SEL0	0x08000000	0x080000C0	0x08000040
	SRAM (Application Processor Tile #4 128 KByte)	APPDSP_RAMMODE_SEL0	0x10000000	0x10000300	0x10000100
	SRAM (Application Processor Tile #5 128 KByte)	APPDSP_RAMMODE_SEL0	0x20000000	0x20000C00	0x20000400
	SRAM (Application Processor Tile #6 128 KByte)	APPDSP_RAMMODE_SEL1	0x01000000	0x01000003	0x01000001
	SRAM (Application Processor Tile #7 128 KByte)	APPDSP_RAMMODE_SEL1	0x02000000	0x0200000C	0x02000004
	SRAM (Application Processor Tile #8 128 KByte)	APPDSP_RAMMODE_SEL1	0x04000000	0x04000030	0x04000010
	SRAM (Application Processor Tile #9 128 KByte)	APPDSP_RAMMODE_SEL1	0x08000000	0x080000C0	0x08000040
	SRAM (Application Processor Tile #10 128 KByte)	APPDSP_RAMMODE_SEL1	0x10000000	0x10000300	0x10000100
	SRAM (Application Processor Tile #11 128 KByte)	APPDSP_RAMMODE_SEL1	0x20000000	0x20000C00	0x20000400
	PWD_APP_DSP	PWD_CTL	0x02000000	0x02000200	—
	PWD_APP_SUB	PWD_CTL	0x04000000	0x04000400	—
	PWD_APP_AUD	PWD_CTL	0x40000000	0x40004000	—

GNSS	PWD_GNSS_ITP	PWD_CTL	0x10000000	0x10001000	—
Domain	PWD_GNSS	PWD_CTL	0x20000000	0x20002000	—
	SRAM (GNSS BB#0)	GNSS_RAMMODE_SEL	0x01000000	0x01000003	0x01000001
	SRAM (GNSS BB#1)	GNSS_RAMMODE_SEL	0x02000000	0x0200000C	0x02000004
	SRAM (GNSS BB#2)	GNSS_RAMMODE_SEL	0x04000000	0x04000030	0x04000010
	SRAM (GNSS BB#3)	GNSS_RAMMODE_SEL	0x08000000	0x080000C0	0x08000040
	SRAM (GNSS BB#4)	GNSS_RAMMODE_SEL	0x10000000	0x10000300	0x10000100
	SRAM (GNSS BB#5)	GNSS_RAMMODE_SEL	0x20000000	0x20000C00	0x20000400
	RF (LNA)	ANA_PW_CTL	0x00100000	0x00100010	—
	RF (MIX)	ANA_PW_CTL	0x00200000	0x00200020	—
	RF (IF)	ANA_PW_CTL	0x00400000	0x00400040	—
	RF (ADC)	ANA_PW_CTL	0x00800000	0x00800080	—
	RF (LO)	ANA_PW_CTL	0x01000000	0x01000100	—
	RF (PLL)	ANA_PW_CTL	0x02000000	0x02000200	—

2. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

3. Interrupt mask cancel

PMU_INT_MASK.MSK[1:0]=2'b00

4. Power supply control execution

PMU_PW_CTL.POWER_CTRL_ON=1

5. Interrupt confirmation

Confirm **PMU_INT_STAT.STAT**[1:0]=2'b01

In the case of **PMU_INT_STAT.STAT**[1]=1, refer to Section 3.4.3.7.

6. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

7. Clock and reset control

Perform proper clock and reset control according to each power domain, SRAM, and Analog circuit.

Power Supply Control Restrictions

When power domains such as the SRAM are turned ON, make sure to turn ON all SRAMs in those power domains. The following describes an example of the power supply control setting.

- In the case of turning ON the PWD_APP (SRAM (Application Processor Tile #0-11) ON)
 - PWD_CTL**=0x01000100 (PWD_APP=ON)
 - APPDSP_RAMMODE_SEL0**=0x3F000FFF (SRAM (Application Processor Tile #0-5) =ON)
 - APPDSP_RAMMODE_SEL1**=0x3F000FFF (SRAM (Application Processor Tile #6-11) =ON)
- In the case of turning ON the PWD_GNSS (SRAM (GNSS BB#0-5) ON)
 - PWD_CTL**=0x20002000 (PWD_GNSS=ON)

- GNSS_RAMMODE_SEL=0x3F000FFF (SRAM (GNSS BB#0-5) =ON)

3.4.4.1.1 RCOSC

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the RCOSC.

1. RCOSC power supply ON setting
ANA_PW_CTL=32'h00010001
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. RCOSC power supply ON control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. Clock control
Control the supply/stop of the clock in accordance with the function block or Analog circuit you use.
 - When supplying the clock
 - **RCOSC_CTRL1.IRO_LV_SENSCLK_XEN=0** (for HPADC)
 - **RCOSC_CTRL1.IRO_LV_LOGICLK_XEN=0** (for each function block)
 - When stopping the clock
 - **RCOSC_CTRL1.IRO_LV_SENSCLK_XEN=1** (for HPADC)
 - **RCOSC_CTRL1.IRO_LV_LOGICLK_XEN=1** (for each function block)

ON => OFF Control Flow

The following describes the flow to turn OFF the power supply of the RCOSC. As a precondition, when there is a block using the RCOSC such as the PMU, use the API to switch the clock source to one other than the RCOSC before turning OFF the RCOSC. The clock of the PMU can be confirmed by **CKSEL_ROOT.RORTC_STAT_CLK_SEL2**.

The following describes the flow.

1. RCOSC power supply OFF setting
ANA_PW_CTL=32'h00010000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. RCOSC power supply OFF control

PMU_PW_CTL.POWER_CTRL_ON=1

5. Interrupt confirmation

Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**

6. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

3.4.4.1.2 XOSC

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the XOSC.

1. XOSC parameter setting

Refer to Table PMU (Power Management Unit)-48 for the settings of **ANA_EN_CTL**.

The XOSC has two operation modes as shown below, in which the register parameters vary according to the mode.

- Internal oscillation mode (system configuration that uses crystal oscillation)
Supported frequencies: 26 MHz
- External clock mode (system configuration that uses TCXO)
Supported frequencies: 26 MHz

Table PMU (Power Management Unit)-48 Parameter Setting for Each Mode

Register Name	Internal Oscillation Mode	External Clock Mode
ANA_EN_CTL.ON_XO_OSC_EN_SET	0	1
ANA_EN_CTL.OFF_XO_OSC_EN_CLR	0	1
ANA_EN_CTL.ON_XO_OSCOUT_EN_SET	0	1
ANA_EN_CTL.OFF_XO_OSCOUT_EN_CLR	0	1
ANA_EN_CTL.ON_XO_EXT_EN_SET	1	0
ANA_EN_CTL.OFF_XO_EXT_EN_CLR	1	0

2. XOSC current adjustment setting

- In the case of internal oscillation mode

Refer to Table PMU (Power Management Unit)-49 for the settings of **XOSC_CTRL2.IXO_LV_I_VAL1**.

Refer to Table PMU (Power Management Unit)-49 for the settings of **XOSC_CTRL2.IXO_LV_I_VAL3**.

- In the case of external clock mode

XOSC_CTRL2.IXO_LV_I_VAL1=8'h00

XOSC_CTRL2.IXO_LV_I_VAL3=8'h00

3. The setting value of current adjustment is different for each frequency of the XOSC.

Table PMU (Power Management Unit)-49 shows the assumed combination of the crystal oscillator, damping resistor, and the oscillation circuit setting.

Table PMU (Power Management Unit)-49 Current Adjustment Setting

Frequency [MHz]	Crystal oscillator		Damping Resistor Rd[Ω]	Oscillation Circuit Setting	
	Model Number	CL[pF]		Before oscillation XOSC_CTRL2.IXO_L V_I_VAL1	After current setting change XOSC_CTRL2.IXO_L V_I_VAL3
19.2	DSR211ATH (KDS)	7	0	30	30
26		8	0	60	40
26	TAS-2016B (TEW)	8	0	60	40
32.768		4	0	20	20
52		5.2	0	90	70

4. XOSC power supply ON control

ANA_PW_CTL=32'h00020002

5. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

6. Interrupt mask cancel

PMU_INT_MASK.MSK[1:0]=2'b00

7. Power supply control execution

PMU_PW_CTL.POWER_CTRL_ON=1

8. Interrupt confirmation

Confirm **PMU_INT_STAT.STAT**[1:0]=2'b01

9. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

10. Clock control

Control the supply/stop of the clock in accordance with the function block or Analog circuit you use.

- In the case of supplying the clock
 - **XOSC_CTRL.IXO_LV_LOCLK_EN**=1 (for GNSS)
 - **XOSC_CTRL.IXO_LV_PLLCLK_EN**=1 (for SYSPLL)
 - **XOSC_CTRL.IXO_LV_SENCLK_EN**=1 (for HPADC)
 - **XOSC_CTRL.IXO_LV_LOGICLK_EN**=1 (for each function block)
- In the case of stopping the clock
 - **OSC_CTRL.IXO_LV_LOCLK_EN**=0 (for GNSS)
 - **XOSC_CTRL.IXO_LV_PLLCLK_EN**=0 (for SYSPLL)
 - **XOSC_CTRL.IXO_LV_SENCLK_EN**=0 (for HPADC)

- **XOSC_CTRL.IXO_LV_LOGICLK_EN=0** (for each function block)

ON => OFF Control Flow

The following describes the flow to turn OFF the power supply of the XOSC. As a precondition, make sure that the power supply of the SYSPLL is turned OFF during this operation.

1. XOSC power supply OFF setting
ANA_PW_CTL=32'h00020000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. XOSC power supply OFF control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11

3.4.4.1.3 SYSPLL

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the SYSPLL. As a precondition, perform the control with the power supply of the XOSC turned ON, and the clock supplied to the SYSPLL (XOSC_CTRL.IXO_LV_PLLCLK_EN=1).

1. SYSPLL division ratio setting

Refer to Table PMU (Power Management Unit)-50 for the settings of **SYS_PLL_CTRL2.ISP_LV_SELRCDIV**.

Refer to Table PMU (Power Management Unit)-50 for the settings of **SYS_PLL_CTRL2.ISP_LV_SELFBDIV**.

The frequency of the SYSPLL is determined by the frequency of the XOSC and register value. The following describes the division ratio settings of the SYSPLL.

Table PMU (Power Management Unit)-50 SYSPLL Division Ratio Setting

XOSC Frequency [MHz]	SYS_PLL_CTRL2.ISP_L V_SELRCDIV[1:0]	SYS_PLL_CTRL2.ISP_L V_SELFBDIV[2:0]	SYSPLL Frequency [MHz]
16.368	0	0	163.68
	0	1	196.42
19.2	1	2	144.00
	0	0	192.00
26	1	1	156.00
	1	2	195.00
32.736	1	0	163.68
	1	1	196.42
52	3	1	156.00
	3	2	195.00

2. SYSPLL power supply ON setting

ANA_PW_CTL=32'h00040004

3. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

4. Interrupt mask cancel

PMU_INT_MASK.MSK[1:0]=2'b00

5. SYSPLL power supply ON control

PMU_PW_CTL.POWER_CTRL_ON=1

6. Interrupt confirmation

Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**

7. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

8. Clock control

Control the supply/stop of the clock in accordance with the function block or Analog circuit you use.

- In the case of supplying the clock
 - **SYS_PLL_CTRL1.ISP_LV_ENDSPCLK=1** (for each function block)
 - **SYS_PLL_CTRL1.ISP_LV_ENGPADCCLK=1** (for GNSS)
- In the case of stopping the clock
 - **SYS_PLL_CTRL1.ISP_LV_ENDSPCLK=1** (for each function block)
 - **SYS_PLL_CTRL1.ISP_LV_ENGPADCCLK=1** (for GNSS)

ON => OFF Control Flow

The following describes the flow to turn OFF the power supply of the SYSPLL.

1. SYSPLL power supply OFF setting

ANA_PW_CTL=32'h00040000

2. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

3. Interrupt mask cancel

PMU_INT_MASK.MSK[1:0]=2'b00

4. SYSPLL power supply OFF control

PMU_PW_CTL.POWER_CTRL_ON=1

5. Interrupt confirmation

Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**

6. Interrupt clear

PMU_INT_CLR.CLR[1:0]=2'b11

3.4.4.1.4 HPADC

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the HPADC. The PWD_SCU must be turned ON for this operation.

1. HPADC initial setting

Turn ON either the XOSC or the RCOSC according to the operation mode of the HPADC.

For details, refer to Section xxx.

2. HPADC power supply ON setting

ANA_PW_CTL=32'h10001000

3. Interrupt clear

- PMU_INT_CLR.CLR[1:0]=2'b11**
4. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
 5. HPADC power supply ON control
PMU_PW_CTL.POWER_CTRL_ON=1
 6. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
 7. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
 8. Reset release
SWRESET_SCU.XRST_SCU_HPADC=1
 9. Clock control
For details, refer to Section xxx.

ON => OFF Control Flow

The following describes the flow to turn OFF the power supply of the HPADC.

1. HPADC power supply OFF setting
ANA_PW_CTL=32'h10000000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. HPADC power supply OFF control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. HPADC reset enable
SWRESET_SCU.XRST_SCU_HPADC=0
8. HPADC clock stop
For details, refer to Section xxx.

3.4.4.1.5 LPADC

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the LPADC. The PWD_SCU must be turned ON for this operation.

1. LPADC power supply ON setting
ANA_PW_CTL=32'h20002000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. LPADC power supply ON control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. LPADC reset release
SWRESET_SCU.XRST_SCU_LPADC=1
8. Clock control
For details, refer to Section xxx.

ON => OFF Control Flow

The following describes the flow for turning OFF the power supply of the LPADC.

1. LPADC power supply OFF setting
ANA_PW_CTL=32'h20000000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. LPADC power supply OFF control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. LPADC reset application
SWRESET_SCU.XRST_SCU_LPADC=0

8. LPADC clock stop
For details, refer to Section xxx.

3.4.4.1.6 RF

OFF => ON Control Flow

The following describes the flow to turn ON the power supply of the RF (LNA, MIX, IF, ADC, LO, PLL). The XOSC, PWD_GNSS_ITP, and PWD_GNSS must be turned ON for this operation.

1. RF power supply ON setting
ANA_PW_CTL=32'h03F003F0
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. RF power supply ON control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. Clock control
For details, refer to Section 3.12.

ON => OFF Control Flow

The following describes the flow to turn OFF the power supply of the RF (LNA, MIX, IF, ADC, LO, PLL).

1. RF power supply OFF setting
ANA_PW_CTL=32'h03F00000
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
3. Interrupt mask cancel
PMU_INT_MASK.MSK[1:0]=2'b00
4. RF power supply OFF control
PMU_PW_CTL.POWER_CTRL_ON=1
5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT[1:0]=2'b01**
6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
7. RF clock stop
For details, refer to Section 3.12.

3.4.5 Power Supply Control Example

3.4.5.1 Actual Example of Power Supply Control

By ORing the power supply control setting (**PWD_CTL**, ***_RAMMODE_SEL**, **ANA_PW_CTL**) of each power supply, you can control multiple power supplies together by a single power supply control request (**PMU_PW_CTL.POWER_CTRL_ON**). The PMU recognizes the upper layer and lower layer of the power supplies and automatically controls the order of the power supply switch control. When controlling the power supply from OFF to ON, the control is started from the power supplies in the upper layer. Conversely, when controlling the power supply from ON to OFF, the control is started from the lower layer. The following describes an example of power supply control.

Power supplies to control

- PWD_APP (OFF=>ON)
- PWD_APP_AUD (OFF=>ON)
- PWD_SCU (ON=>OFF)
- SRAM (Application Processor Tile #4) (OFF=>ON)

Power supply control flow

1. Power supply control setting

PWD_CTL=0x41014100

OR the following power supply control settings

- **PWD_CTL=0x01000100** (PWD_APP=ON)
- **PWD_CTL=0x40004000** (PWD_APP_AUD=ON)
- **PWD_CTL=0x00010000** (PWD_SCU=ON)

APPDSP_RAMMODE_SEL0=0x3F000FFF

Note:

Due to the power supply control restrictions, turn ON all SRAMs of the PWD_APP layer.

OR the following power supply control settings

- **APPDSP_RAMMODE_SEL0=0x01000003** (SRAM (Application Processor Tile #0) =ON)
- **APPDSP_RAMMODE_SEL0=0x0200000C** (SRAM (Application Processor Tile #1) =ON)
- **APPDSP_RAMMODE_SEL0=0x04000030** (SRAM (Application Processor Tile #2) =ON)
- **APPDSP_RAMMODE_SEL0=0x080000C0** (SRAM (Application Processor Tile #3) =ON)
- **APPDSP_RAMMODE_SEL0=0x10000300** (SRAM (Application Processor Tile #4) =ON)
- **APPDSP_RAMMODE_SEL0=0x20000C00** (SRAM (Application Processor Tile #5) =ON)

APPDSP_RAMMODE_SEL1=0x3F000FFF

OR the following power supply control settings

- **APPDSP_RAMMODE_SEL1=0x01000003** (SRAM (Application Processor Tile #6) =ON)

- **APPDSP_RAMMODE_SEL1**=0x0200000C (SRAM (Application Processor Tile #7) =ON)
 - **APPDSP_RAMMODE_SEL1**=0x04000030 (SRAM (Application Processor Tile #8) =ON)
 - **APPDSP_RAMMODE_SEL1**=0x080000C0 (SRAM (Application Processor Tile #9) =ON)
 - **APPDSP_RAMMODE_SEL1**=0x10000300 (SRAM (Application Processor Tile #10) =ON)
 - **APPDSP_RAMMODE_SEL1**=0x20000C00 (SRAM (Application Processor Tile #11) =ON)
2. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
 3. Interrupt mask setting
PMU_INT_MASK.MSK[1:0]=2'b00
 4. Power supply control execution
PMU_PW_CTL.POWER_CTRL_ON=1
 5. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT**[1:0]=2'b01
 6. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
 7. Clock and reset control
Perform proper clock and reset control according to each power domain, SRAM, and Analog circuits.
 8. Turn OFF all SRAMs other than the power supply control setting SRAM (Application Processor Tile #4)
APPDSP_RAMMODE_SEL0=0x2F00CFF (SRAM (Application Processor Tile #0-3, 5) =OFF)
APPDSP_RAMMODE_SEL1=0x3F000000 (SRAM (Application Processor Tile #6-11) =OFF)
 9. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11
 10. Interrupt mask setting
PMU_INT_MASK.MSK[1:0]=2'b00
 11. Power supply control execution
PMU_PW_CTL.POWER_CTRL_ON=1
 12. Interrupt confirmation
Confirm **PMU_INT_STAT.STAT**[1:0]=2'b01
 13. Interrupt clear
PMU_INT_CLR.CLR[1:0]=2'b11

3.4.5.2 Application Processor Sleep/Wakeup Control

In this document, the term Sleep refers to cases when any of the power domains of the CXD5602 turn OFF, or when the DSP belonging to that power domain is not operating. On the other hand, Wakeup refers to cases when they turn ON, or when the DSP belonging to that power domain starts operating. Since the Application Processor of the PWD_APP_DSP cannot perform Sleep/Wakeup of its own power domain (PWD_APP_DSP), Sleep/Wakeup is performed from the System and I/O Processor instead.

The following describes an overview and the control flow of Sleep/Wakeup of the PWD_APP_DSP. Also, Figure

PMU (Power Management Unit)-32 shows the control flow diagram.

Control Overview

- Sleep control

The Application Processor requests Sleep (PWD_APP_DSP "OFF") control to the System and I/O Processor. After the Application Processor has made this request, it enters WFI state. The System and I/O Processor then confirms that the Application Processor has entered WFI state, and performs OFF control of the PWD_APP_DSP.

- Wakeup control

Wakeup occurs as a result of an interrupt to the Application Processor. However, the Application Processor is in Sleep, and cannot receive the interrupt nor perform ON control of the PWD_APP_DSP. Therefore, during Sleep, the System and I/O Processor receives the interrupt instead, and performs ON control of the PWD_APP_DSP.

Sleep (PWD_APP_DSP=OFF) Control Flow

- Control of Application Processor side

Since Sleep control is not performed during the operation of the Application Processor, the interrupt is masked and the Application Processor enters WFI state.

1. Mask all interrupts made to the Application Processor.

INT_EN*=0

For details on the interrupt mask **INT_EN***, refer to Section 3.3.2.

2. Request Sleep (PWD_APP_DSP "OFF") control to the System and I/O Processor.
3. Issue WFI command.

- Control of System and I/O Processor side (reference)

The OFF request of the PWD_APP_DSP is received from the Application Processor, and the control starts.

1. The WFI monitor register (**DSP_SLEEPING**) of the Application Processor is polled, and the change to WFI state is confirmed.
2. The PWD_APP_DSP is turned OFF (Refer to Section 3.4.4.1 for Basic flow of power supply control).
3. Cancel the interrupt mask of receiving the interrupt on the Application Processor's behalf.

The following is the setting for using SYDMAC[0] as the Wakeup trigger.

INT_EN3.SYDMAC[0]=1

Wakeup (PWD_APP_DSP=ON) Control Flow

Wakeup starts when the interrupt is received. As an example, the following describes the flow when Wakeup is performed using the interrupt **INT_CAUSE3.SYMAC[0]** as the trigger.

- Control of the System and I/O Processor side

1. Confirm **INT_CAUSE3.SYMAC[0]=1**

2. Interrupt mask

INT_EN3.SYDMAC[0]=0

3. Turn ON the PWD_APP_DSP (Refer to Section 3.4.4.1 Basic flow of power supply control)

- Control of Application Processor side (reference)

Starts when the System and I/O Processor turns ON the power supply of the PWD_APP_DSP

1. Interrupt mask cancel

INT_EN2.SYDMAC[0]=1

2. Detect interrupt **INT_CAUSE2.SYDMAC[0]** and clear

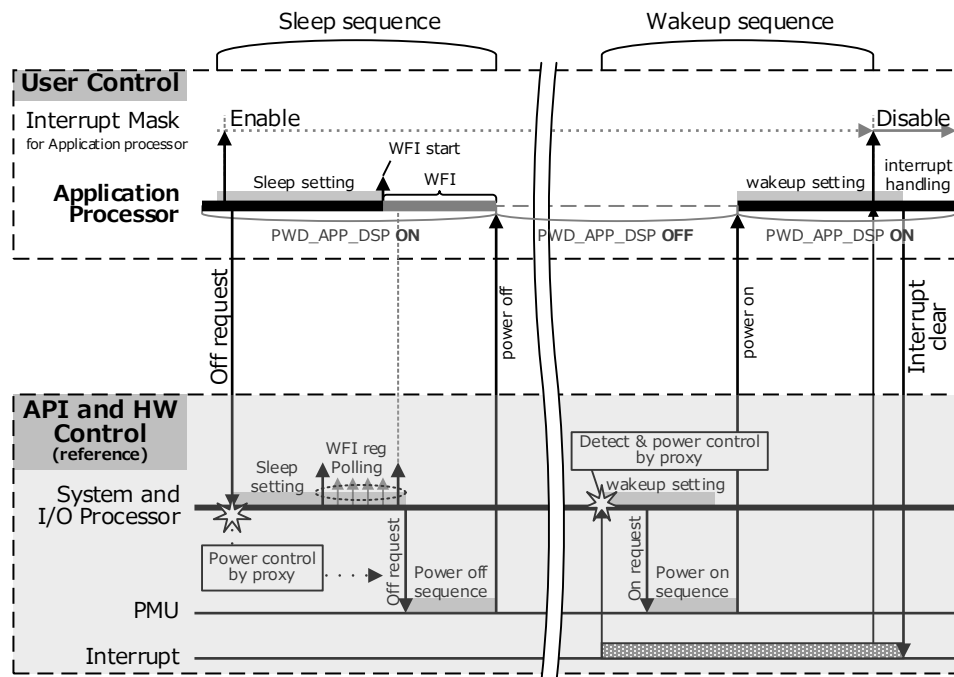


Figure PMU (Power Management Unit)-32 Sleep/Wakeup Control Flow of the Application Processor

3.5 Clock and Reset (Clock Reset Generator)

3.5.1 Overview

The Clock Reset Generator (CRG) is the block that controls the clock and reset of the overall CXD5602.

For the clock sources, there are XOSC and RCOSC, SYSPLL, RTC Clock, and RF. The RTC Clock is supplied from the outside of the CXD5602.

Clock control includes clock switching, clock supply, and clock stop. Reset control includes reset enable, reset release, and reset enable using the WDT.

Since clock control and reset control are performed using the API, this Section describes the information for confirming the statuses of the clock and reset.

3.5.2 Clock Scheme for CRG

Figure Clock and Reset (Clock Reset Generator)-33 shows the overall clock scheme for the CRG, while Figure Clock and Reset (Clock Reset Generator)-34 shows the details. In Figure Clock and Reset (Clock Reset Generator)-34, the registers indicated as ANA (number), SEL (number), and CG (number) are explained in the register descriptions provided in the CRG Section. For descriptions on **CKDIV_CPU_DSP_BUS.CK_M0**, **CKDIV_CPU_DSP_BUS.CK_AHB**, and **CKDIV_CPU_DSP_BUS.CK_APB**, refer to Section 3.14.3.

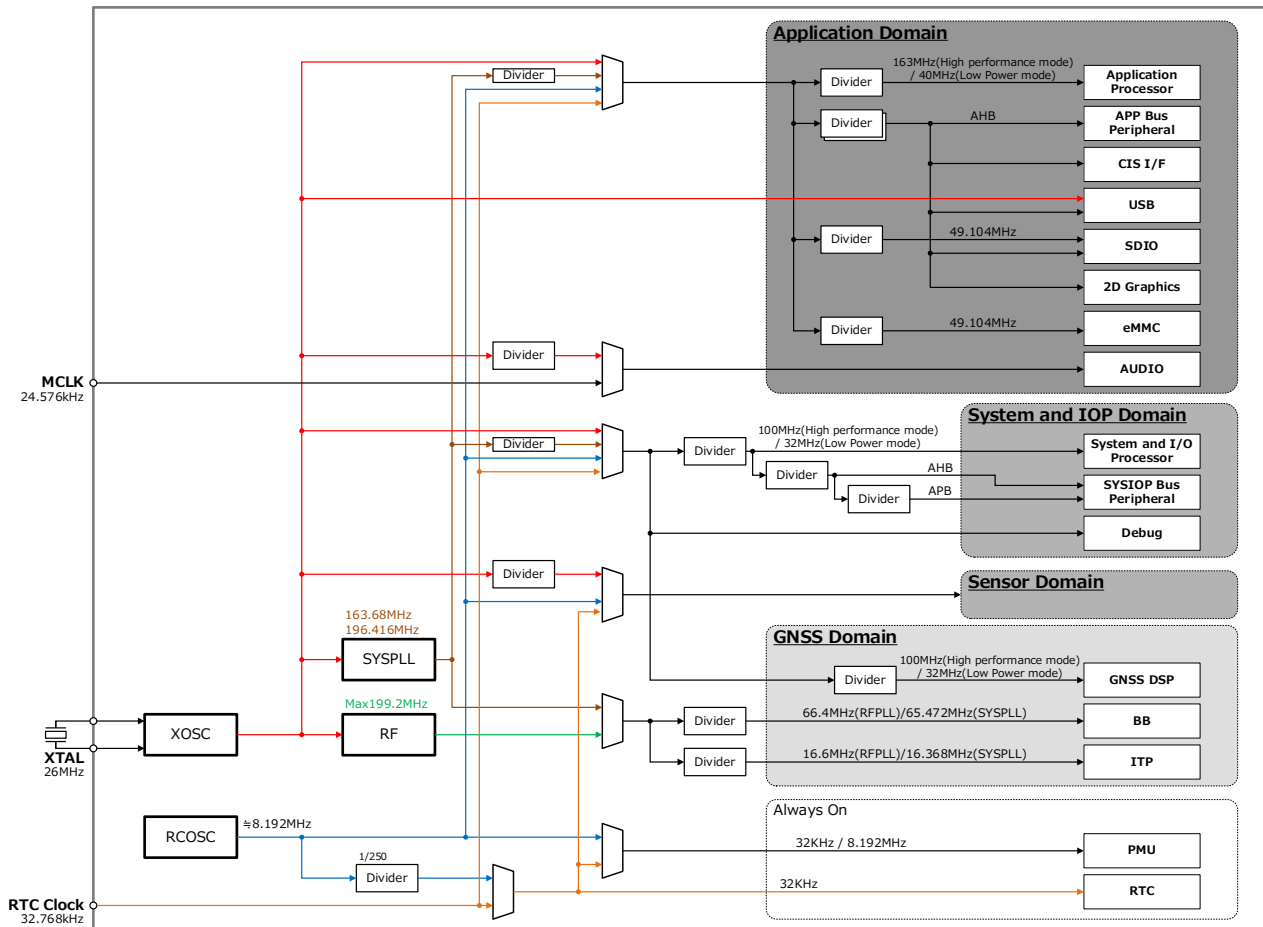


Figure Clock and Reset (Clock Reset Generator)-33 CRG Control Area within Overall Clock Scheme

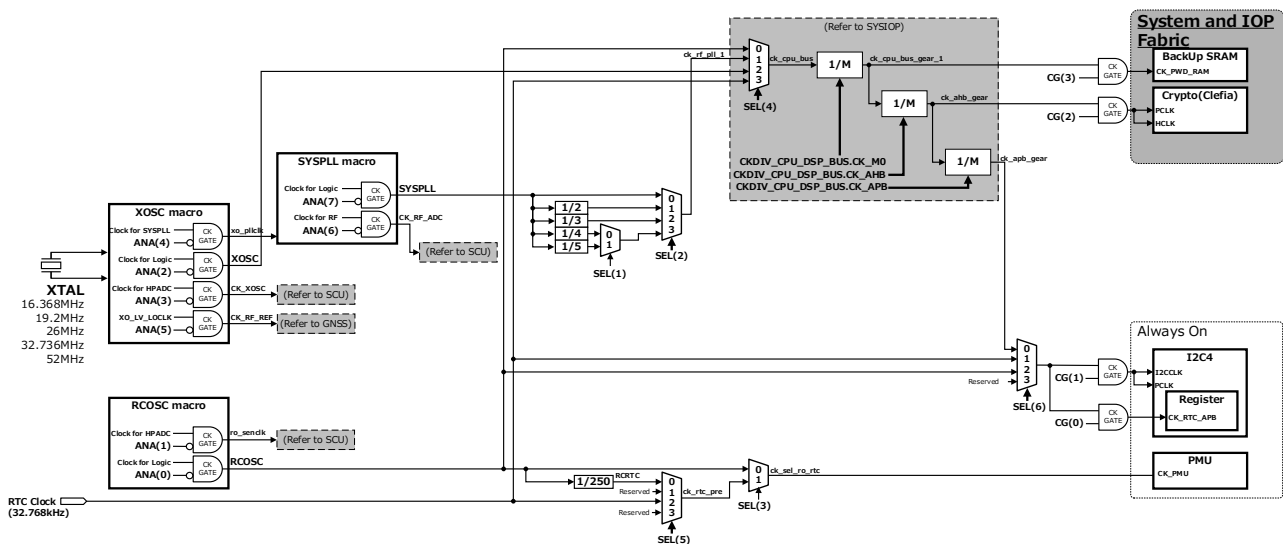


Figure Clock and Reset (Clock Reset Generator)-34 CRG Clock Scheme

3.5.3 Analog Circuits

The CRG has three analog circuits (RCOSC block, XOSC block, and SYSPLL block). The following shows the setting confirmation registers of each analog circuit. Some of them are RW registers, but use them as RO registers. For descriptions of the RF block, refer to Section 3.12.

3.5.3.1 RCOSC Block Setting Confirmation

The RCOSC is an internal ring oscillator that operates at 8.192 MHz. In initial state, the oscillation frequency is higher than 8.192 MHz, but by using the calibration process of the API, it can be adjusted to 8.192 MHz.

3.5.3.1.1 Register Descriptions

Table Clock and Reset (Clock Reset Generator)-51 shows the control registers related to the RCOSC block.

Table Clock and Reset (Clock Reset Generator)-51 RCOSC Block Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100590	RCOSC_CTRL1	Reserved	RW	[31:15]	0	Reserved
		IRO_LV_SENSCLK_XEN	RW	[14]	1	Indicated as ANA(1) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for HPADC 0: Enable, 1: Disable
		IRO_LV_LOGICLK_XEN	RW	[13]	0	Indicated as ANA(0) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for each function block 0: Enable, 1: Disable
		Reserved	RW	[12:0]	1	Reserved

3.5.3.2 XOSC Block Setting Confirmation

The XOSC operates at the following 5 frequencies. The selectable frequencies are different between internal oscillation and external clock input mode.

- Frequency
 - 26 MHz
- Mode
 - Internal oscillation mode (system configuration using crystal oscillation)
 - *Supported frequencies: 26 MHz
 - External clock input mode (system configuration using TCXO)

*Supported frequencies: 26 MHz

The XOSC can be used as the processor's operation clock and is also supplied as the reference clock to the SYSPLL and RF.

3.5.3.2.1 Register Descriptions

Table Clock and Reset (Clock Reset Generator)-52 shows the control registers related to the XOSC block.

Table Clock and Reset (Clock Reset Generator)-52 XOSC Block Status Register

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100580	XOSC_CTRL	Reserved	RW	[31:20]	0	Reserved
		IXO_LV_LOCLK_EN	RW	[19]	0	Indicated as ANA(5) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for GNSS 0: Clock supplied, 1: Clock stopped
		IXO_LV_PLLCLK_EN	RW	[18]	0	Indicated as ANA(4) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for SYSPLL block 0: Clock supplied, 1: Clock stopped
		IXO_LV_SENCLK_EN	RW	[17]	0	Indicated as ANA(3) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for HPADC 0: Clock supplied, 1: Clock stopped
		IXO_LV_LOGICLK_EN	RW	[16]	0	Indicated as ANA(2) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for each function block 0: Clock supplied, 1: Clock stopped
		Reserved	RW	[15:0]	0	Reserved

3.5.3.3 SYSPLL Block Setting Confirmation

The frequencies of SYSPLL can be confirmed by the XOSC frequency and division ratio setting register as shown in Table Clock and Reset (Clock Reset Generator)-53.

Table Clock and Reset (Clock Reset Generator)-53 SYSPLL Frequency Confirmation

XOSC Frequency [MHz]	SYS_PLL_CTRL2.ISP_L V_SELRCDIV[1:0]	SYS_PLL_CTRL2.ISP_L V_SELFBDIV[2:0]	SYSPLL Frequency [MHz]
16.368	0	0	163.68
	0	1	196.42
19.2	1	2	144.00
	0	0	192.00
26	1	1	156.00
	1	2	195.00
32.736	1	0	163.68
	1	1	196.42
52	3	1	156.00
	3	2	195.00

3.5.3.3.1 Register Descriptions

Table Clock and Reset (Clock Reset Generator)-54 shows the control registers related to the SYSPLL block.

Table Clock and Reset (Clock Reset Generator)-54 SYSPLL Block Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100588	SYS_PLL _CTRL1	Reserved	RW	[31:4]	0	Reserved
		ISP_LV_ENDSPCLK	RW	[3]	0	Indicated as ANA(7) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for each function block 0: Clock supplied, 1: Clock stopped
		Reserved	RW	[2]	0	Reserved
		ISP_LV_ENGPADC CLK	RW	[1]	0	Indicated as ANA(6) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for GNSS 0: Clock supplied, 1: Clock stopped
		Reserved	RW	[0]	0	Reserved
0x0410058C	SYS_PLL	ISP_LV_SELRCDIV	RW	[31:30]	0	RCDIV frequency division ratio switching

	_CTRL2	ISP_LV_SELFBDIV	RW	[29:27]	3'b001	FBDIV frequency division ratio switching
		Reserved	RW	[26:0]	0	Reserved

3.5.4 Clock Setting Confirmation

3.5.4.1 Register Descriptions

The following describes the status confirmation registers of the clock switching and the clock Enable. Some of them are RW registers, but use them as RO registers.

3.5.4.1.1 Clock Switching

Table Clock and Reset (Clock Reset Generator)-55 shows the status registers of clock switching.

Table Clock and Reset (Clock Reset Generator)-55 Clock Switching Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041004C4	CKSEL_ROOT	PMU_STAT_CLK_SEL4	RO	[31:30]	0	Indicated as SEL(5) in Figure Clock and Reset (Clock Reset Generator)-34 PMU's clock source switching status 2'b00: RCRTC (frequency of dividing the RCOSC by 250) 2'b01: Reserved 2'b10: RTC Clock 2'b11: Reserved
		Reserved	RW	[29:24]	0	Reserved
		STAT_CLK_SEL4	RO	[23:22]	0	Indicated as SEL(4) in Figure Clock and Reset (Clock Reset Generator)-34 Clock source switching status for System and I/O Processor/AHB/APB 2'b00: RCOSC 2'b01: SYSPLL 2'b10: XOSC 2'b11: RTC Clock
		Reserved	RW	[21:14]	0	Reserved

		RORTC_STAT_CLK_SEL2	RO	[13]	0	Indicated as SEL(3) in Figure Clock and Reset (Clock Reset Generator)-34 Clock source switching status for power supply control 0: RCOSC 1: RTC Clock
		Reserved	RW	[12]	0	Reserved
		RFPLL1_STAT_CLK_SEL4	RO	[11:10]	0	Indicated as SEL(2) in Figure Clock and Reset (Clock Reset Generator)-34 SYSPLL frequency division switching status 2'b00: No frequency division 2'b01: divided by 2 (Duty H:L=1:1) 2'b10: divided by 3 (Duty H:L=2:1) 2'b11: divided by 4 (Duty H:L=1:1) or divided by 5 (Duty H:L=3:2)
		Reserved	RW	[9:3]	0	Reserved
		CPU_PLL_DIV5	RW	[2]	0	Indicated as SEL(1) in Figure Clock and Reset (Clock Reset Generator)-34 Either SYSPLL4 or 5 frequency division switching status 0: divided by 4 1: divided by 5
		Reserved	RW	[1:0]	0	Reserved
0x041004C8	CKSEL_P MU	Reserved	RO	[31:2]	0	Reserved
		SEL_RTC_PCLK	RW	[1:0]	0	Indicated as SEL(6) in Figure Clock and Reset (Clock Reset Generator)-34 I2C4 clock source switching status 2'b00: ck_apb_gear 2'b01: RTC Clock 2'b10: RCOSC 2'b11: Prohibited setting

3.5.4.1.2 Clock Enable

Table Clock and Reset (Clock Reset Generator)-56 shows the status registers of clock Enable (clock supplied/clock stopped).

Table Clock and Reset (Clock Reset Generator)-56 Clock Enable Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041004C0	PMU_CON_RE_CKE	Reserved	RO	[31:4]	0	Reserved
		BKMEM	RW	[3]	1	Indicated as CG(3) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for BackUpSRAM 1: Clock supplied 0: Clock stopped
		HCLK_KAKI	RW	[2]	0	Indicated as CG(2) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for Crypto (Clefia)
		RTC_PCLK	RW	[1]	1	Indicated as CG(1) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for I2C4
		PMU_RTC_PCLK	RW	[0]	1	Indicated as CG(0) in Figure Clock and Reset (Clock Reset Generator)-34 Clock Enable for I2C4 register IF

3.5.5 Power Domain Reset

The reset of each power domain can be controlled by the registers excluding some domains.

When releasing a reset, first perform ON control of the corresponding power domain, and then release the reset.

To enable a reset, first perform OFF control of the corresponding power domain, and then enable the reset.

Table Clock and Reset (Clock Reset Generator)-57 shows the relation between each power domain and the reset control registers.

Table Clock and Reset (Clock Reset Generator)-57 Power Domain and the Reset Control Registers

Power Domain	Register
PWD_PMU	None
PWD_CORE	Reset is automatically released at start up
PWD_SYSIOP	
PWD_SYSIOP_SUB	
PWD_SCU	PWD_RESET0.PWD_SCU
PWD_APP	PWD_RESET0.PWD_APP
PWD_APP_DSP	Enables/releases reset of domain layers lower than the PWD_APP
PWD_APP_SUB	
PWD_APP_AUD	
PWD_GNSS_ITP	PWD_RESET0.PWD_GNSS_ITP
PWD_GNSS	PWD_RESET0.PWD_GNSS

3.5.5.1 Register Descriptions

Table Clock and Reset (Clock Reset Generator)-58 shows the reset registers of the power domain. There is a Write Enable for each reset control bit, and reset control is performed for only the power domain to which “1” has been written to the Write Enable.

Table Clock and Reset (Clock Reset Generator)-58 Reset Registers of the Power Domain

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100060	PWD_RE SET0	WEN	RO	[31:30]	0	Reserved
			WO	[29]	0	Write Enable (PWD_GNSS)
				[28]	0	Write Enable (PWD_GNSS_ITP)
				[27:25]	0	Reserved
				[24]	0	Write Enable (PWD_APP)
				[23]	0	Reserved
				[22]	0	Write Enable (PWD_SYSIOP_SUB)
				[21:17]	0	Reserved
				[16]	0	Write Enable (PWD_SCU)
		Reserved	RO	[15:14]	0	Reserved
		PWD_GNSS	RW	[13]	0	Reset of PWD_GNSS power domain 0: Reset is performed 1: Reset release
		PWD_GNSS_ITP	RW	[12]	0	Reset of PWD_GNSS_ITP power domain.
		Reserved	RO	[11:9]	0	Reserved
		PWD_APP	RW	[8]	0	Reset of PWD_APP power domain
		Reserved	RO	[7]	0	Reserved
		PWD_SYSIOP_SUB	RW	[6]	1	Reset of PWD_SYSIOP_SUB power domain
		Reserved	RO	[5:1]	0	Reserved
		PWD_SCU	RW	[0]	0	Reset of PWD_SCU power domain

3.5.6 Reset by WDT

3.5.6.1 Function Details

By detecting the asserting of the WDT within the System and I/O Processor, a reset is automatically issued to each block of the CXD5602. However, reset by the WDT is not performed for the following registers or SRAM. (Reset is performed only during POR).

- Register: **RAMMODE.LS** (0x041006E4)
- Register: **BOOT_CAUSE.RAW_WDT_REBOOT** (0x04100484)
- SRAM: BackUpRAM

Note:

In the case of accessing the BackUpRAM after reset by WDT, clear the WDT factor register.

The WDT asserting flag of the System and I/O Processor is stored in the

BOOT_CAUSE.RAW_WDT_REBOOT.

To clear the flag, write “1” to the **BOOT_CAUSE.CLR_WDT_REBOOT.**

Reset by WDT can be made valid/invalid by the **WDT_SRST_EN.EN.**

3.5.6.2 Register Descriptions

Table Clock and Reset (Clock Reset Generator)-59 shows the control registers of reset by WDT.

Table Clock and Reset (Clock Reset Generator)-59 WDT Reset Control Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100640	WDT_SRST_EN	Reserved	RO	[31:1]	0	Reserved
		EN	RW	[0]	0	System reset by WDT valid/invalid 0: Invalid 1: Valid
0x04100484	BOOT_CAUSE	Reserved	RO	[31:1]	0	Reserved
		CLR_WDT_REBOOT	WO	[5]	0	WDT asserting flag clear 1: Clear BOOT_CAUSE.CAUSE.RAW_WDT_REBOOT to “0”
		CLR_INITIAL_BOOT	WO	[4]	0	Boot flag clear 1: Clear BOOT_CAUSE.CAUSE.RAW_INITIAL_BOOT to “0”
		Reserved	RO	[3:2]	0	Reserved
		RAW_WDT_REBOOT	RO	[1]	0	WDT asserting flag 1: Reset enable occurred by WDT asserting.

		RAW_INITIAL_BOOT	RO	[0]	1	Boot flag 1: Boot by POR or WDT When booted by POR RAW_WDT_REBOOT =0 RAW_INITIAL.BOOT =1 When booted from WDT RAW_WDT_REBOOT =1 RAW_INITIAL.BOOT =1

3.6 RTC

3.6.1 Outlines and Features

Real Time Clock (RTC) continues counting time up with 32.768 kHz clock frequency. RTC is made up of 15-bit PreCounter that generates one second interval, and 32-bit PostCounter that counts time every second. When Time Counter meets Alarm-set time, RTC outputs an Alarm. The Alarm can be used for CPU interrupt.

Two RTC systems are embedded in this LSI.

List of RTC

- RTC0 (power supply domain: PWD_PMU)
- RTC1 (power supply domain: PWD_SYSIOP)

RTC0 is supplied with VDD_CORE of CXD5602, and after the reset release, it continues counting time. On the other hand, RTC1 counts time only when PWD_SYSIOP is powered on. When the PWD_SYSIOP power supply is turned off, the Time Counter returns to “0”. As for power on/off setting of RTC0 and RTC1, refer to Chapter 3.4.

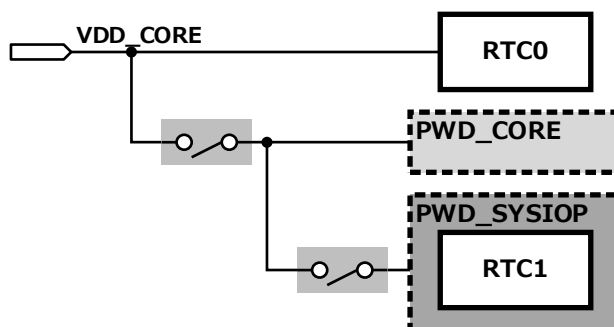


Figure RTC-35 RTC0/1 Power Supply Framework

Time Synchronization

In this manual, copying Time Counter values between RTCs is referred to as Time Synchronization. RTC0 and RTC1 can mutually synchronize Time Counter values. Time Counter values of a RTC IC outside CXD5602, typically the CXD5247 PMIC, can be synchronized to RTC0 or RTC1.

3.6.2 Clock Input

The clock source of the RTC is selected from either a real time clock (32.768 kHz) provided by an RTC IC outside CXD5602 or real time clock from an internal clock (about 32 kHz) divided from the RCOSC. Initial value after the reset release is “0” (see Table 3.6-1). When you use RCOSC, you must calibrate it to 8.192 MHz by using API, and then use it for the RTC.

Table RTC-60 Clock Resource of RTC

Clock Selection CKSEL_ROOT. PMU_STAT_CLK_SEL4[1]	Explanation
0	Clock resource is RCOSC. The RCOSC is calibrated to 8.192 MHz for use. Frequency is about 32 kHz. (initial value after the reset release of CXD5602)
1	Clock resource is real time clock provided from RTC_CLK_IN terminal. Frequency is 32.768 kHz

RTC Clock, which is connected to RTC1 and APB IF (RTC0/1 register control) block, can be provided or stopped providing by Clock Enable. Provide RTC1 and register with RTC Clock before controlling them.

Table RTC-61 Clock Enable of RTC

Clock Enable SYSIOP_CKEN.SYSIOP_RTC	Explanation
0	stops RTC Clock
1	provides with RTC Clock (initial value after the reset release of CXD5602)

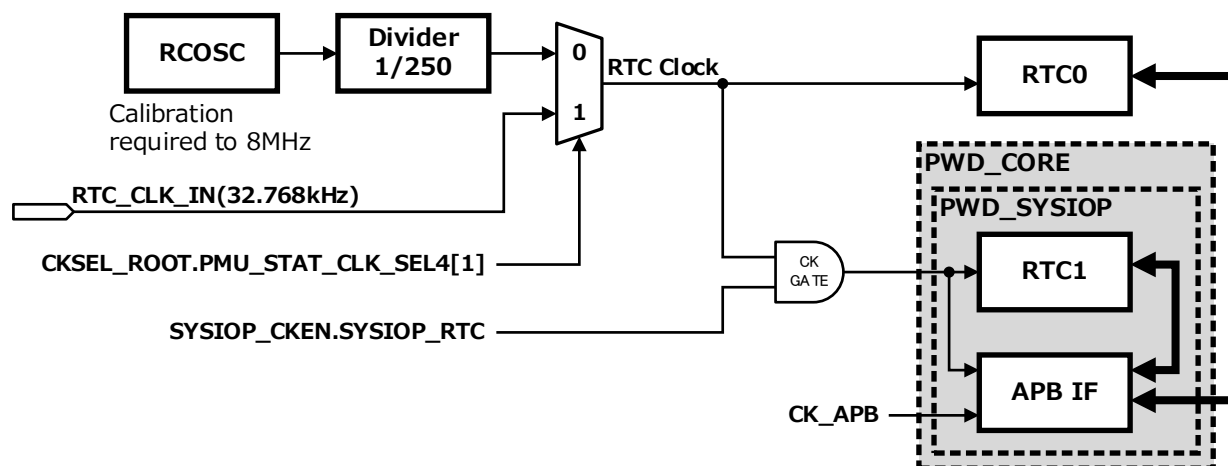


Figure RTC-36 Clock Resources of RTC

3.6.3 Function List

Table RTC-62 shows list of functions that this block holds.

Table RTC-62 Function List

No	Function Name	Description
1	RTC Counter Update/Synchronization	updates internal RTC counter in variety of conditions
2	Alarm Output	outputs Alarm Flag at the prescribed time

3.6.4 Function Block Diagrams

Figure RTC-37 is a block diagram that shows functional specification of this block. There are one Time Counter and three Alarm Timers. Registers are set via APB IF block. APB IF block is operated by PWD_SYSIOP power supply. RTC0 can select one Alarm from three Alarms, and output it from CXD5602 RTC_IRQ_OUT terminal. Update function of Time Counter (Time Update) is shown in the block diagram on the next page.

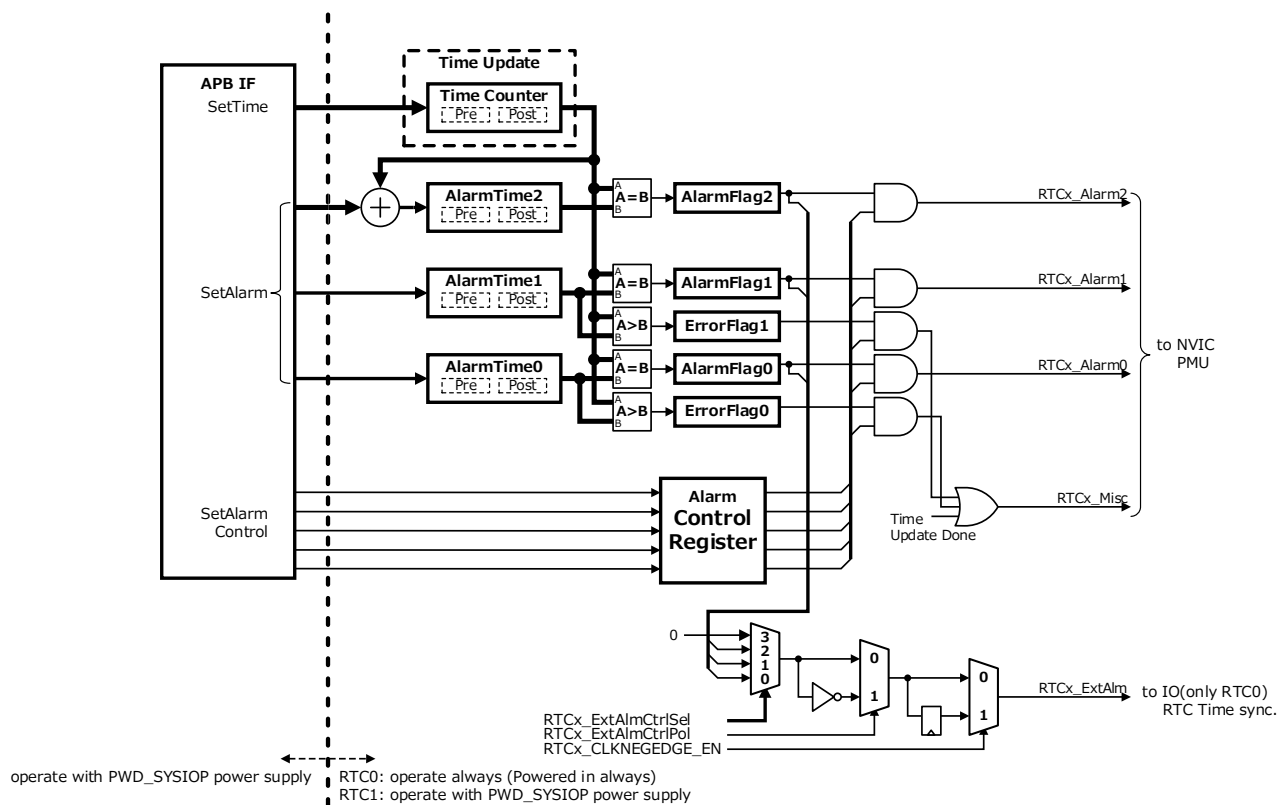


Figure RTC-37 RTC Block Diagram

As for Time Counter, there are two ways of updating and synchronizing time separately. By using Interrupt, you can check whether the Time Counter has been completely updated or not.

- How to set Time Counter
 1. You can set the designated Time Counter value
 2. You can adjust the current Time Counter
- How to set Time Synchronization
 3. You can set another RTC Time Counter value inside CXD5602.
 4. At the timing of asserting either External Alarm Flag (Interrupt from PMIC_INT) or Alarm from RTC inside CXD5602 (RTCx_ExtAlm), you can set the designated Time Counter value.

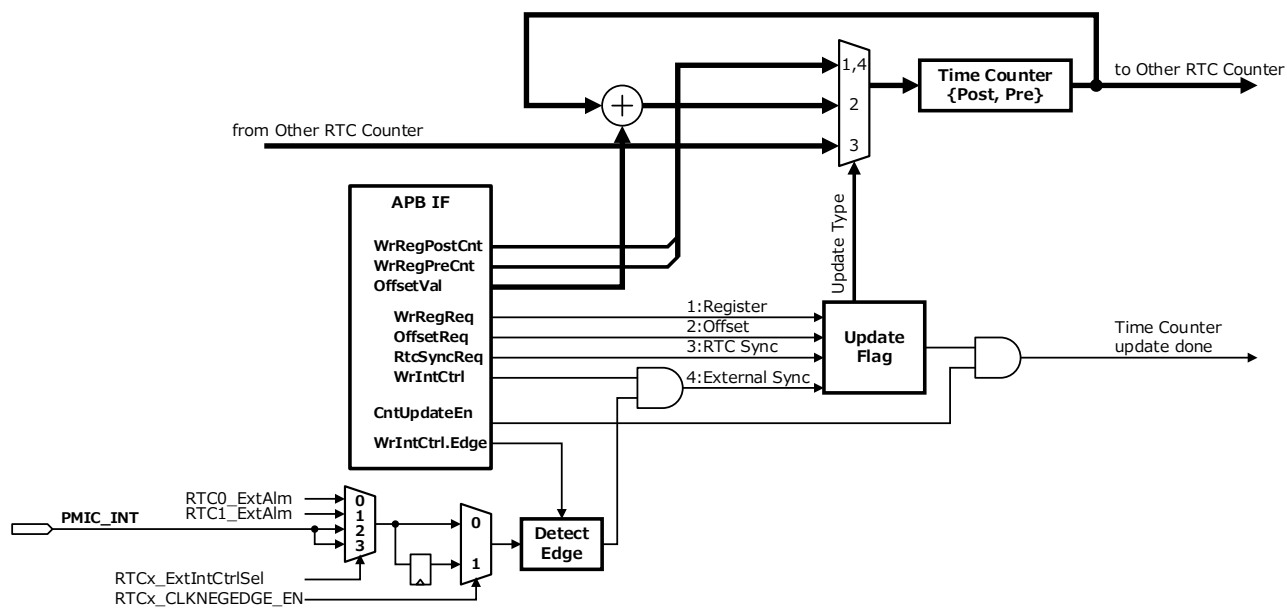


Figure RTC-38 RTC (Time Update) Block Diagram

3.6.4.1 Address Map

RTC0 and RTC1 have each Base Address and register for synchronization setting. Addresses are as follows.

- RTC0
 - 0x04108000 Base Address
 - 0x04100730 Time Synchronization setting
- RTC1
 - 0x04109000 Base Address
 - 0x41030470 Time Synchronization setting

3.6.5 Detailed Function and Control Specification

3.6.5.1 List of Registers

Table RTC-63 Register List of Counter Value Write Control System

Offset	Register Name	Attribute	Function	Initial Value
0x00	WrRegPostCnt	RW	Time Counter value (PostCounter)	0x00000000
0x04	WrRegPreCnt	RW	Time Counter value (PreCounter)	0x00000000
0x08	WrRegReq	RW	Request for setting of Time Counter value	0x00000000
0x0C	Reserved	RO	Reserved	0x00000000
0x10	Reserved	RO	Reserved	0x00000000
0x14	Reserved	RO	Reserved	0x00000000
0x18	WrIntCtrl	RW	Request for waiting for External Alarm Flag Edge Detection Control of External Alarm Flag	0x00000000
0x1C	WrIntClr	RW	External Synchronization Cancel of Request for waiting for External Alarm Flag	0x00000000
0x20	OffsetVal	RW	Correction value of Time Counter (PreCounter)	0x00000000
0x24	OffsetReq	RW	Correction request for Time Counter (PreCounter)	0x00000000
0x28	RtcSyncReq	RW	Synchronization request to other RTC (synchronizing one RTC's time with another RTC's time)	0x00000000
0x2C	Reserved	RO	Reserved	0x00000000

Table RTC-64 Register List of Time Counter Value Read Control System

Offset	Register Name	Attribute	Function	Initial Value
0x30	RdReq	RW	Read Request for PostCounter and PreCounter	0x00000000
0x34	RdPostCnt	RO	PostCounter Read Value at Read Request	0x00000000
0x38	RdPreCnt	RO	PreCounter Read Value at Read Request	0x00000000
0x3C	Reserved	RO	Reserved	0x00000000
0x40	RtPostCnt	RO	PostCounter Read Value when RtPostCnt Register was read	0x00000000
0x44	RtPreCnt	RO	PreCounter Read Value when RtPostCnt Register was read	0x00000000
0x48	Reserved	RO	Reserved	0x00000000
0x4C	Reserved	RO	Reserved	0x00000000

Table RTC-65 Register List of Alarm Control System

Offset	Register name	Attribute	Function	Initial Value
0x50	SetAlmPostCnt0	RW	Comparison Value of PostCounter for Alarm0	0xFFFFFFFF
0x54	SetAlmPreCnt0	RW	Comparison Value of PostCounter for Alarm0 and Status The status of some bits is RO.	0x00007FFF
0x58	SetAlmPostCnt1	RW	Comparison Value of PostCounter for Alarm1	0xFFFFFFFF
0x5C	SetAlmPreCnt1	RW	Comparison Value of PreCounter for Alarm1 and Status The status of some bits is RO.	0x00007FFF
0x60	SetAlmPostCnt2	RW	Comparison Value of PostCounter for Alarm2	0xFFFFFFFF
0x64	SetAlmPreCnt2	RW	Comparison Value of PostCounter for Alarm2 and Status The status of some bits is RO.	0x00007FFF
0x68	Reserved	RO	Reserved	0x00000000
0x6C	Reserved	RO	Reserved	0x00000000
0x70	AlmClr	WO	Clear of Normal Alarm Flag and Error Alarm Flag	0x00000000
0x74	AlmOutEn0	RW	Enable Signal Control and Status of O(Err)Alarm0, Read Value of DbgAlmOutEn0 (Enable Signal Value for Alarm0 currently used by RTC) The status of some bits is RO.	0x00000000
0x78	AlmOutEn1	RW	Enable Signal Control and Status of O(Err)Alarm1, Read Value of DbgAlmOutEn1 (Enable Signal Value for Alarm1 currently used by RTC) The status of some bits is RO.	0x00000000
0x7C	AlmOutEn2	RW	Enable Signal Control and Status of O(Err)Alarm2, Read Value of DbgAlmOutEn2 (Enable Signal Value for Alarm2 currently used by RTC) The status of some bits is RO.	0x00000000
0x80	AlmFlg	RO	Normal Alarm Flag and Error Alarm Flag	0x00000000
0x84	Reserved	RO	Reserved	0x00000000
0x88	Reserved	RO	Reserved	0x00000000
0x8C	Reserved	RO	Reserved	0x00000000
0x90	DbgSetAlmPostCnt0	RO	Read Value of DbgSetAlmCnt0[46:15] (Comparison Value of PostCounter for Alarm0 currently used by RTC)	0xFFFFFFFF
0x94	DbgSetAlmPreCnt0	RO	Read Value of DbgSetAlmCnt0[14:0] (Comparison Value of PreCounter for Alarm0 currently used by RTC)	0x00007FFF
0x98	DbgSetAlmPostCnt1	RO	Read Value of DbgSetAlmCnt1[46:15]	0xFFFFFFFF

			(Comparison Value of PostCounter for Alarm1 currently used by RTC)	
0x9C	DbgSetAlmPreCnt1	RO	Read Value of DbgSetAlmCnt1[14:0] (Comparison Value of PreCounter for Alarm1 currently used by RTC)	0x00007FFF
0xA0	DbgSetAlmPostCnt2	RO	Read Value of DbgSetAlmCnt2[46:15] (Comparison Value of PostCounter for Alarm2 currently used by RTC)	0xFFFFFFFF
0xA4	DbgSetAlmPreCnt2	RO	Read Value of DbgSetAlmCnt2[14:0] (Comparison Value of PreCounter for Alarm2 currently used by RTC)	0x00007FFF
0xA8	Reserved	RO	Reserved	0x00000000
0xAC	Reserved	RO	Reserved	0x00000000

Table RTC-66 Register List of Time Update Confirming System

Offset	Register Name	Attribute	Function	Initial Value
0xB0	CntUpdateClr	WO	Clear of interrupt notifying update completion of RTC Counter	0x00000000
0xB4	CntUpdateEn	RW	Enable Signal Control of interrupt notifying update completion of RTC Counter	0x00000000
0xB8	CntUpdateFlg	RO	Interrupt flag notifying update completion of RTC Counter	0x00000000
0xBC	Reserved	RO	Reserved	0x00000000
0xC0	DiffSignBit	RO	Sign bit of difference value between one RTC Counter and other RTC Counter	0x00000000
0xC4	DiffPostCnt	RO	Read Value of difference value [46:15] between one RTC Counter and other RTC Counter	0x00000000
0xC8	DiffPreCnt	RO	Read Value of difference value [14:0] between one RTC Counter and other RTC Counter	0x00000000
0xCC	Reserved	RO	Reserved	0x00000000

Table RTC-67 List of External Alarm Output and Time Synchronization Register

Absolute Address	Register Name	Attribute	Function	Initial Value
0x04100730	RTC0_RTC_CTL	RW	List of RTC0 external alarm output and time synchronization register	0x00000000
0x41030470	RTC1_RTC_CTL	RW	List of RTC1 external alarm output and time synchronization register	0x00000000

3.6.5.2 Register Descriptions

By turning off the PWD_SYSIOP power supply, all register values of RTC1 (from 0x04109000 to 0x041090C8) return to initial values. However, no register values of RTC0 (from 0x04108000 to 0x041080C8) return to initial values. When tuning on the PWD_SYSIOP power supply again, alarm information set in the RTC0 can be read. The following are registers that do not return to initial values.

- AlmOutEn(0/1/2).Dbg
- AlmOutEn(0/1).ErrDbg
- DbgSetAlmPostCnt(0/1/2).Dbg
- DbgSetAlmPreCnt(0/1/2).Dbg
- AlmFlg.Flg(0/1/2)
- AlmFlg.ErrFlg(0/1)

3.6.5.2.1 **WrRegPostCnt(0x00)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RW															

- bit[31:0] : Post[31:0] (PostCounter Write Value)
This is a value reflected on PostCounter of RTC when Write Request (WrRegReq) is issued, or when RTC receives an interrupt (External Alarm Flag) from PMIC_INT.

3.6.5.2.2 **WrRegPreCnt(0x04)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RW														

- bit[14:0] : Pre[14:0] (PreCounter Write Value)

This is a value reflected on PreCounter of RTC when Write Request (WrRegReq) is issued, or when RTC receives External Alarm Flag.

3.6.5.2.3 **WrRegReq(0x08)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Busy A
-															RW

When you write “1” on **WrRegReq.BusyA**, this register issues a write request. After the write request is issued, **WrRegPostCnt** values and **WrRegPreCnt** values are reflected on RTC Counter values. (Of RTC Counter 47 bits, **WrRegPostCnt** values are reflected on higher 32 bits, and **WrRegPreCnt** values are reflected on lower 15 bits.) This register is cleared to “0” after executing the request and becomes possible to issue a request again. (**OffsetReq.BusyA** and **RdReq.BusyA** indicate similar status.)

- bit[0] : BusyA (Write Request)

BusyA	Description of Functions
0	Writing 0: You cannot write “0”.
1	Writing 1: issues Write Request

	When WrReg(Post/Pre)Cnt value is reflected to (Post/Pre)Counter and Write Request becomes possible to be issued again, this register is cleared to “0” automatically.

3.6.5.2.4 **WrIntCtrl(0x18)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Edge	Reserved						Busy
-								RW	-						RW

- bit[0] : Busy (Request for waiting for External Alarm Flag)

When you write “1” on Busy, the internal RTC comes into the status of waiting for External Alarm Flag. When the internal RTC detects the edge of the External Alarm Flag during this waiting status, **WrIntPostCnt** value and **WrIntPreCnt** value are reflected on PostCounter and PreCounter separately, and the internal RTC is synchronized with the external RTC.

You can cancel Request for waiting for External Alarm Flag by writing “1” on **WrIntClr** register.

Busy	Description of Functions
0	Writing 0: You cannot write “0”.
1	Writing 1: makes internal RTC come into the status of waiting for the External Alarm Flag. When the internal RTC detects the External Alarm Flag during this waiting status and WrInt(Post/Pre)Cnt value is reflected on (Post/Pre)Counter, this register is cleared to “0” automatically.

- bit[8] : Edge (Positive/Negative Edge Detection of the External Alarm Flag)

Edge	Description of Functions
0	Writing 0: detects rising edges of the External Alarm Flag and synchronizes the internal RTC with the external RTC.
1	Writing 1: detects falling edges of the External Alarm Flag and synchronizes the internal RTC with the external RTC.

3.6.5.2.5 **WrIntClr(0x1C)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Busy
-															RW

- bit[0] : Busy (Cancel of waiting for External Alarm Flag)

When you write “1” on Busy, this register cancels Request for waiting for External Alarm Flag (**WrIntCtrl.Busy** is cleared to “0”).

Busy	Description of Functions
0	Writing 0: You cannot write “0”.
1	Writing 1: cancels a Request for waiting for External Alarm Flag. When it is canceled, this register is cleared to “0” automatically.

3.6.5.2.6 **OffsetVal(0x20)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Offset							
-								RW							

- bit[7:0] : Offset[7:0] (Correction value of RTC Counter value)

This register adds Offset value to RTC PreCounter. The Offset range is from -64 to 63.

Set the register value with two’s complements. When carry or borrow to PostCounter occurs, this register updates PostCounter.

3.6.5.2.7 **OffsetReq(0x24)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Busy A
-															RW

- bit[0] : BusyA (Correction request for RTC Counter value)

This register issues a correction request for RTC Counter value. After issuing the request, it adds **OffsetVal** value to RTC Counter.

BusyA	Description of Functions
0	Writing 0: You cannot write "0".
1	Writing 1: issues a correction request for RTC. After correcting RTC Counter, this register is cleared to "0" when the same request becomes possible to be issued again.

3.6.5.2.8 RtcSyncReq(0x28)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Req
-															RW

- bit[0] : Req (Synchronization request with other RTC Counter)

When you write “1”, this register issues a synchronization request. After issuing the request, this register makes one RTC import the other internal RTC counter value to its own value, and makes it synchronize with the other RTC. (Example: When this register issues a synchronization request to RTC0, RTC0 imports RTC1’s RTC Counter value and is synchronized with RTC1.)

Req	Description of Functions
0	Writing 0: You cannot write “0”.
1	Writing 1: issues a synchronization request with the other RTC Counter. After completing the synchronization, this register is cleared to “0” automatically when the same request becomes possible to be issued again.

3.6.5.2.9 **RdReq(0x30)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Busy A
-															RW

- bit[0] : BusyA (Read Request)

When you write “1”, this register issues a Read Request. Once the Read Request is issued, RTC Counter value at the time when it is issued can be read from **RdPostCnt** and **RdPreCnt**.

BusyA	Description of Functions
0	Writing 0: You cannot write “0”.
1	Writing 1: issues a Read Request. After reflecting values on RdPostCnt and RdPreCnt , this register is cleared to “0” automatically when the same request becomes possible to be issued again.

3.6.5.2.10 **RdPostCnt(0x34)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RO															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RO															

- bit[31:0] : Post[31:0] (PostCounter value at the time of Read Request)

By reading this register, you can see the PostCounter value at the point of time when the read request was issued.

3.6.5.2.11 **RdPreCnt(0x38)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RO														

- bit[14:0] : Pre[14:0] (PreCounter value at the time of Read Request)

By reading this register, you can see the PreCounter value at the point of time when the read request was issued.

3.6.5.2.12 **RtPostCnt(0x40)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RO															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RO															

- bit[31:0] : Post[31:0] (PostCounter value when RtPostCnt was read)
The following are differences from Rd(Post/Pre)Cnt.
 - There is no need to issue a Read Request (**RdReq**).
 - After you write “1” on **RdReq**, there is no restriction to wait for **RdReq** to become 0.
- Restriction on the use of this register
 - AS for **Rt(Post/Pre)Cnt**, read **RtPostCnt** before reading **RtPreCnt**.
 - If relation between CK_APB and CK_RTC (RTC Clock (32.768kHz)) is “frequency of CK_APB < frequency of CK_RTC × 10”, do not read **Rt(Post/Pre)Cnt**. The value cannot be guaranteed.

3.6.5.2.13 **RtPreCnt(0x44)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RO														

- bit[14:0] : Pre[14:0] (PreCounter value when PostCounter was read)
By reading this register, you can see the PreCounter value at the point of time when you read RtPostCnt.

3.6.5.2.14 **SetAlmPostCnt0(0x50)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RW															

- bit[31:0] : Post[31:0] (Comparison Value of PostCounter for **AlmFlg.Flg0** and **AlmFlg.ErrFlg0**)

This register sets Operation time (PostCounter) of Alarm0.

This register compares **SetAlm(Post/Pre)Cnt0** with RTC Counter (PostCounter and PreCounter) by using absolute value, and generates Normal Alarm0 or Error Alarm0.

Normal Alarm0 or Error Alarm0 is generated when the RTC Counter value meets the following conditions.

- Normal Alarm: is generated if value written on **SetAlm(Post/Pre){0,1}** matches RTC Counter value
- Error Alarm: is generated if written value is smaller than RTC Counter value when **SetAlmPre{0,1}** is set

- Restriction on the use of this register

AS for **SetAlm(Post/Pre)Cnt{0,1,2}**, write values on **SetAlmPostCnt{0,1,2}** before writing values on **SetAlmPreCnt{0,1,2}**.

•

3.6.5.2.15 **SetAlmPreCnt0(0x54)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															Busy
-															RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RW														

- bit[14:0] : Pre[14:0] (Comparison value of PreCounter for AlmFlg.Flg0 and AlmFlg.ErrFlg0)

This register sets operation time (PreCounter) of Alarm0.

It takes time to reflect a new Alarm Operation time. During reflecting, do not update the Alarm Operation time. You can check whether it is in the process of reflecting by using **Busy**.

- bit[16] : Busy (**SetAlmPreCnt0** Write Busy status)

This register indicates how far **SetAlm(Post/Pre)Cnt0** register is reflected.

When **Busy** indicates “1”, the register is reflecting Alarm Operation time (means that **SetAlm(Post/Pre)Cnt0** must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: Alarm Operation time is not set or reflected completely.
1	Reading 1: Alarm Operation time is being reflected. SetAlm(Post/Pre)Cnt0 must not be written.

3.6.5.2.16 SetAlmPostCnt1(0x58)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RW															

- bit[31:0] : Post[31:0] (Comparison Value of PostCounter for **AlmFlg.Flg1** and **AlmFlg.ErrFlg1**)
This register sets Operation time (PostCounter) of Alarm1.
This register compares **SetAlm (Post/Pre) Cnt1** with RTC Counter (PostCounter and PreCounter) by using absolute value, and generates Normal Alarm1 or Error Alarm1.

3.6.5.2.17 SetAlmPreCnt1(0x5C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															Busy
-															RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RW														

- bit[31:0] : Pre[14:0] (Comparison Value of PreCounter for **AlmFlg.Flg1** and **AlmFlg.ErrFlg1**)
This register sets Operation Time (PreCounter) of the Alarm1.
It takes time to reflect a new Alarm Operation time. During reflecting, do not update the Alarm Operation time. You can check whether it is in the process of reflecting by using Busy.
- bit[16] : Busy (SetAlmPreCnt1 Write Busy status)
When **Busy** indicates “1”, the register is reflecting Alarm Operation time (means that **SetAlm(Post/Pre)Cnt1** must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: Alarm Operation time is not set or reflected completely.

1	Reading 1: Alarm Operation time is being reflected. SetAlm(Post/Pre)Cnt1 must not be written.

3.6.5.2.18 SetAlmPostCnt2(0x60)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Post															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post															
RW															

- bit[31:0] : Post[31:0] (Comparison Value of PostCounter for **AlmFlg.Flg2**)

This register sets Operation time (PostCounter) of Alarm2.

The function of Alarm2 is different from that of Alarm0 and Alarm1.

AlmFlg.Flg2 is asserted when time passes to the value set on **SetAlm(Post/Pre)Cnt2**, starting from the time written on **SetAlmPreCnt2**.

3.6.5.2.19 SetAlmPreCnt2(0x64)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															Busy
-															RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RW														

bit[31:0] : Pre[14:0] (Comparison Value of PostCounter for AlmFlg.Flg2)

This register sets Operation Time (PreCounter) of Alarm2.

It takes time to reflect a new Alarm Operation time. During reflecting, do not update the Alarm Operation time. You can check whether it is in the process of reflecting by using **Busy**.

- bit[16] : Busy (SetAlmPreCnt2 Write Busy status)

When **Busy** indicates “1”, the register is reflecting Alarm Operation time (means that

SetAlm(Post/Pre)Cnt2 must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: Alarm Operation time is not set or reflected completely.
1	Reading 1: Alarm Operation time is being reflected. SetAlm(Post/Pre)Cnt2 must not be written.

3.6.5.2.20 AlmClr(0x70)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														Err Flg1	Err Flg0
-														WO	WO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													Flg2	Flg1	Flg0
-													WO	WO	WO

When an Alarm occurs, an Alarm Interrupt is asserted (set). When a Clear Register is written, the Alarm Interrupt can be deasserted (reset) instantly.

- **bit[0] : Flg0 (Clear of Normal Alarm Flag0)**

When you write “1” on AlmClr.Flg0, Normal Alarm0 Interrupt is deasserted, and Normal Alarm Flag0 is cleared.

Flg0	Description of Functions
0	Writing 0: invalid
1	Writing 1: deasserts Normal Alarm Flag0 When Normal Alarm Flag0 is deasserted, this register is cleared to “0” automatically.

- **bit[1] : Flg1 (Clear of Normal Alarm Flag1)**

Flg1	Description of Functions
0	Writing 0: invalid
1	Writing 1: deasserts Normal Alarm Flag1 When Normal Alarm Flag1 is deasserted, this register is cleared to “0” automatically.

- **bit[1] : Flg1 (Clear of Alarm Flag2)**

Flg2	Description of Functions

0	Writing 0: invalid
1	Writing 1: deasserts Normal Alarm Flag2 When Normal Alarm Flag2 is deasserted, this register is cleared to “0” automatically.

- bit[16] : ErrFlg0 (Clear of Error Alarm Flag0)

When you write “1” on **AlmClr.Flgl0**, Error Alarm0 Interrupt is deasserted, and Error Alarm Flag0 is cleared.

ErrFlg0	Description of Functions
0	Writing 0: invalid
1	Writing 1: deasserts Interrupt of Error Alarm Flag0 When Error Alarm Flag0 is deasserted, this register is cleared to “0” automatically.

- bit[17] : ErrFlg1 (Clear of Error Alarm Flag1)

ErrFlg1	Description of Functions
0	Writing 0: invalid
1	Writing 1: deasserts Interrupt of Error Alarm Flag1 When Error Alarm Flag1 is deasserted, this register is cleared to “0” automatically.

3.6.5.2.21 AlmOutEn0(0x74)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Err	Reserved														Err
Dbg															En
RO	-														RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg	Reserved						Busy	Reserved						En	
RO	-						RO	-						RW	

bit[0] : En (Enable Signal for Normal Alarm0 Interrupt)

This register does the settings for notifying processor of Normal Alarm Flag0.

It takes time to reflect the settings. During reflecting, do not update the settings. You can check whether it is in the process of reflecting by using **Busy**.

En	Description of Functions
0	Writing 0: disables an interrupt request to processor. Even if conditions are met, interrupt will be deasserted.
1	Writing 1: enables an interrupt request to processor.

	If conditions are met, interrupt will be asserted.

If 1'b0 is set on En, an interrupt request is disabled. However, status register AlmFlg.Flg0 transitions to 1'b1 if conditions are met.

- bit[8] : Busy (Write Busy Status)

This register indicates how far **AlmOutEn0** register is reflected.

When **Busy** indicates “1”, the register is reflecting Enable Signal (means that **AlmOutEn0** must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: AlmOutEn0 is not set or reflected completely.
1	Reading 1: AlmOutEn0 is being reflected. AlmOutEn0 must not be written.

- bit[15] : Dbg (Enable Signal Value for current Normal Alarm0 Interrupt)

This register is used for debugging. By reading this register, you can see Enable Signal value for the Normal Alarm0 Interrupt that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **AlmOutEn0.En** or not.

- bit[16] : ErrEn (Enable Signal for Error Alarm0 Interrupt)

This register does the settings for notifying processor of Error Alarm Flag0.

ErrEn	Description of Functions
0	Writing 0: disables an interrupt request to processor. Even if conditions are met, interrupt will be deasserted.
1	Writing 1: enables an interrupt request to processor. If conditions are met, interrupt will be asserted.

If 1'b0 is set on ErrEn, an interrupt request is disabled. However, status register AlmFlg.ErrFlg0 transitions to 1'b1 if conditions are met.

- bit[31] : ErrDbg (Enable Signal Value for current Error Alarm0 Interrupt)

This register is used for debugging. By reading this register, you can see Enable Signal value for the Error Alarm0 Interrupt that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **AlmOutEn0.ErrEn** or not.

3.6.5.2.22 **AlmOutEn1(0x78)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Err	Reserved														Err
Dbg															En
RO	-														RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg	Reserved						Busy	Reserved							En
RO	-						RO	-							RW

- bit[0] : En (Enable Signal for Normal Alarm1 Interrupt)

This register does the settings for notifying processor of Normal Alarm Flag1.

It takes time to reflect the settings. During reflecting, do not update the settings. You can check whether it is in the process of reflecting by using **Busy**.

En	Description of Functions
0	Writing 0: disables an interrupt request to processor. Even if conditions are met, interrupt will be deasserted.
1	Writing 1: enables an interrupt request to processor. If conditions are met, interrupt will be asserted.

If 1'b0 is set on En, an interrupt request is disabled. However, status register AlmFlg.Flg1 transitions to 1'b1 if conditions are met.

- bit[8] : Busy (Write Busy Status)

This register indicates how far **AlmOutEn1** register is reflected.

When **Busy** indicates “1”, the register is reflecting Enable Signal (means that **AlmOutEn1** must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: AlmOutEn1 is not set or reflected completely.
1	Reading 1: AlmOutEn1 is being reflected. AlmOutEn1 must not be written.

- bit[15] : Dbg (Enable Signal Value for current Normal Alarm1 Interrupt)

This register is used for debugging. By reading this register, you can see Enable Signal value for the Normal Alarm1 Interrupt that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **AlmOutEn1.En** or not.

- bit[16] : ErrEn (Enable Signal for Error Alarm1 Interrupt)

This register does the settings for notifying processor of Error Alarm Flag1.

ErrEn	Description of Functions
0	Writing 0: disables an interrupt request to processor. Even if conditions are met, interrupt will be deasserted.
1	Writing 1: enables an interrupt request to processor. If conditions are met, interrupt will be asserted.

If 1'b0 is set on ErrEn, an interrupt request is disabled. However, status register AlmFlg.ErrFlg1 transitions to 1'b1 if conditions are met.

- bit[31] : ErrDbg (Current Enable Signal Value)

This register is used for debugging. By reading this register, you can see Enable Signal value for the Error Alarm1 Interrupt that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **AlmOutEn1.ErrEn** or not.

3.6.5.2.23 **AlmOutEn2(0x7C)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg	Reserved						Busy	Reserved						En	
RO	-						RO	-						RW	

- bit[0] : En (Enable Signal for Normal Alarm2 Interrupt)

This register does the settings for notifying processor of Normal Alarm Flag2.

It takes time to reflect the settings. During reflecting, do not update the settings. You can check whether it is in the process of reflecting by using **Busy**.

En	Description of Functions
0	Writing 0: disables an interrupt request to processor. Even if conditions are met, interrupt will be deasserted.
1	Writing 1: enables an interrupt request to processor. If conditions are met, interrupt will be asserted.

If 1'b0 is set on En, an interrupt request is disabled. However, status register AlmFlg.Flg2 transitions to 1'b1 if conditions are met.

- bit[8] : Busy (Write Busy Status)

This register indicates how far AlmOutEn2 register is reflected.

When **Busy** indicates “1”, the register is reflecting Enable Signal (means that **AlmOutEn2** must not be updated). Once the reflection is completed, **Busy** becomes “0” automatically.

Busy	Description of Functions
0	Reading 0: AlmOutEn2 is not set or reflected completely.
1	Reading 1: AlmOutEn2 is being reflected. AlmOutEn2 must not be written.

- bit[15] : Dbg (Enable Signal Value for current Normal Alarm2 Interrupt)

This register is used for debugging. By reading this register, you can see Enable Signal value for the Normal Alarm2 Interrupt that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **AlmOutEn2.En** or not.

3.6.5.2.24 **AlmFlg(0x80)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														Err Flg1	Err Flg0
-														RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													Flg2	Flg1	Flg0
-													RO	RO	RO

By reading this register, you can see Normal Alarm and Error Alarm Flag (Alarm Interrupt value before controlling registers Enabled or Disabled by using AlmOutEn). When the conditions are as described in the Table RTC-68 below, an Alarm occurs. When the Alarm is asserted, **AlmFlg** becomes “1”. If you want to clear **AlmFlg** to “0”, write “1” on **AlmClr**.

Table RTC-68 Alarm Occurrence Condition

Register	Alarm Occurrence Condition
Flg0	when set value of Alarm0 matches RTC Counter value
Flg1	when set value of Alarm1 matches RTC Counter value
Flg2	when time passes to the set value of Alarm2, based on the RTC Counter value at the time of being written on SetAlmPreCnt2
ErrFlg0	when set value of Alarm0 at the time of being written on SetAlmPreCnt0 is smaller than RTC Counter value
ErrFlg1	when set value of Alarm1 at the time of being written on SetAlmPreCnt1 is smaller than RTC Counter value

Note:

RTC Counter={PostCounter[31:0], PreCounter[14:0] }

Set value of Alarm{0,1,2}= {SetAlmPostCnt{0,1,2} [31:0], SetAlmPreCnt{0,1,2} [14:0] }

- bit[0] : Flg0 (Normal Alarm Flag0)

Flg0	Description of Functions
0	Normal Alarm0 Interrupt is deasserted.
1	Normal Alarm0 Interrupt is asserted.

- bit[1] : Flg1 (Normal Alarm Flag1)

Flg1	Description of Functions
0	Normal Alarm1 Interrupt is deasserted.

1	Normal Alarm1 Interrupt is asserted.

- bit[2] : Flg2 (Normal Alarm Flag2)

Flg2	Description of Functions
0	Normal Alarm2 Interrupt is deasserted.
1	Normal Alarm2 Interrupt is asserted.

- bit[0] : ErrFlg0 (Error Alarm Flag0)

Flg0	Description of Functions
0	Error Alarm0 Interrupt is deasserted.
1	Error Alarm0 Interrupt is asserted.

- bit[1] : ErrFlg1 (Error Alarm Flag1)

Flg1	Description of Functions
0	Error Alarm1 Interrupt is deasserted.
1	Error Alarm1 Interrupt is asserted.

3.6.5.2.25 DbgSetAlmPostCnt0(0x90)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dbg															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg															
RW															

- bit[31:0] : Dbg[31:0] (Current SetAlmPostCnt0 value)

This register is used for debugging. By reading this register, you can see **SetAlmPostCnt0** value that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **SetAlmPostCnt0** or not.

3.6.5.2.26 DbgSetAlmPreCnt0(0x94)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Dbg														
-	RW														

- bit[14:0] : Dbg[14:0] (Current SetAlmPreCnt0 value)

This register is used for debugging. By reading this register, you can see **SetAlmPreCnt0** Value that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **SetAlmPreCnt0** or not.

3.6.5.2.27 DbgSetAlmPostCnt1(0x98)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dbg															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg															
RW															

- bit[31:0] : Dbg[31:0] (Current SetAlmPostCnt1 value)

This register is used for debugging. By reading this register, you can see **SetAlmPostCnt1** value that is currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **SetAlmPostCnt1** or not.

3.6.5.2.28 DbgSetAlmPreCnt1(0x9C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Dbg														
-	RW														

- bit[14:0] : Dbg[14:0] (Current SetAlmPreCnt1 value)

This register is used for debugging. By reading this register, you can see **SetAlmPreCnt1** value that is

currently used in RTC. By using this register, you can check whether the set value has been normally reflected on **SetAlmPreCnt1** or not.

3.6.5.2.29 DbgSetAlmPostCnt2(0xA0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dbg															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dbg															
RW															

- bit[31:0] : Dbg[31:0] (Current **SetAlmPostCnt2** value)

This register is used for debugging. By reading this register, you can see comparison value of PostCounter for Alarm2 that is currently used in RTC. (means current **SetAlmPostCnt2** plus RTC Counter value at the time when **SetAlmPreCnt2** was written).

By using this register, you can check whether the set value has been normally reflected on **SetAlmPostCnt2** or not.

3.6.5.2.30 DbgSetAlmPreCnt2(0xA4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Pre														
-	RW														

- bit[14:0] : Dbg[14:0] (Current **SetAlmPreCnt2** Value)

This register is used for debugging. By reading this register, you can see comparison value of PostCounter for Alarm2 that is currently used in RTC. (means current **SetAlmPreCnt2** plus RTC Counter value at the time when **SetAlmPreCnt2** was written)

By using this register, you can check whether the set value has been normally reflected on **SetAlmPreCnt2** or not.

3.6.5.2.31 **CntUpdateClr(0xB0)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Flg
-															WO

When RTC Counter has been updated completely, the interrupt flag notifying that RTC Counter has been updated is asserted (set). If Clear Register is written, the interrupt flag can be deasserted (reset) instantly.

As for conditions that the interrupt flag notifying that RTC Counter has been updated is asserted, refer to **CntUpdateFlg(0xB8)**

- bit[0] : Flg (Clear of the interrupt flag notifying that RTC Counter has been updated)

When you write “1” on **CntUpdateClr.Flg**, the interrupt flag notifying that RTC Counter has been updated is deasserted and cleared to “0”.

Flg	Description of Functions
0	Writing 0: invalid
1	Writing 1: deasserts interrupt flag notifying that RTC Counter has been updated

3.6.5.2.32 **CntUpdateEn(0xB4)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															En
-															RW

- bit[0] : En (Enable Signal for the interrupt flag notifying that RTC Counter has been updated)

This register does the settings for notifying processor that RTC Counter has been updated.

En	Description of Functions
0	Writing 0: disables an interrupt request to processor.
1	Writing 1: enables an interrupt request to processor.

3.6.5.2.33 **CntUpdateFlg(0xB8)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Flg
-															RO

By reading this register, you can see the interrupt flag notifying that RTC Counter has been updated (Interrupt value before being controlled Enabled or Disabled by CntUpdateEn). If RTC Counter is updated under the following conditions, **CntUpdateFlg** becomes “1”. If you want to clear **CntUpdateFlg** to “0”, write “1” on **CntUpdateClr**.

- [Update of RTC Counter value](#)
- [Synchronization of external RTC](#)
- [Synchronization between internal RTCs](#)
- [Correction of RTC Counter value](#)

3.6.5.2.34 **DiffSignBit(0xC0)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Val
-															RO

- bit[0] : Val (sign bit of difference value from other RTC Counter)

By reading this register, you can see sign when difference (means one RTC Counter (47 bits) minus other RTC Counter (47 bits)) is calculated.

Val	Description of Functions
0	Positive
1	Negative

- Restriction on the use of this register

Check the interrupt flag notifying that RTC Counter has been updated (**CntUpdateFlg(0xB8)**) before reading **DiffSignBit**, **DiffPostCnt**, and **DiffPretCnt**.

3.6.5.2.35 **DiffPostCnt(0xC4)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Val															
RW															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Val															
RW															

- bit[31:0] : Val[31:0] (Difference from other RTC Counter value)

By reading this register, you can see higher 32 bits of the difference (47 bits) (means one RTC Counter (47 bits) minus other RTC Counter (47 bits)).

3.6.5.2.36 **DiffPreCnt (0xC8)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Val														
-	RW														

- bit[14:0] : Val[14:0] (Difference from other RTC Counter value)
By reading this register, you can see lower 15 bits of the difference (47 bits) (means one RTC Counter (47 bits) minus other RTC Counter (47 bits)).

3.6.5.2.37 **RTC0_RTC_CTL (0x04100730)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CLK NEG EDG E_EN	Reserved		SYNC_SEL		Reserved			EXT AL M_P OL	Reserved		EXTALM_SEL	
			RW								RW				
-			RW	-		RW		-			RW	-		RW	

- bit[1:0] : EXTALM_SEL [1:0] (External Alarm Output Select Signal)
This register selects one AlarmFlag from AlarmFlag0, AlarmFlag1, and AlarmFlag2 as an Alarm output outside (RTC0_ExtAlm).

EXTALM_SEL	Description of Functions
0	AlarmFlag0(AlmFlg,Flg0) is used as an External Output Alarm (RTC0_ExtAlm).
1	AlarmFlag1(AlmFlg,Flg1) is used as an External Output Alarm (RTC0_ExtAlm).
2	AlarmFlag2(AlmFlg,Flg2) is used as an External Output Alarm (RTC0_ExtAlm).
3	0 is output as an External Output Alarm (RTC0_ExtAlm). (When EXTALM_POL indicates "0")

EXTALM_SEL	Description of Functions
1	1 is output as an External Output Alarm (RTC0_ExtAlm). (When EXTALM_POL indicates "1")

- bit[4] : EXTALM_POL (External Alarm Output Select Signal)

This register sets signal logic (positive logic or negative logic) of External Output Alarm.

EXTALM_POL	Description of Functions
0	outputs an External Output Alarm (RTC0_ExtAlm) signal in positive logic
1	outputs an External Output Alarm (RTC0_ExtAlm) signal in negative logic

- bit[9:8] : SYNC_SEL [1:0] (External Alarm Output Select Signal)

This register selects one Alarm used as a trigger of Time Synchronization.

EXTALM_SEL	Description of Functions
0	RTC0_ExtAlm is used as a trigger of Time Synchronization.
1	RTC1_ExtAlm is used as a trigger of Time Synchronization.
2	When IOCSYS_IOMD0.PMIC_INT indicates 2, this alarm is used. For details, refer to Chapter 3.1.4.3.2.
3	When IOCSYS_IOMD0.PMIC_INT indicates 3, this alarm is used. For details, refer to Chapter 3.1.4.3.3.

- bit[12] : CLKNEGEDGE_EN (Inverted Clock Setting)

By using this register, External Output Alarm and Time Synchronization Trigger Signal are set whether to synchronize at the falling edge of the clock.

EXTALM_POL	Description of Functions
0	External Output Alarm and Time Synchronization are performed at the rising edge of the clock. External Output Alarm and Time Synchronization Trigger Signal synchronize to usual clock.
1	External Output Alarm and Time Synchronization are performed at the falling edge of the clock. External Output Alarm and Time Synchronization Trigger Signal synchronize to inverted clock (falling edge of the usual clock).

3.6.5.2.38 RTC1_RTC_CTL (0x04100730)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
-															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CLK NEG EDG E_E N	Reserved		SYNC_SEL		Reserved			EXT AL M_P OL	Reserved		EXTALM_S EL	
			RW								RW				
-				-		RW		-				-		RW	

- bit[1:0] : EXTALM_SEL [1:0] (External Alarm Output Select Signal)

This register selects one AlarmFlag from AlarmFlag0, AlarmFlag1, and AlarmFlag2 as an Alarm output outside (RTC1_ExtAlm).

EXTALM_SEL	Description of Functions
0	AlarmFlag0 is used as an External Output Alarm (RTC1_ExtAlm).
1	AlarmFlag1 is used as an External Output Alarm (RTC1_ExtAlm).
2	AlarmFlag2 is used as an External Output Alarm (RTC1_ExtAlm).
3	0 is output as an External Output Alarm (RTC0_ExtAlm). (When EXTALM_POL indicates “0”) 1 is output as an External Output Alarm (RTC0_ExtAlm). (When EXTALM_POL indicates “1”)

- bit[4] : EXTALM_POL (External Alarm Output Select Signal)

This register sets signal logic (positive logic or negative logic) of External Output Alarm.

EXTALM_POL	Description of Functions
0	outputs an External Output Alarm (RTC1_ExtAlm) signal using positive logic
1	outputs an External Output Alarm (RTC1_ExtAlm) signal using negative logic

- bit[9:8] : SYNC_SEL [1:0] (External Alarm Output Select Signal)

This register selects one Alarm used as a trigger of Time Synchronization.

EXTALM_SEL	Description of Functions
0	RTC0_ExtAlm is used as a trigger of Time Synchronization.

EXTALM_SEL	Description of Functions
1	RTC1_ExtAlm is used as a trigger of Time Synchronization.
2	This alarm is used when IOCSYS_IOMD0.PMIC_INT indicates 2. For details, refer to Chapter 3.1.4.3.2.
3	This alarm is used when IOCSYS_IOMD0.PMIC_INT indicates 3. For details, refer to Chapter 3.1.4.3.3.

- bit[12] : CLKNEGEDGE_EN (Inverted Clock Setting)

By using this register, External Output Alarm and Time Synchronization Trigger Signal are set whether to synchronize at the falling edge of the clock.

EXTALM_POL	Description of Functions
0	External Output Alarm and Time Synchronization are performed at the rising edge of the clock. External Output Alarm and Time Synchronization Trigger Signal synchronize to usual clock (rising edge of the clock).
1	External Output Alarm and Time Synchronization are performed at the falling edge of the clock. External Output Alarm and Time Synchronization Trigger Signal synchronize to inverted clock (falling edge of the usual clock).

3.6.5.3 Control Flow

3.6.5.3.1 Update of RTC Counter Value

This function is used when you reflect values, which are set by registers, on RTC Counter value (PostCounter[31:0], PreCounter[14:0]). The sequence is as follows.

1. On **WrRegPostCnt** register, write a value that you want to reflect on PostCounter.
2. On **WrRegPreCnt** register, write a value that you want to reflect on PreCounter.
3. Write “1” on WrRegReq.BusyA register.

You can check whether RTC Counter value has been updated in the following two ways.

- performing polling to **WrRegReq.BusyA** until it returns to “0”
- receiving interrupt request CntUpdateFlg which means that RTC Counter has been updated

3.6.5.3.2 Correction of RTC Counter Value

This function is used to correct RTC Counter values. You can set corrected RTC Counter values by providing current RTC Counter value with relative values. The sequence is as follows.

1. Write a correction value on **OffsetVal** register.

Correction values must be written with two's complements.

2. Write “1” on OffsetReq.BusyA register.

You can check whether RTC Counter value has been corrected in the following two ways.

- performing polling to **OffsetReq.BusyA** until it returns to “0”.
- receiving interrupt request **CntUpdateFlg** which means that RTC Counter has been updated

3.6.5.3.3 Synchronization of External RTC

Synchronization of External RTC is a function that sets time of RTC inside CXD5602 by receiving interrupts from outside including PMIC (PMIC_INT).

Synchronizing CXD5602 with CXD5247

The sequence when CXD5602 (hereinafter called the LSI) is synchronized with CXD5247 (hereinafter called the PMIC) is described below. As frequency and synchronizing timing depend on connected PMIC setting, adjust the time to synchronize in accordance with PMIC.

1. PMU confirms RTC Counter value of PMIC.
2. Set the time when PMIC outputs External Alarm Flag (Interrupt from PMIC_INT).
For example, when the time that you want to synchronize is Y[46:0], set Y[46:6]-1 as the time that External Alarm Flag is output.
(Y must be future time value compared with the RTC Counter value that was confirmed in 1 above.)
3. On WrReg(Post/Pre)Cnt register, write the time Y[46:0]+0x3+Δ that synchronizes with internal RTC. Δ is a difference between the LSI and the PMIC. For details, refer to chapter “Difference Calculation between CXD5602 and CXD5247”.

When Δ is 0x0, calculate the formula replacing the Δ with 0x40. When the synchronization is performed between internal RTCs, calculate the formula replacing the Δ with 0x40 at all times.

The following are examples of setting synchronizing internal RTC with external RTC.

Table RTC-69 Examples of Setting Synchronizing Internal RTC with External RTC Synchronization Setting

Desired Time for Synchronization Y[46:0]	Output Time of External Alarm Flag Y[46:6]-1	Difference Δ between the LSI and PMIC 0x00 ~ 0x3F	RTC Synchronization Time Setting for the LSI (WrReg(Post/Pre)Cnt) Y[46:0]+0x03+ Δ
0x100	0x3	0x00	0x143 (= 0x100 + 0x03 + 0x40)
		0x01	0x104 (= 0x100 + 0x03 + 0x01)
		0x02	0x105 (= 0x100 + 0x03 + 0x02)
		...	...
		0x3E	0x141 (= 0x100 + 0x03 + 0x3E)
		0x3F	0x142 (= 0x100 + 0x03 + 0x3F)
0x140	0x4	0x00	0x183 (= 0x140 + 0x03 + 0x40)
		0x01	0x144 (= 0x140 + 0x03 + 0x01)
		0x02	0x145 (= 0x140 + 0x03 + 0x02)
		...	...
		0x3E	0x181 (= 0x140 + 0x03 + 0x3E)
		0x3F	0x182 (= 0x140 + 0x03 + 0x3F)

4. Write “1” on WrIntCtrl.Busy register.

Receiving PMIC External Alarm from PMIC_INT, synchronization between RTC in the PMIC and RTC in the CXD5602 will be completed on the time (Y[46:6]-1) designated in 2 above. Once synchronization has been completed, **WrIntCtrl.Busy** becomes “0”.

WrRegPostCnt value is reflected on PostCounter, and **WrRegPreCnt** value is reflected on PreCounter.

By using interrupt CntUpdateFlg notifying that RTC Counter has been updated, you can check whether the synchronization has been completed or not.

5. Clear PMIC External Alarm Flag.

Synchronizing CXD5247 with CXD5602

The following is the synchronization sequence when CXD5602 (hereinafter called LSI) is combined with CXD5247 (hereinafter called PMIC).

1. Read RTC Counter value of the LSI by using Rt(Post/Pre)Cnt.

Set the time when Interrupt is output to PMIC by using RTCx_ExtAlm (hereinafter called External Output Alarm).

For alarm time setting, refer to “Alarm Output Setting”, and for Output Selection of External Output Alarm, refer to “**RTC0_RTC_CTL (0x04100730)**.”

If you want to synchronize the value of CXD5602 with CXD5247 when the value of {PostCounter[31:0],PreCounter[14:0]} has reached X[46:0], the time to output External Output Alarm to CXD5247 will be set as follows:

For example, when EXTALM_SEL is set as 2, the setting value of {SetAlmPostCnt2[31:0],SetAlmPreCnt2[14:0]} will be upper 41 bits = X[46:6]-1, and lower 6 bits = 0x3F. X must be future time value compared with RTC Counter value read out in 1 above.

Note:

The followings are settings of External Output Alarm synchronized with X[46:0]=0xFFFC00

- Time to output
 - Time to output: [46:6]=X[46:6]-1=0x3FFF-0x1=0x3FFE
 - Time to output: [5:0]= 0x3F
 - Setting of time to output External Output Alarm (when Normal Alarm0 is used)
 - SetAlmPostCnt0[31:0]= Time to output [46:15]=0x1F
 - SetAlmPreCnt0[14:0]= Time to output [14:0]=0x7FBF
2. On PMIC, set the time X[46:6]+3, which the PMIC is synchronized with the RTC of the LSI.
- At the set time described in 2 above, RTC inside the LSI outputs External Alarm Flag to PMIC, and synchronization of PMIC with the LSI is completed.

Difference Calculation between CXD5602 and CXD5247

RTC of CXD5602 operates at 32.7 kHz clock frequency. Meanwhile, RTC of CXD5247 operates at 512 Hz clock frequency. For this reason, there might be time difference between the PMIC and the LSI when CXD5247 (hereinafter called PMIC) is synchronized with CXD5602 (hereinafter called LSI). Accordingly, calculate the difference Δ in advance. Then, set the time for the synchronization taking into account it. How to calculate the difference Δ is shown below.

1. Set the time that External Alarm Flag is output from PMIC to the LSI using the offset time.
PMIC will output External Alarm Flag to the LSI at the set time.
2. Right after receiving External Alarm Flag, the LSI reads RTC Counter value inside RTC by using **Rt(Post/Pre)Cnt**.
3. Hold the lower 6 bits of **RtPreCnt** as difference Δ between PMIC and the LSI.
Hold difference Δ in Flash Memories or the like before getting into Deep Sleep mode.
4. Clear the PMIC External Alarm Flag.

3.6.5.3.4 Synchronization Between Internal RTCs

This function is used when synchronization of time counter value is performed between RTC0 and RTC1. When a synchronization request is issued to one RTC, it takes in the RTC Counter value of another RTC and gets synchronized with another RTC.

When you synchronize RTC0 with RTC Counter value of RTC1, write “1” on RtcSyncReq of RTC0.

When you synchronize RTC1 with RTC Counter value of RTC0, write “1” on RtcSyncReq of RTC1.

You can check whether synchronization has been completed in the following two ways.

- polling to **WrRegReq** of one RTC, which wrote 1 on **RtcSyncReq** register, and confirming that it returns to “0”
- receiving interrupt request **CntUpdateFlg** which means that RTC has been updated

3.6.5.3.5 Alarm Output Setting

This function is used to set time for Alarm Output. The sequence is as follows taking Alarm0 as an example.

When you want to use Alarm1, read each register in the sequence replacing Flg0/En0/Cnt0 part with Flg1/En1/Cnt1. Likewise, when you want to use Alarm2, read each register in the sequence replacing Flg0/En0/Cnt0 part with Flg2/En2/Cnt2.

- When you set Alarm output time (first time)
 1. Write “1” on AlmClr.Fl0 and AlmClr.ErrFl0 registers.
Clear Normal and Error Alarm Flags to “0”.
 2. Write “1” on AlmOutEn0.En and AlmOutEn0.ErrEn registers at the same time.
Enable O(Err)Alarm0 to be output.

3. On SetAlmPostCnt0 register, write the time that you want to output an Alarm.
Make sure to write SetAlmPostCnt0 before SetAlmPreCnt0.
 4. On **SetAlmPreCnt0** register, write the time that you want to output an Alarm.
An Alarm is output at the time set in 3 and 4 above.
You can check whether an Alarm has been output in the following two ways.
 - performing polling to AlmFlg.Flg0 until it returns to “0”
 - receiving Alarm interrupt request
- When you output an Alarm again
 1. Write “1” on **AlmClr.Flg0** and **AlmClr.ErrFlg0** registers.
Clear Normal and Error Alarm Flags to “0”.
 2. On SetAlmPostCnt0 register, write the time that you want to output an Alarm.
 3. On SetAlmPreCnt0 register, write the time that you want to output an Alarm.
 - When you do not use Alarm anymore after outputting an Alarm
 1. Write “0” on AlmOutEn0.En and AlmOutEn0.ErrEn registers.
Disable O(Err)Alarm0 to be output.
 2. Write “1” on AlmClr.Flg0 and AlmClr.ErrFlg0 registers.
Clear Normal and Error Alarm Flags to “0”.

3.7 I2C

3.7.1 Features and Overview

This LSI integrates four I2C masters.

I2C List

- I2C0 (Power domain : PWD_SCU)
- I2C1 (Power domain : PWD_SCU)
- I2C2 (Power domain : PWD_SYSIOP_SUB)
- I2C4 (Power domain : PWD_CORE)

Transfer Rate

The maximum transfer rate of the I2C is determined by the combination of the clock selected as the clock source (SYSPLL, XOSC, RCOSC, or RTC), the X'tal Oscillator clock, and the voltage mode (High Performance mode/Low Power mode). The following table describes each combination and their maximum transfer rates.

The transfer rate also varies with the external load capacity. Here, the values are shown under an ideal state.

Table I2C-70 XOSC (26 MHz), High Performance Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	48.750	39.000	26.000	8.192	0.032768
I2C2 BCK	kbps	400	400	400	356	1.424696
I2C4 BCK	kbps	400	400	400	356	1.424696
SCU (ck_scu_pre)	MHz	-	-	13.000	8.192	0.032768
I2C0,I2C1 BCK	kbps	-	-	400	356	1.424696

Table I2C-71 XOSC (26 MHz), Low Power Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	32.500	31.200	26.000	8.192	0.032768
I2C2 BCK	kbps	400	400	400	356	1.424696
I2C4 BCK	kbps	400	400	400	356	1.424696
SCU (ck_scu_pre)	MHz	-	-	13.000	8.192	0.032768
I2C0,I2C1 BCK	kbps	-	-	400	356	1.424696

3.7.2 I2C0, I2C1

The I2C0 and I2C1 are the I2C masters and support Standard and Fast Mode. In addition to direct control from the System and I/O Processor, they can be controlled using the sequencer of the SCU, in which the use of the sequencer can reduce the load on the System and I/O Processor. Control from the System and I/O Processor and control from the sequencer are exclusive and cannot be performed simultaneously. For information on the sequencer, refer to Chapter of the SCU (3.9).

3.7.2.1 Register List

Table I2C-80 shows a register list of the I2C0 and I2C1.

Table I2C-72 I2C0 and I2C1 Register List

Address	Register Name	Type	Description	initial Value
0x0418D400 0x0418D7FC	I2C0 register (For details, refer to the API)			-
0x0418D800 0x0418DBFC	I2C1 register (For details, refer to the API)			-

3.7.2.2 Clock and Reset

Figure I2C-39 shows the clock and reset system of the I2C0 and I2C1.

Before accessing the I2C0 or I2C1 registers, make sure to set SCU_CKEN.SCU=1'b1.

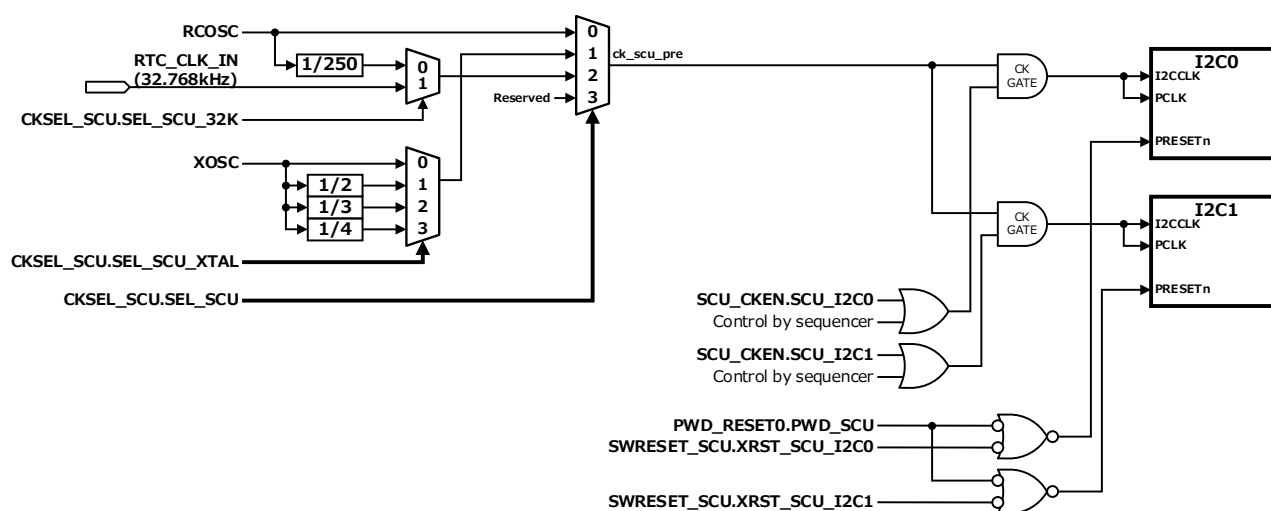


Figure I2C-39 I2C0/I2C1 Clock and Reset System

The I2C0 and I2C1 are integrated within the SCU, and clock control is possible by the System and I/O Processor or sequencer of the SCU. For clock gating control of the I2CCLK, there is control using the register and control using the sequencer, and the clock is supplied when either is in the supply setting.

The clock source can be selected from: the RCOSC; the clock generated by dividing the XOSC; the RCOSC divided by 250; or the RTC.

3.7.2.3 Clock Supply Start and Stop

3.7.2.3.1 Clock Supply Start

The following describes the method to start clock supply to the I2C0 and I2C1.

1. Clock supply start (internal circuit initialization)
SCU_CKEN.SCU_I2C0 = 1'b1
SCU_CKEN.SCU_I2C1 = 1'b1
Reads the address 0x0418D400 of I2C0 (dummy read to wait for completion of preceding setting)
Reads the address 0x0418D800 of I2C1 (dummy read to wait for completion of preceding setting)
2. Clock stop
SCU_CKEN.SCU_I2C0 = 1'b0
SCU_CKEN.SCU_I2C1 = 1'b0
Reads the address 0x0418D400 of I2C0 (dummy read to wait for completion of preceding setting)
Reads the address 0x0418D800 of I2C1 (dummy read to wait for completion of preceding setting)
3. Reset cancel
SWRESET_SCU.XRST_SCU_I2C0 = 1'b1
SWRESET_SCU.XRST_SCU_I2C1 = 1'b1
4. Clock supply start
SCU_CKEN.SCU_I2C0 = 1'b1
SCU_CKEN.SCU_I2C1 = 1'b1

3.7.2.3.2 Clock Supply Stop

The following describes the method to stop clock supply to the I2C0 and I2C1.

1. Clock stop
SCU_CKEN.SCU_I2C0 = 1'b0
SCU_CKEN.SCU_I2C1 = 1'b0

3.7.3 I2C2

The I2C2 is the I2C master and supports Standard and Fast Mode.

3.7.3.1 Register List

Table I2C-81 shows a register list of the I2C2.

Table I2C-73 I2C2 Register List

Address	Register Name	Type	Description	initial Value
0x041AA000 0x041AAFFF	I2C2 register (For details, refer to the API)			-

3.7.3.2 Clock and Reset

Figure I2C-40 shows the clock and reset system of the I2C2.

When accessing the I2C2 register, supply the clock to the AHB/APB Bus Bridge.

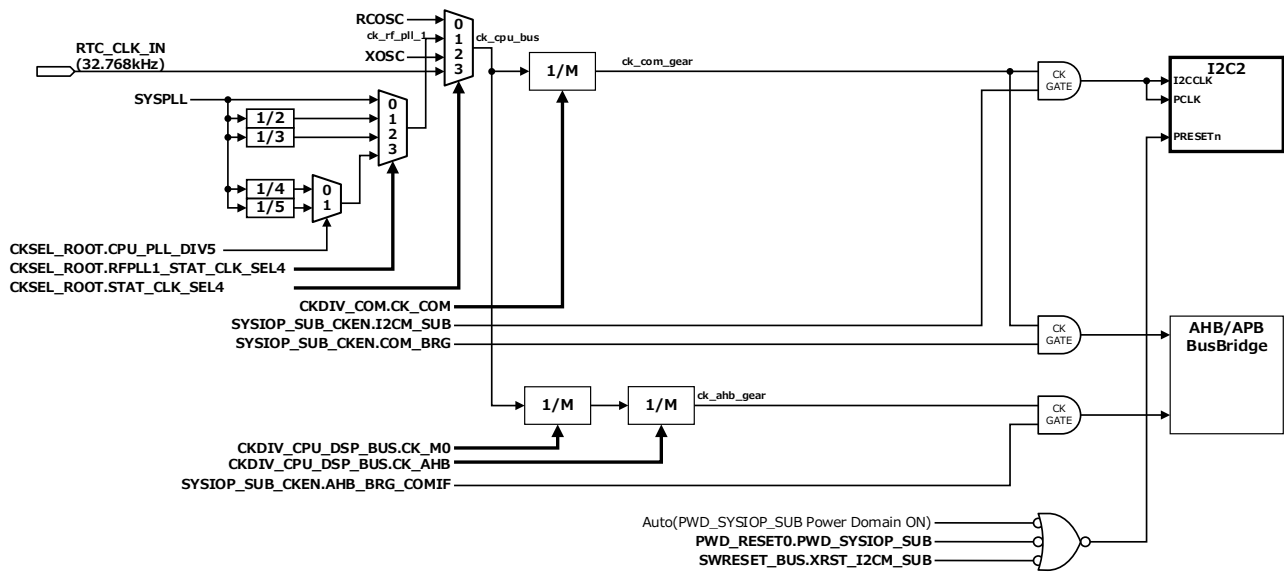


Figure I2C-40 I2C2 Clock and Reset System

3.7.3.3 Clock Supply Start and Stop

3.7.3.3.1 Clock Supply Start

The following describes the method to start clock supply to the I2C2.

1. Clock supply start of the AHB/APB Bus Bridge.
SYSIOP_SUB_CKEN.COM_BRG = 1'b1
SYSIOP_SUB_CKEN.AHB_BRG_COMIF = 1'b1
2. Clock supply start (internal circuit initialization).
SYSIOP_SUB_CKEN.I2CM_SUB = 1'b1
Reads the address 0x041AA000 of I2C2 (dummy read to wait for completion of preceding setting)
3. Clock stop
SYSIOP_SUB_CKEN.I2CM_SUB = 1'b0
Reads the address 0x041AA000 of I2C2 (dummy read to wait for completion of preceding setting)
4. Reset release
SWRESET_BUS.XRST_I2CM_SUB = 1'b1
5. Clock supply start
SYSIOP_SUB_CKEN.I2CM_SUB = 1'b1

3.7.3.3.2 Clock Supply Stop

The following describes the method to stop the clock supply to the I2C2.

1. Clock stop
SYSIOP_SUB_CKEN.I2CM_SUB = 1'b0

3.7.4 I2C4

The I2C4 is the I2C master and supports Standard and Fast Mode.

3.7.4.1 Register List

Table I2C-82 shows a register list of the I2C4.

Table I2C-74 I2C4 Register List

Address	Register Name	Type	Description	initial Value
0x04106000 0x04106FFF	I2C4 registers (For details, refer to the API)			-

3.7.4.2 Clock and Reset

Figure I2C-41 shows the clock and reset system of the I2C4.

Before accessing the I2C4 registers, make sure to set CKSEL_PMU.SEL_RTC_PCLK=1'b0 and SYSIOP_CKEN.APB=1'b1.

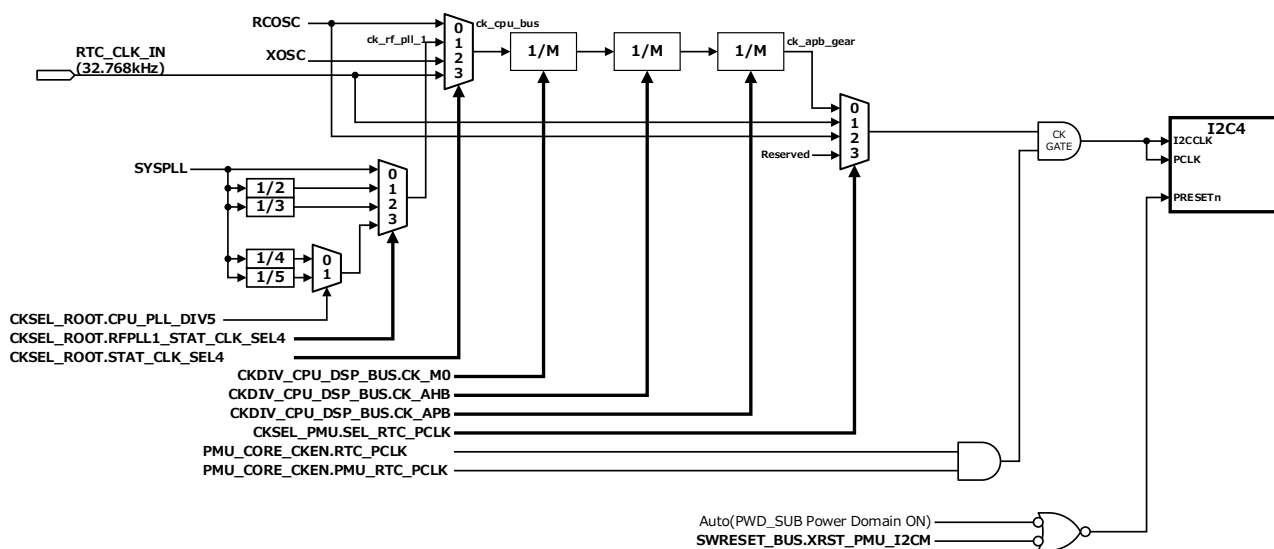


Figure I2C-41 I2C4 Clock and Reset System

3.7.4.3 Clock Supply Start and Stop

3.7.4.3.1 Clock Supply Start

The following describes the method to start clock supply to the I2C4.

1. Clock supply start (internal circuit initialization).
PMU_CORE_CKEN.RTC_PCLK = 1'b1
PMU_CORE_CKEN.PMU_RTC_PCLK = 1'b1
Reads the address 0x04106000 of I2C4 (dummy read to wait for completion of preceding setting)
2. Clock stop
PMU_CORE_CKEN.RTC_PCLK = 1'b0
PMU_CORE_CKEN.PMU_RTC_PCLK = 1'b0
Reads the address 0x04106000 of I2C4 (dummy read to wait for completion of preceding setting)
3. Reset release
SWRESET_BUS.XRST_PMU_I2CM = 1'b1
4. Clock supply start
PMU_CORE_CKEN.RTC_PCLK = 1'b1
PMU_CORE_CKEN.PMU_RTC_PCLK = 1'b1

3.7.4.3.2 Clock Supply Stop

The following describes the method to stop the clock supply to the I2C4.

1. Clock stop
PMU_CORE_CKEN.RTC_PCLK = 1'b0
PMU_CORE_CKEN.PMU_RTC_PCLK = 1'b0

3.8 DMAC

3.8.1 Overview and Features

List of DMACs

- SDMAC (Power domain: PWD_SYSIOP)
The SDMAC is for the Sensor and performs DMA transfer between the SCU and each SRAM
- HDMAC (Power domain: PWD_SYSIOP)
The HDMAC is for the HOSTIFC and performs DMA transfer between the HOSTIFC and each SRAM
- SYDMAC (Power domain: PWD_SYSIOP)
The SYDMAC is for the System and performs DMA transfer between each SRAM
- SYSUBDMAC (Power domain: PWD_SYSIOP_SUB)
The SYSUBDMAC is for the System and performs DMA transfer of each SRAM, and data store and load to/from the FLASH
- ADMAC (Power domain: PWD_APP_DSP)
The ADMAC is for the Application processor and performs DMA transfer between each SRAM
- IDMAC (Power domain: PWD_APP_SUB)
The IDMAC performs DMA transfer of the Display and Wi-Fi data

3.8.2 Function Descriptions

- SDMAC
The PrimeCell® μ DMA Controller (PL230) from ARM Limited is equipped. There are 32 channels of DMA channels. For details, refer to the PrimeCell® μ DMA Controller (PL230) Technical Reference Manual.
This Controller adds a feature to notify the CPU of independent interrupts of each DMA channel.
- HDMAC, SYDMAC, SYSUBDMAC, ADMAC
The [PrimeCell® Single Master DMA Controller \(PL081\)](#) from ARM Limited is equipped. For details, refer to the [PrimeCell® Single Master DMA Controller \(PL081\)](#) Technical Reference Manual.
This Controller adds a feature to notify the CPU of independent interrupts of each DMA channel.
- IDMAC
The functions have been modified based on the PrimeCell® DMA Controller (PL080) from ARM Limited.

Table DMAC-83 shows the DMA request bit assignment for Memory-to-peripheral transfer and Peripheral-to-memory transfer of each DMAC. The ADMAC supports Memory-to-memory transfer only.

Table DMAC-75 DMA Request Bit Assignment

Request Bit	SDMAC	HDMAC	SYDMAC	SYSUBDMAC	ADMAC	IDMAC
[0]	SPI3 TX	I2C3 TX	Reserved	Reserved	Reserved	UART2 TX
[1]	SPI3 RX	I2C3 RX	Reserved	Reserved	Reserved	UART2 RX
[2]	I2C0 TX	SPI2 TX	Reserved	I2C2 TX	Reserved	SPI4 TX
[3]	I2C0 RX	SPI2 RX	Reserved	I2C2 RX	Reserved	SPI4 RX
[4]	I2C1 TX	HOSTIFC	Reserved	UART1 TX	Reserved	SPI5 TX
[5]	I2C1 RX	UART0 TX	Reserved	UART1 RX	Reserved	SPI5 RX
[6]	LPADC0	UART0 RX	Reserved	SPI0 TX	Reserved	Reserved
[7]	LPADC1	Reserved	Reserved	SPI0 RX	Reserved	Reserved
[8]	LPADC2	Reserved	Reserved	Reserved	Reserved	Reserved
[9]	LPADC3	Reserved	Reserved	Reserved	Reserved	Reserved
[10]	HPADC0	Reserved	Reserved	Reserved	Reserved	Reserved
[11]	HPADC1	Reserved	Reserved	Reserved	Reserved	Reserved
[12]	SCU FIFO RX(1)	Reserved	Reserved	Reserved	Reserved	Reserved
[13]	SCU FIFO RX(2)	Reserved	Reserved	Reserved	Reserved	Reserved
[14]	SCU FIFO RX(3)	Reserved	Reserved	Reserved	Reserved	Reserved
[15]	SCU FIFO RX(4)	Reserved	Reserved	Reserved	Reserved	Reserved
[16]	SCU FIFO RX(5)	-	-	-	-	-
[17]	SCU FIFO RX(6)	-	-	-	-	-
[18]	SCU FIFO RX(7)	-	-	-	-	-
[19]	SCU FIFO RX(8)	-	-	-	-	-
[20]	SCU FIFO RX(9)	-	-	-	-	-
[21]	SCU FIFO RX(10)	-	-	-	-	-
[22]	SCU FIFO RX(11)	-	-	-	-	-
[23]	SCU FIFO RX(12)	-	-	-	-	-
[24]	SCU FIFO RX(13)	-	-	-	-	-
[25]	SCU FIFO RX(14)	-	-	-	-	-

3.8.3 SDMAC

Adds a feature to notify the CPU of independent interrupts or each DMA channel to the PrimeCell® μ DMA Controller (PL230).

- The interrupt signal is changed from pulse to level
- The interrupt factor register (dma_done, dma_err) is added.

Figure DMAC-42 shows an overview of the independent interrupt signals of each DMA channel.

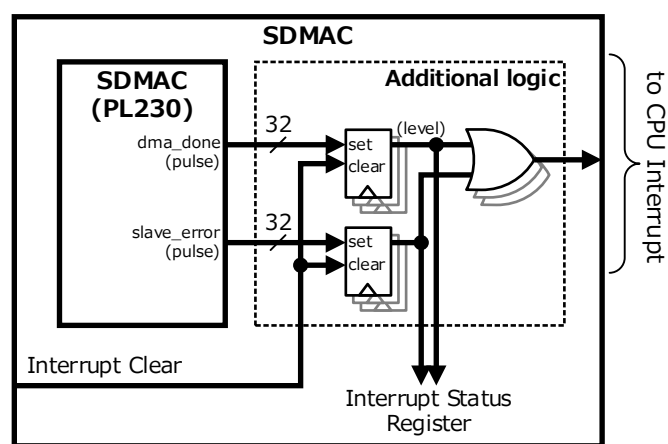


Figure DMAC-42 SDMAC Overview of Added Functions

3.8.3.1 Register List

Table DMAC-84 shows the registers that control the SDMAC.

Table DMAC-76 SDMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x04120000 0x0412004C	PrimeCell® μ DMA Controller (PL230) register			-
0x04120050	dma_done	RW	Notifies DMA transfer completion of each DMA channel	0x0
0x04120054	dma_err	RW	Notifies AHB error occurrence of each DMA channel	0x0
0x04120058 0x04120DFC	Reserved	RO	Reserved	0x0
0x04120E00 0x04120FFC	PrimeCell® μ DMA Controller (PL230) register			-

3.8.3.2 Register Descriptions

Table DMAC-85 shows descriptions of the registers added to the SDMAC.

Table DMAC-77 SDMAC Added Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04120050	dma_done	dma_done	RW	[31:0]	0x0	DMA channel number of DMA transfer completion Read as: 0: DMA transfer not completed 1: DMA transfer completed Write as: 0: No effect 1: Set dma_done LOW
0x04120054	dma_err	dma_err	RW	[31:0]	0x0	DMA channel number of AHB error occurrence Read as: 0: AHB no error occurred 1: AHB error occurred Write as: 0: No effect 1: Set dma_err LOW

3.8.3.3 Clock and Reset

Figure DMAC-43 shows the clock and reset system diagram of the SDMAC.

Reset of the SDMAC is automatically released when the PWD_SYSIOP power domain is turned ON.

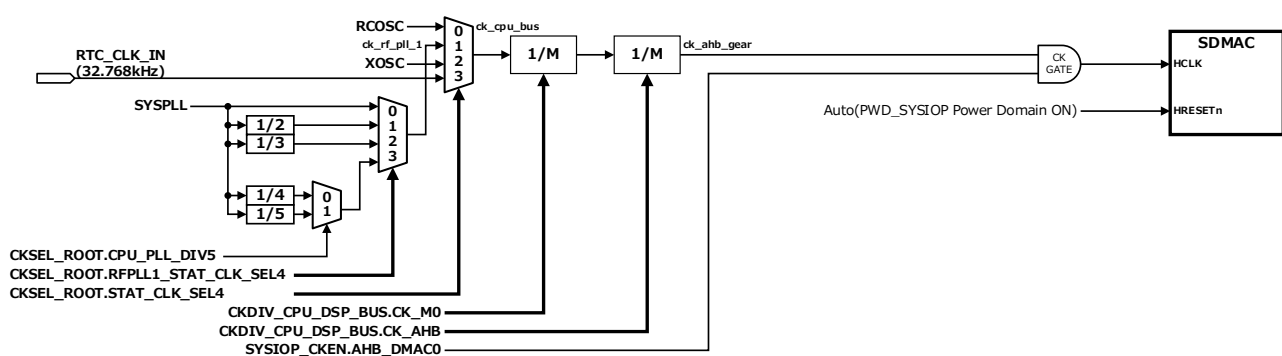


Figure DMAC-43 SDMAC Clock and Reset System

3.8.3.4 Clock Supply Start and Stop

3.8.3.4.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the SDMAC.

1. Reset release
Automatically released when the PWD_SYSIOP power domain is turned ON.
2. Clock supply start
SYSIOP_CKEN.AHB_DMAC0=1'b1

3.8.3.4.2 Clock Supply Stop

Perform the following control to stop supplying the HCLK clock of the SDMAC.

1. Clock supply stop
SYSIOP_CKEN.AHB_DMAC0=1'b0

3.8.4 HDMAC

Adds a feature to notify the CPU of independent interrupts of each DMA channel to the [PrimeCell® Single Master DMA Controller \(PL081\)](#). Figure DMAC-44 shows an overview of the added functions.

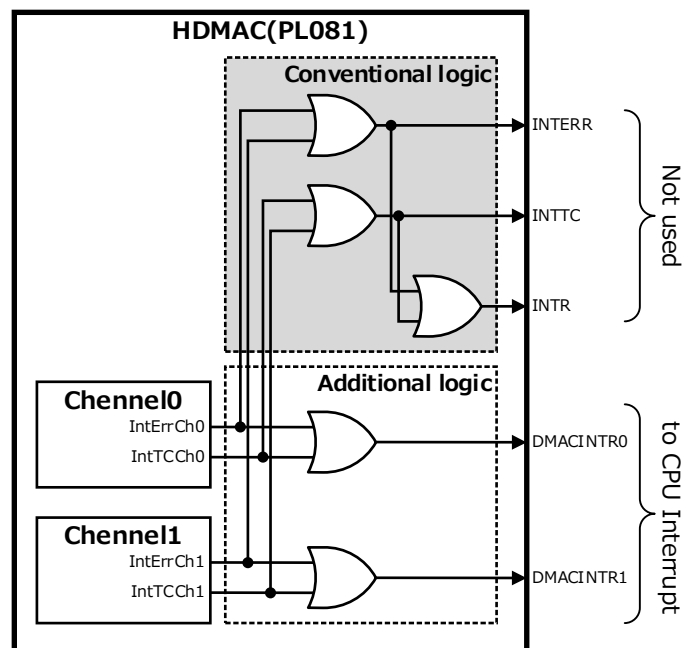


Figure DMAC-44 HDMAC Overview of Added Functions

3.8.4.1 Register List

Table DMAC-86 shows the registers that control the HDMAC.

Table DMAC-78 HDMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x04121000 0x04121FFC	PrimeCell® Single Master DMA Controller (PL081) register			-

3.8.4.2 Clock and Reset

Figure DMAC-45 shows the clock and reset system diagram of the HDMAC.

Reset of the HDMAC is automatically released when the PWD_SYSIOP power domain is turned ON.

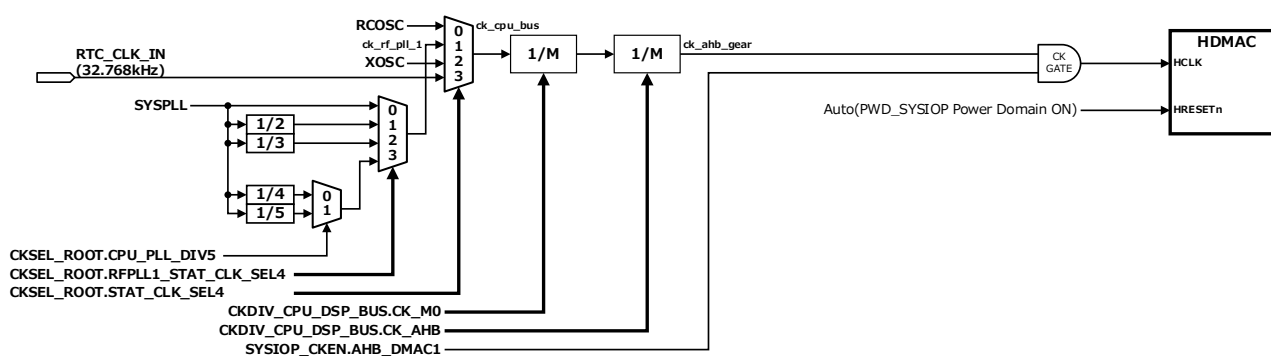


Figure DMAC-45 HDMAC Clock and Reset System

3.8.4.3 Clock Supply Start and Stop

3.8.4.3.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the HDMAC.

1. Reset release
Automatically released when the PWD_SYSIOP power domain is turned ON.
2. Clock supply start
SYSIOP_CKEN.AHB_DMACH1=1'b1

3.8.4.3.2 Clock Supply Stop

Perform the following control to stop supplying the HCLK clock of the HDMAC.

1. Clock supply stop

SYSIOP_CKEN.AHB_DMAC1=1'b0

3.8.5 SYDMAC

3.8.5.1 Register List

Table DMAC-87 shows the registers that control the SYDMAC.

Table DMAC-79 SYDMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x04122000 0x04122FFC	PrimeCell® Single Master DMA Controller (PL081) register			-

3.8.5.2 Clock and Reset

Figure DMAC-46 shows the clock and reset system diagram of the SYDMAC.

Reset of the SYDMAC is automatically released when the PWD_SYSIOP power domain is turned ON.

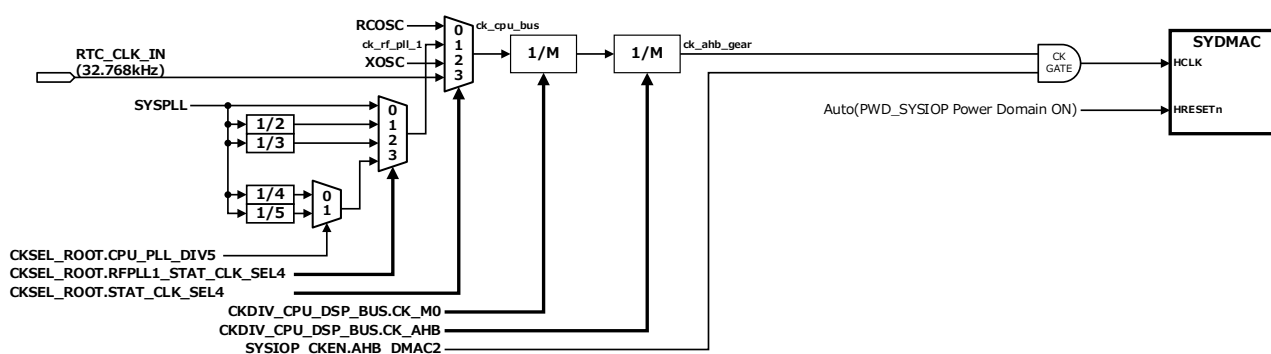


Figure DMAC-46 SYDMAC Clock and Reset System

3.8.5.3 Clock Supply Start and Stop

3.8.5.3.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the SYDMAC.

1. Reset release
Automatically released when the PWD_SYSIOP power domain is turned ON.
2. Clock supply start
SYSIOP_CKEN.AHB_DMAC2=1'b1

3.8.5.3.2 Clock Supply Stop

Perform the following control to stop supplying the HCLK clock of the SYDMAC.

1. Clock supply stop
SYSIOP_CKEN.AHB_DMAC2=1'b0

3.8.6 SYSUBDMAC

3.8.6.1 Register List

Table DMAC-88 shows the registers that control the SYSUBDMAC.

Table DMAC-80 SYSUBDMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x04123000 0x04123FFC	PrimeCell® Single Master DMA Controller (PL081) register			-

3.8.6.2 Clock and Reset

Figure DMAC-47 shows the clock and reset system diagram of the SYSUBDMAC.

Reset of the SYSUBDMAC is automatically released when the PWD_SYSIOP_SUB power domain is turned ON.

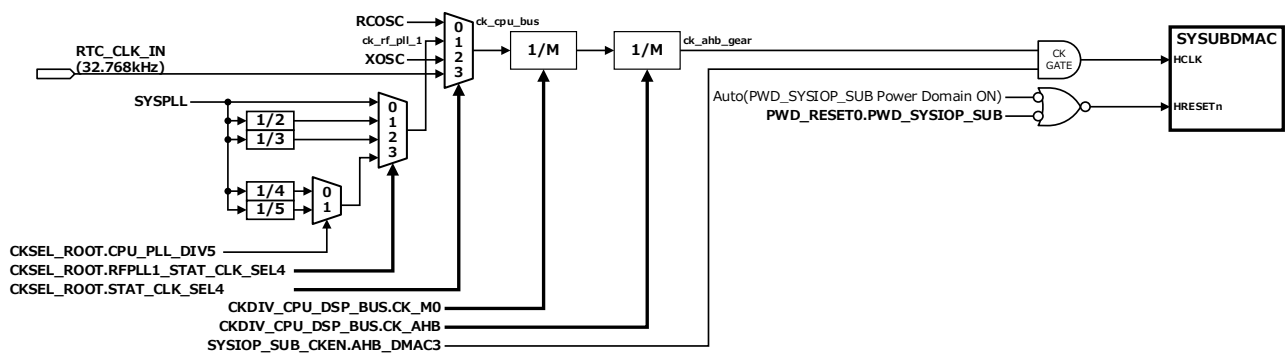


Figure DMAC-47 SYSUBDMAC Clock and Reset System

3.8.6.3 Clock Supply Start and Stop

3.8.6.3.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the SYSUBDMAC.

- 1. Reset release
Automatically released when the PWD_SYSIOP_SUB power domain is turned ON.
- 2. Clock supply start
SYSIOP_SUB_CKEN.AHB_DMAC3=1'b1

3.8.6.3.2 Clock Supply Stop

- 1. Clock supply stop
SYSIOP_SUB_CKEN.AHB_DMAC3=1'b0

3.8.7 ADMAC

3.8.7.1 Register List

Table DMAC-89 shows the registers that control the ADMAC.

Table DMAC-81 ADMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x0E020000 0x0E020FFF	PrimeCell® Single Master DMA Controller (PL081) register			-

3.8.7.2 Clock and Reset

Figure DMAC-48 shows the clock and reset system diagram of the ADMAC.

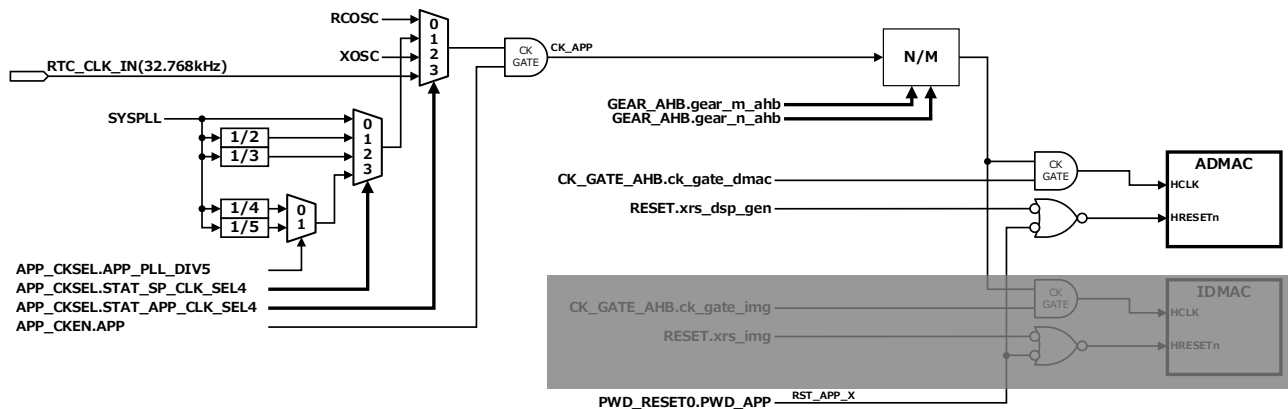


Figure DMAC-48 ADMAC Clock and Reset System

3.8.7.3 Clock Supply Start and Stop

3.8.7.3.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the ADMAC.

1. Reset release

PWD_RESET0.PWD_APP=1'b1

RESET.xrs_dsp_gen=1'b1

2. Supply the CK_APP (Refer to APP (Chapter 3.13))

3. AHB bus clock supply and division ratio setting

GEAR_AHB.gear_m_ahb= (arbitrary: denominator setting of the division ratio)

GEAR_AHB.gear_n_ahb= (arbitrary: numerator setting of the division ratio)

CK_GATE_AHB.ck_gate_dmac=1'b1

3.8.7.3.2 Clock Supply Stop

Perform the following control to stop supplying the HCLK clock of the ADMAC.

1. AHB bus clock stop

CK_GATE_AHB.ck_gate_dmac=1'b0

3.8.8 IDMAC

The functions of the IDMAC have been modified based on the PrimeCell® DMA Controller (PL080) from ARM Limited.

Features of the IDMAC

- There are five DMA channels, each of which supports unidirectional transfer.
- Accepts transfer requests from IMG_SSP and IMG_UART
- Enables single data transfer and burst data transfer. In the case of burst data transfer, the size can be set by the program
- Enables Scatter/Gather transfer by use of the linked list.
- Each channel has an independent 16 byte FIFO built in.
- Supports only little endian

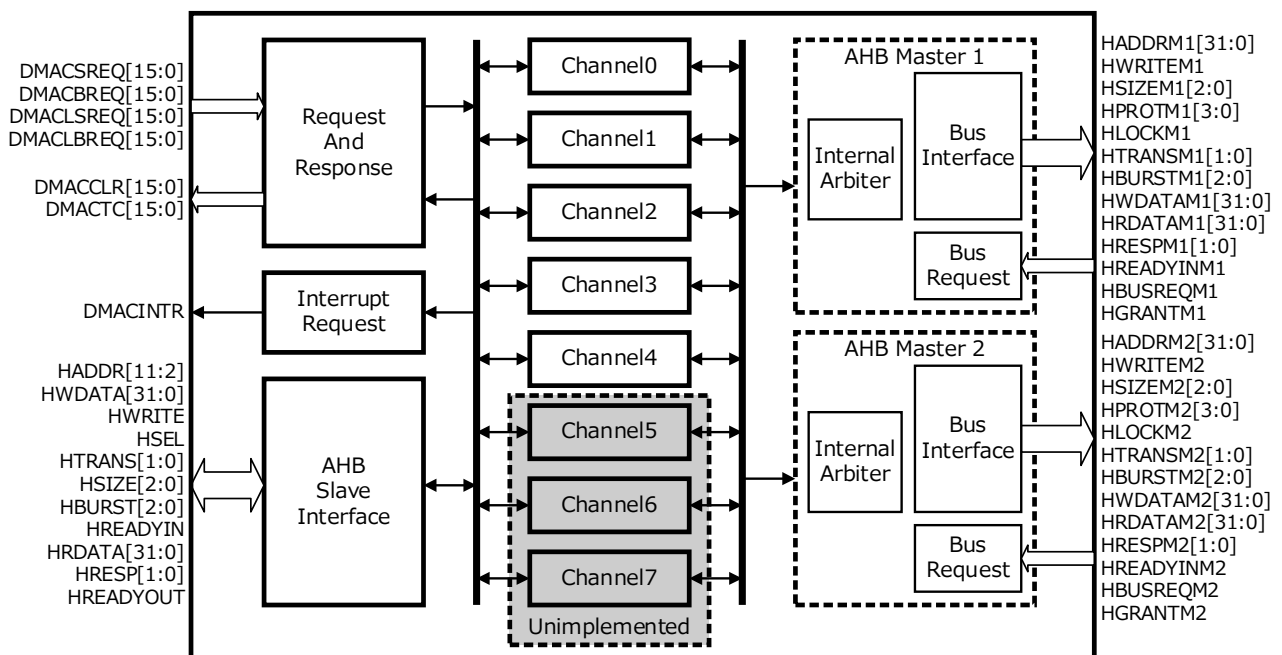


Figure DMAC-49 IDMAC Function Block Diagram

3.8.8.1 Register List

Table DMAC-8 shows the registers that control the IDMAC.

Table DMAC-8 IDMAC Control Register List

Address	Register Name	Type	Description	initial Value
0x04123000	DMACIntStatus	RO	Interrupt Status Register	0
0x04123004	DMACIntTCStatus	RO	Interrupt Terminal Count Status Register	0
0x04123008	DMACIntTCClr	W	Interrupt Terminal Count Clear Register	-
0x0412300C	DMACIntErrorStatus	RO	Interrupt Error Status Register	0
0x04123010	DMACIntErrClr	W	Interrupt Error Clear Register	-
0x04123014	DMACRawIntTCStatus	RO	Raw Interrupt Terminal Count Status Register	0
0x04123018	DMACRawIntErrorStatus	RO	Raw Error Interrupt Status Register	0
0x0412301C	DMAEnbldChns	RO	Enabled channel register	0
0x04123020	DMACSoftBReq	RW	Software burst request register	0
0x04123024	DMACSoftSReq	RW	Software single request register	0
0x04123028	DMACSoftLBReq	RW	Software last burst request register	0
0x0412302C	DMACSoftLSReq	RW	Software last single request register	0
0x04123030	DMACConfiguration	RW	Configuration register	0x0400
0x04123034	DMACSync	RW	Synchronization register	0xFFFF
0x04123038	DMACSRReqMask	RW	Single Request Mask register	0xFFFF
0x04123100	DMACSrcAddr_n (n=0-3,step=0x20)	RW	Channel source address registers	0
0x04123104	DMACDestAddr_n (n=0-3,step=0x20)	RW	Channel destination address registers	0
0x04123108	DMACLLI_n (n=0-3,step=0x20)	RW	Channel linked list item register	0
0x0412310C	DMACExtControl_n (n=0-3,step=0x20)	RW	Extended Channel Control register	0
0x04123110	DMACConfiguration_n (n=0-3,step=0x20)	RW	Channel Configuration register	0
0x04123114	DMACDefLLI_n (n=0-3,step=0x20)	RW	Channel Default Link List Item registers	0
0x04123180 0x041234FC	Reserved	RO	Reserved	0
0x04123500	DMACITCR	RW	Test Control Register	0

0x04123504	DMACITOP1	RW	Integration Test Output Register 1	0
0x04123508	DMACITOP2	RW	Integration Test Output Register 2	0
0x0412350C	DMACITOP3	RW	Integration Test Output Register 3	0
0x04123510 0x041237FC	Reserved	RO	Reserved	0
0x04123800	DMACAUX0	RW	DMAC Auxury Register 0	0
0x04123804	DMACAUX1	RW	DMAC Auxury Register 1	0
0x04123808	DMACAUX2	RW	DMAC Auxury Register 2	0
0x0412380C	DMACAUX3	RW	DMAC Auxury Register 3	0

3.8.8.2 Register Descriptions

Table DMAC-9 shows the descriptions of the registers of the IDMAC.

Table DMAC-9 IDMAC Control Register Descriptions

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04123000	DMACIntStatus	-	RO	[31:0]	0	Same as PL080
0x04123004	DMACIntTCStatus	-	RO	[31:0]	0	Same as PL080
0x04123008	DMACIntTCClr	-	W	[31:0]	-	Same as PL080
0x0412300C	DMACIntErrorStatus	-	RO	[31:0]	0	Same as PL080
0x04123010	DMACIntErrClr	-	W	[31:0]	-	Same as PL080
0x04123014	DMACRawIntTCStatus	-	RO	[31:0]	0	Same as PL080
0x04123018	DMACRawIntErrorStatus	-	RO	[31:0]	0	Same as PL080
0x0412301C	DMAEnbldChns	-	RO	[31:0]	0	Same as PL080
0x04123020	DMACSoftBReq	-	RW	[31:0]	0	Same as PL080
0x04123024	DMACSoftSReq	-	RW	[31:0]	0	Same as PL080
0x04123028	DMACSoftLBReq	-	RW	[31:0]	0	Same as PL080
0x0412302C	DMACSoftLSReq	-	RW	[31:0]	0	Same as PL080
0x04123030	DMACConfiguration Sets the operation mode of the DMA controller	Reserved	RO	[31:16]	0	Reserved
		FSIZE	RO	[15:14]	2'b00	Can read out the FIFO size of the DMAC. Takes the following values depending on the configuration of the DMAC. 0: 16 byte 1: 32 byte 2: 64 byte 3: 128 byte

		ARB	RO	[13]	1'b0	When the arbiter within the DMAC schedules the transfers (for multiple transfer requests), the scheme that determines the priority can be read out. Takes the following values depending on the configuration of the DMAC. 0: Fixed-priority 1: Round-robin		
		TR	RO	[12]	1'b0	Can read out whether or not there is a DMA external trigger function. Takes the following values depending on the configuration of the DMAC. 0: Operates without external trigger 1: Waits for external trigger		
		DLLI	RO	[11]	1'b1	Can read out whether or not there is a DefLLI function of the DMAC. Takes the following values depending on the configuration of the DMAC. 0: Disables the DefLLI function 1: Enables the DefLLI function		
		TS	RO	[10]	1'b1	Can read out whether the Channel Control register mapping of the DMAC is TransferSize expanded mapping or Default mapping. Takes the following values depending on the configuration of the DMAC. 0: The Channel Control register mapping is Default mapping 1: The Channel Control register mapping is TransferSize expanded mapping		
		Reserved	RO	[9:3]	0	Reserved		
		M2	RW	[2]	1'b0	Same as PL080		
		M1	RW	[1]	1'b0			
		E	RW	[0]	1'b0	Same as PL080		
		0x04123034	DMACSync	-	RW	[31:0]	0	Same as PL080
		0x04123038	DMACReqMask	Reserved	RO	[31:16]	0	Reserved

		DMACSR EQMASK	RW	[15:0]	0	Masks the input of the DMA data transfer request input terminal DMASREQ[15:0]. When masked, only DMABREQ[15:0] becomes valid. 0: DMASREQ input is masked 1: DMASREQ input is valid Note that the setting of this register changes the handshake method between the DMAC and Peripherals and should be used with care. When single data transfer requests are disabled, only burst requests can be accepted.
0x04123100	DMACSrcAddr_n (n=0-3,step=0x20)	SRCADD R	RW	[31:0]	0	Same as PL080
0x04123104	DMACDestAddr_n (n=0-3,step=0x20)	DESTADD R	RW	[31:0]	0	Same as PL080
0x04123108	DMACLLI_n (n=0-3,step=0x20)	-	RW	[31:0]	0	Same as PL080
0x0412310C	DMACExtControl_n (n=0-3,step=0x20) Indicates the control information of each channel's transfer size, burst size, transfer data width, etc. during the DMA data transfer. This register must be set before the corresponding DMA channel is enabled. When Scatter/Gather transfer is being performed, it will be automatically updated to the value of the corresponding linked list.	I	RW	[31]	1'b0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) The enable bit for terminal count interrupt, which controls whether the current LLI is expected to trigger the terminal count interrupt.
		DI	RW	[30]	1'b0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Controls whether or not to increment the destination address. 0: No increment 1: Increments each time a transfer occurs
		SI	RW	[29]	1'b0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Controls whether or not to increment the source address. 0: No increment 1: Increments each time a transfer occurs

	The Channel Control register mapping changes according to the TS value of the DMACConfiguration register.	D	RW	[28]	1'b0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the AHB master channel used for the destination data transfer. 0: Selects AHB master 1 for the destination data transfer. 1: Selects AHB master 2 for the destination data transfer.
		S	RW	[27]	1'b0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the AHB master channel used for the source data transfer. 0: Selects AHB master 1 for the source data transfer. 1: Selects AHB master 2 for the source data transfer.
		DWIDTH	RW	[26:25]	0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the transfer data size of the destination bus. 0: byte transfer 1: halfword transfer 2: word transfer 3: Reserved
		SWIDTH	RW	[24:23]	0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the transfer data size of the source bus. 0: byte transfer 1: halfword transfer 2: word transfer 3: Reserved The data sizes of the source side and the destination side do not have to be the same. The hardware automatically performs the packing and unpacking of the data when required.

		DSIZE	RW	[22:21]	0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the burst size of the destination data transfer. Make sure to set this value to the burst size of the destination peripheral or to the memory boundary size if the memory is the destination. The burst size sets the amount of data to be transferred when the DMACxBREQ signal becomes active at the destination peripheral. The amount of data actually transferred can be calculated by multiplying this burst size by the DWidth. 0: 1 Burst 1: 4 Burst 2: 8 Burst 3: 16 Burst
		SSIZE	RW	[20:19]	0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) Indicates the burst size of the source data transfer. Make sure to set this value to the burst size of the source peripheral or to the memory boundary size if the memory is the source. The burst size sets the amount of data to be transferred when the DMACxBREQ signal becomes active at the source peripheral. The amount of data actually transferred can be calculated by multiplying this burst size and the SWidth. 0:1 Burst 1:4 Burst 2:8 Burst 3:16 Burst

		TRANSFERSIZE	RW	[18:0]	0	When DMACConfiguration.TS=1 (TransferSize expanded mapping) When the DMA controller is the flow controller, the amount of data transfer to be performed is written to this register. Values can be written from 0 to 524287. The actual number of bytes of transferred data is equal to the product of multiplying this by the data width set in the aforementioned SWidth bit. When read out, the completed amount of transfer is indicated. When the DMA controller is not the flow controller, this value becomes invalid.
0x04123110	DMACConfiguration_n (n=0-3,step=0x20) For various settings of the DMA channels. This register does not change by update of the LLI item.	TRIGGER PERIPHERAL	RW	[31:28]	0	When DMACConfiguration.TR=1 (when waiting for external trigger) This is the selection bit for external trigger Peripheral. When the external trigger function is disabled, this bit is invalid. When DMACConfiguration.TR=0 (when operating without external trigger) Becomes Reserved. When writing, set to "0", when reading, mask it.
		TEN	RW	[27]	0	When DMACConfiguration.TR=1 (when waiting for external trigger) This is the external trigger function enable bit. 0: External trigger function is disabled 1: External trigger function is enabled When DMACConfiguration.TR=0 (when operating without external trigger function) Becomes Reserved. When writing, set to "0", when reading, mask it.
		Reserved	RO	[26]	0	Reserved

		DESTMEMBURST	RW	[25]	0	Sets access of the AHB port, which is set as the memory access of the Destination side, so that it always conforms to the burst length set by DBSize. This is used to raise the efficiency of memory access. However, since the FIFO size is 16/32/64 byte, 4/8/16 burst is the largest number of bursts in word size. Be cautious with the DBSize setting of the Channel Control register.
		SRCMEMBURST	RW	[24]	0	Sets access of the AHB port, which is set as the memory access of the Source side, so that it always conforms to the burst length set by SBSIZE. This is used to raise the efficiency of memory access. However, since the FIFO size is 16/32/64 bytes, 4/8/16 burst is the largest number of bursts in word size. Be cautious with the SBSIZE setting of the Channel Control register.
		Reserved	RO	[23:19]	0	Reserved
		HALT	RW	[18]	0	Same as PL080
		ACTIVE	RW	[17]	0	Same as PL080
		LOCK	RW	[16]	0	When this bit is set, locked transfer (HLOCK=H) is performed.
		ITC	RW	[15]	0	Same as PL080
		IE	RW	[14]	0	Same as PL080
		FLOWCNTRL	RW	[13:11]	0	Same as PL080
		Reserved	RO	[10]	0	Reserved
		DESTPERIPHERAL	RW	[9:6]	0	Same as PL080
		Reserved	RO	[5]	0	Reserved
		SRCPERIPHERAL	RW	[4:1]	0	Same as PL080
		E	RW	[0]	0	Same as PL080

0x04123114	DMACDefLLI_n (n=0-3,step=0x20) The register for setting the DefLLI. Does not perform automatic update. When	DEFLLI	RW	[31:2]	0	The address that points to the Default Linked List Item. When transfer starts with the DefLLI function enabled, the LLI of the address that DefLLI points to is read before starting data transfer, and following the update of SrcAddr, DestAddr, LLI, and Control, the transfer starts.
	DMACConfiguration.DLLI=1 (DefLLI function exists), this register exists. When	DEFLE	RW	[1]	0	Selects enable/disable of the DefLLI function. 0: Disabled 1: Enabled
	DMACConfiguration.DLLI=0 (DefLLI function does not exist), all bits become Reserved. When writing, set to "0", when reading, mask it.	DEFLM	RW	[0]	0	Sets the AHB bus master channel that becomes active when the DefLLI is loaded. 0: Selects AHB master 1 1: Selects AHB master 2
0x04123500	DMACITCR	-	RW	[31:0]	0	Same as PL080
0x04123504	DMACITOP1	-	RW	[31:0]	0	Same as PL080
0x04123508	DMACITOP2	-	RW	[31:0]	0	Same as PL080
0x0412350C	DMACITOP3	-	RW	[31:0]	0	Same as PL080
0x04123800	DMACAUX0	AUX_0	RW	[31:0]	0	Any data can be set
0x04123804	DMACAUX1	AUX_1	RW	[31:0]	0	Any data can be set
0x04123808	DMACAUX2	AUX_2	RW	[31:0]	0	Any data can be set
0x0412380C	DMACAUX3	AUX_3	RW	[31:0]	0	Any data can be set

Important Points to Note

- About locked transfer
Locked transfer is not supported. Do not set the corresponding function registers.
- **DMACConfiguration**
Make sure to set the M1, M2 bits to little endian. Setting them to big endian is prohibited.
- **DMACSync**
Use it with the synchronization logic enabled.
- **DMACSreqMask**
Use it with Input enable (Default).
- Transfer using DefLLI function
In the case of writing to the DMACConfiguration_n while the DMAC channel is transferring data, set the **DMACDefLLI_n.DefLE** to “0” beforehand regardless of the bit to be set. Violation of this restriction can result in unexpected operation of the DMAC.
- About the Src/Dst address
For 32bit (Word), 16bit (HalfWord) access, the addresses must be aligned. Make sure to follow the restrictions of each channel's SrcAddr, DstAddr, and Swidth, Dwidth.
 1. If Swidth=Word, SrcAddr[1:0]=2'b00
 2. If Swidth=HalfWord, SrcAddr[0]=1'b0
 3. If Dwidth=Word, DstAddr[1:0]=2'b00
 4. If Dwidth=HalfWord, DstAddr[0]=1'b0
- About Transfersize
When the Dwidth is larger than the Swidth in each DMAC channel, depending on the TransferSize, broken numbers may occur against the data width, and the transfer cannot be completed and the data will be lost. Transfer completion interrupts will not be issued either. Make sure to follow the below restrictions regardless of the flow control of the DMAC.
 1. If Swidth=Byte, Dwidth=HalfWord, the TransferSize must be a multiple of two.
 2. If Swidth=Byte, Dwidth=Word, the TransferSize must be a multiple of four.
 3. If Swidth=HalfWord, Dwidth=Word, the TransferSize must be a multiple of two.
- About the master port setting
When accessing an address area outside the IMG block, use the AHB1 port. When accessing the internal peripheral area, use the AHB2 port. Be cautious with the settings of related function registers.

3.8.8.3 Clock and Reset

Figure DMAC-50 shows the clock and reset system diagram of the IDMAC.

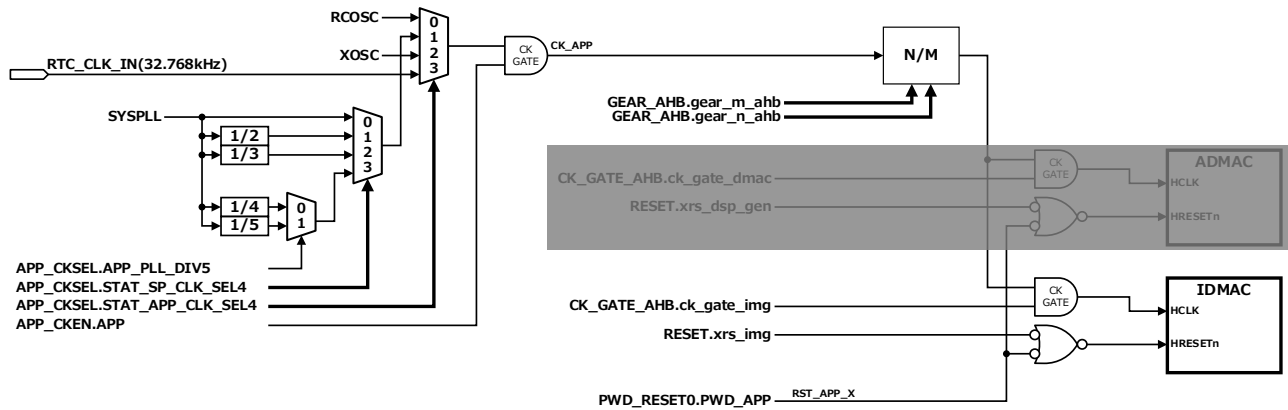


Figure DMAC-50 IDMAC Clock and Reset System

3.8.8.4 Clock Supply Start and Stop

3.8.8.4.1 Clock Supply Start

Perform the following control to start supplying the HCLK clock of the IDMAC.

1. Reset release

PWD_RESET0.PWD_APP=1'b1

RESET.xrs_img=1'b1

2. Supply the CK_APP (Refer to APP (Chapter 3.13))

3. AHB bus clock supply and division ratio setting

GEAR_AHB.gear_m_ahb= (arbitrary: denominator setting of the division ratio)

GEAR_AHB.gear_n_ahb= (arbitrary: numerator setting of the division ratio)

CK_GATE_AHB.ck_gate_dmac=1'b1

3.8.8.4.2 Clock Supply Stop

Perform the following control to stop supplying the HCLK clock of the IDMAC.

1. AHB bus clock stop

CK_GATE_AHB.ck_gate_img=1'b0

3.9 SCU (Sensor Control Unit)

3.9.1 SCU Overview and Features

The Sensor Control Unit (referred to as “SCU” hereinafter) is the block that provides control of capturing output data from the external sensor information.

It offers the following features.

(1) Sensor Interface Function

Analog Input (High Performance ADC) x 2 channels

Successive approximation ADC, 10 bit resolution, 32 kS/s maximum sampling rate

Analog Input (Low Power ADC) x 4 channels

Successive approximation ADC, 10 bit resolution, 32 kS/s maximum sampling rate (when operating one channel)

SPI (master) x 1 channel

Uses the PrimeCell Synchronous Serial Port (PL022) from ARM Limited; supports a maximum transfer frequency of 6.5 MHz

Allows the use of three Slave Selection signals (CS)

I2C (master) x 2 channels

Fast Mode support (Maximum 393.9 kbps)

For details on each sensor interface, refer to the Chapters of each function.

(2) Sequencer Functions for capturing sensor data

The Sequencer performs the following sequence of processes.

Using the designated time intervals as a trigger, it intermittently captures the sensor data from the sensor I/F.

Performs arithmetic processing (MATH_PROC) to the sensor data and stores the results in the FIFO within the SCU.

When storing the calculation results in the FIFO, it adds time stamp information of the time the data was captured.

When the sequencer within the SCU is not used, the CPU can directly control the SPI, I2C, and ADC.

The CPU Block (Ultra Small & Ultra Low Power CPU) is customized as a System for APB Peripheral control

Contains 8 KByte (32bit x 2048words) of SRAM for commands of the internal sequencer and 2 KByte (32bit x 512words) of SRAM for data.

(3) FIFO Functions for Storing Sensor Data

The FIFO has 27 partitions, which are classified into four types.

- Decimation Partitions (4 per each set) x 2 sets
- Normal Sensor Partitions x 8
- Virtual Sensor Partitions x 10

- Random Access Partitions x 1

Each partition is assigned to regions divided within an SRAM having 40 KByte (32bit x 2048words + 32bit x 8192 words) space.

Power supply control of the FIFO SRAM can be performed from the PMU (Power Supply Control Unit) outside the SCU.

A time stamp is attached to each data of the FIFO.

The FIFO data can be read out from the CPU, or from an external host via the HOSTIFC.

In accordance with the data size of the FIFO, handshake is performed with the DMAC outside the SCU, allowing DMA transfer to be performed.

In accordance with the data size of the FIFO, an interrupt signal can be output.

(4) MATH_PROC functions for arithmetic processing of the sensor data

The following arithmetic processing can be executed in a programmable fashion.

- Unsigned data/signed data conversion
- Gain multiplication by each vector element
- Offset addition by each vector element
- Decimation
- Multiplication processing with clipping
- 2nd order IIR filter
- Normalization Processing
- Excess Detection (Event)

(5) PWM function that is capable of external output

The SCU has eight channels of timers for the Pulse Width Modulation (PWM). Up to four of these channels can be output to the external terminals for LED brightness adjustment as the PWM. Timers that are not used as PWMs can be used as timers for the SCU clock reference.

The start timing can be synchronized between each channel of the timers.

The LPADC/HPADC can receive the conversion timing from the timers.

The signal output from the external terminal can be combined by AND or OR logic of the eight channels of output signals.

3.9.2 SCU Block Diagram

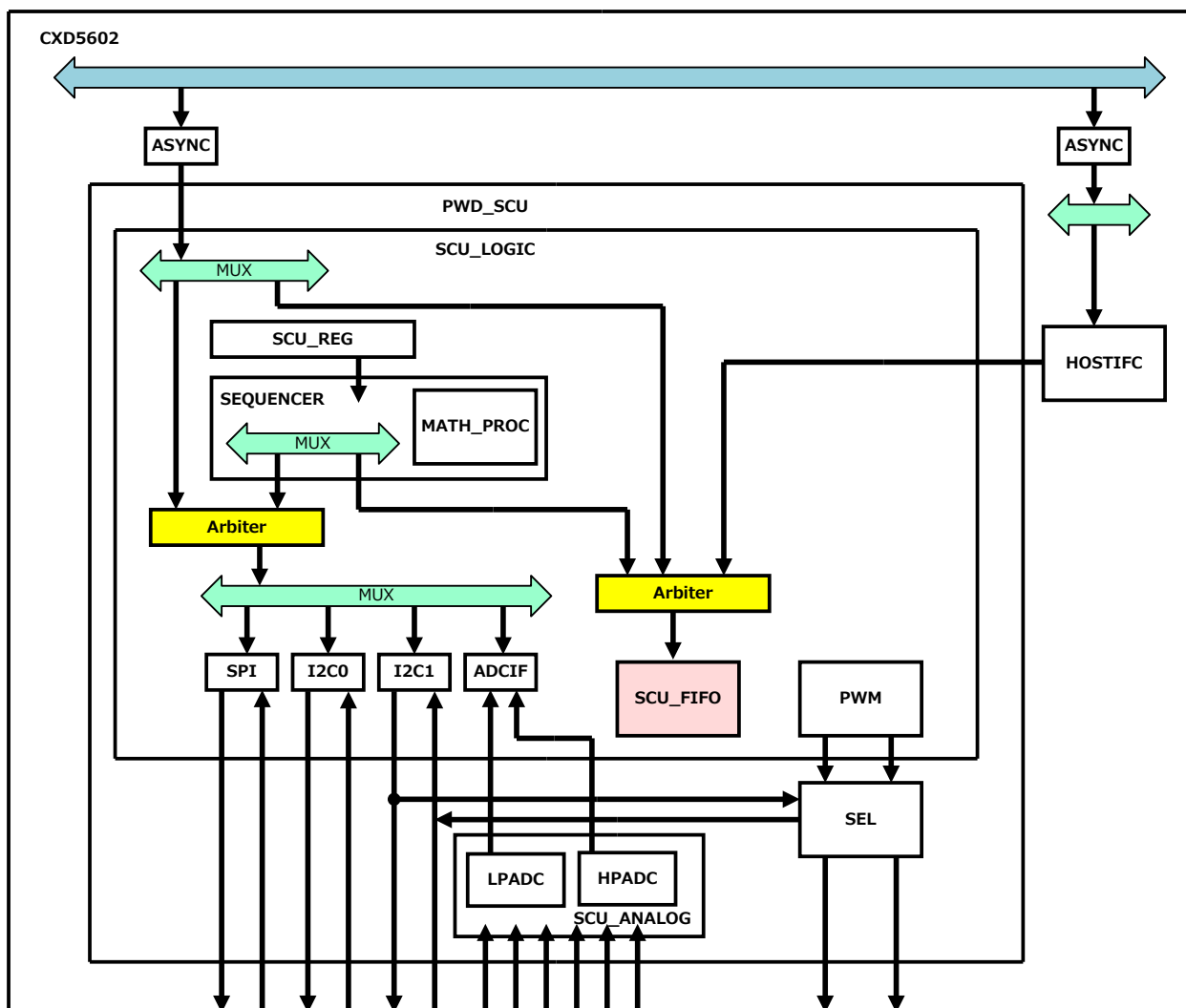


Figure SCU (Sensor Control Unit)-51 Block Function Overview

3.9.3 Memory Map

Figure SCU (Sensor Control Unit)-52 shows the MemoryMap as seen from the SYSCPU.

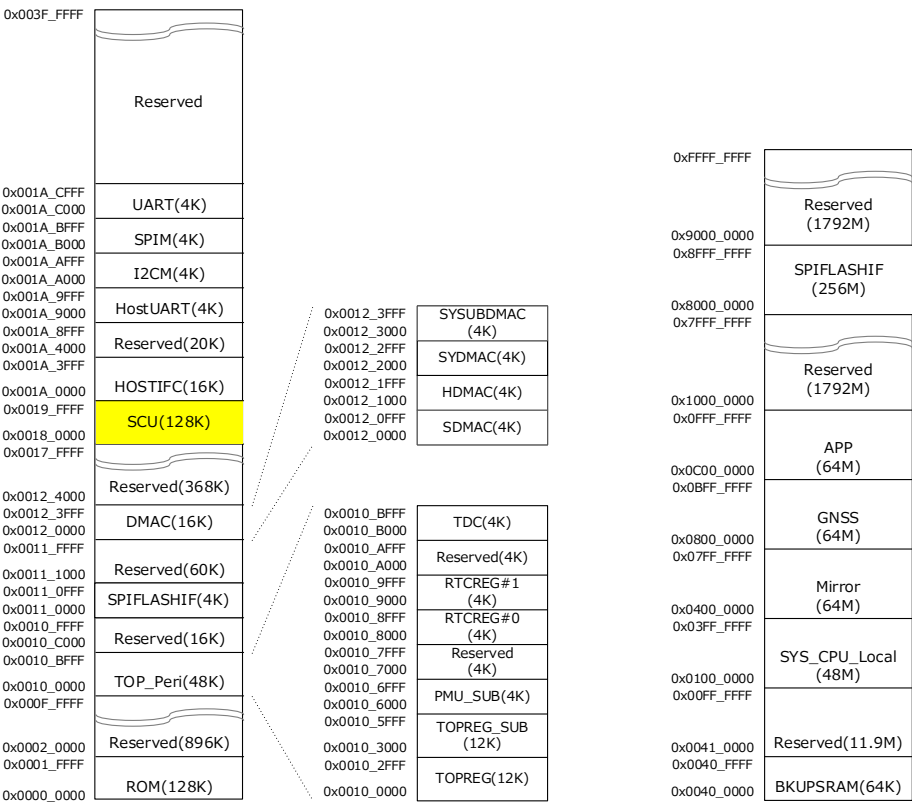


Figure SCU (Sensor Control Unit)-52 Memory Mapping from the Upper CPUs; the CPU in the SYSIOP and the CPU in the GNSS; (hereinafter in the Chapter on SCU, referred as “upper CPUs”)

Figure SCU (Sensor Control Unit)-53 shows the Memory Map within the SCU as seen by the upper CPUs.

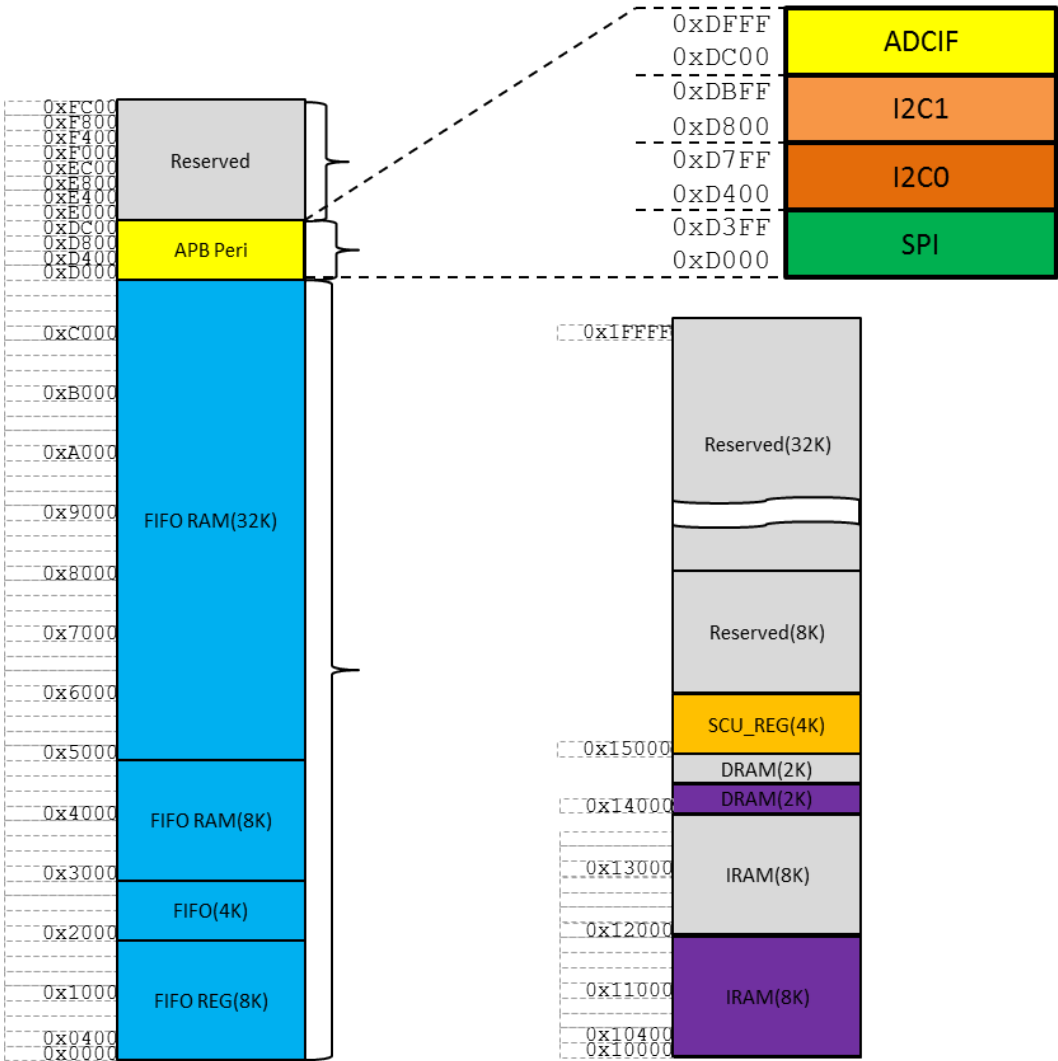


Figure SCU (Sensor Control Unit)-53 Memory Mapping within the SCU as seen from the Upper CPUs

The Reserved area within this Figure is writing-invalid (no error response) and “0” read during readout (no error response).

The data storage region including the FIFO RAM (32 KByte) and FIFO RAM (8 KByte) is 40 KByte. Refer to Section 3.9.8 for details.

The FIFO (4 KByte) is the port for data writing and readout. Refer to Table SCU (Sensor Control Unit)-103 for details.

The FIFO REG (8 KByte) handles controls around the FIFO. Refer to Section 3.9.12.10 for details.

The SCU_REG (4 KByte) is the control register. Refer to Section 3.9.12.3 for details.

The DRAM (2 KByte) is used as the SCU_RAM. Refer to Section 3.9.12.11 for details.

The IRAM (8 KByte) is used as the SEQ_IRAM. This stores the control firmware of the internal sequencer.

Figure SCU (Sensor Control Unit)-54 shows the Memory Map as seen from the internal sequencer of the SCU.

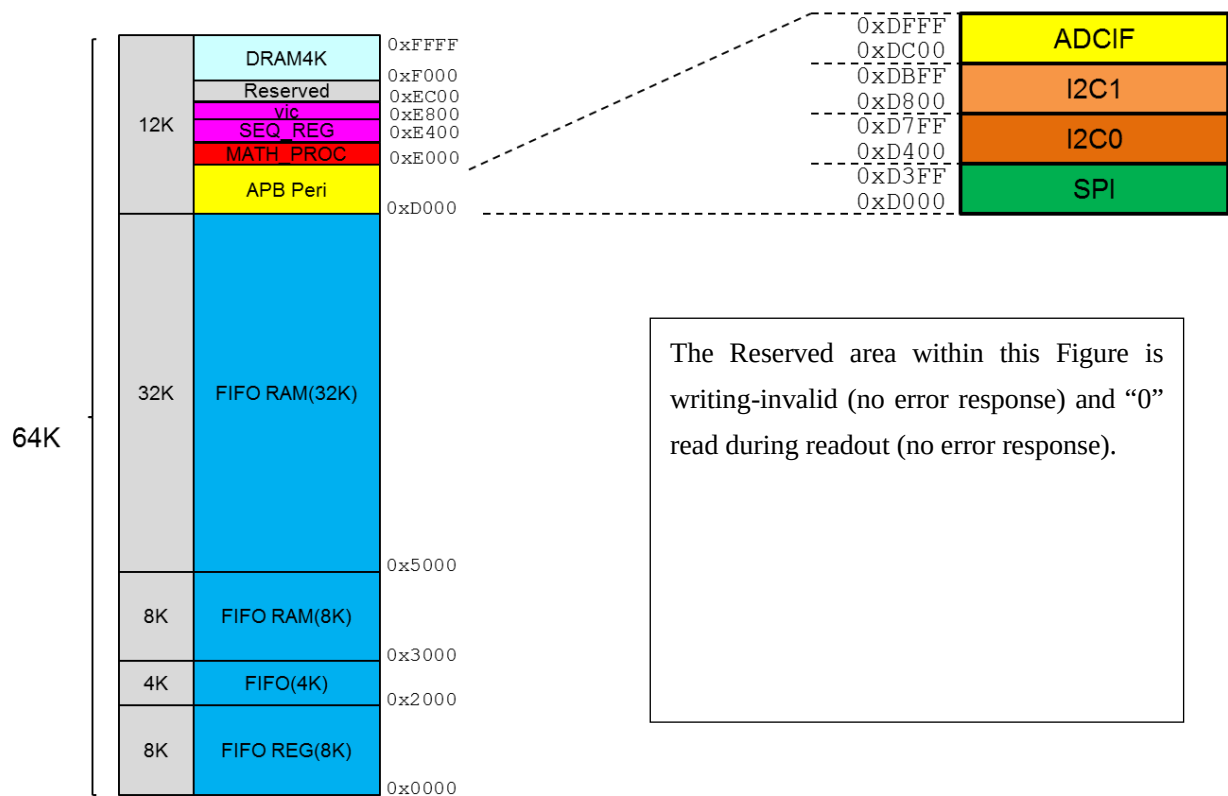


Figure SCU (Sensor Control Unit)-54 Memory Mapping as seen from the Internal Sequencer

Figure SCU (Sensor Control Unit)-55 shows the Memory Mapping as seen from the SCU window of the HOSTIFC.

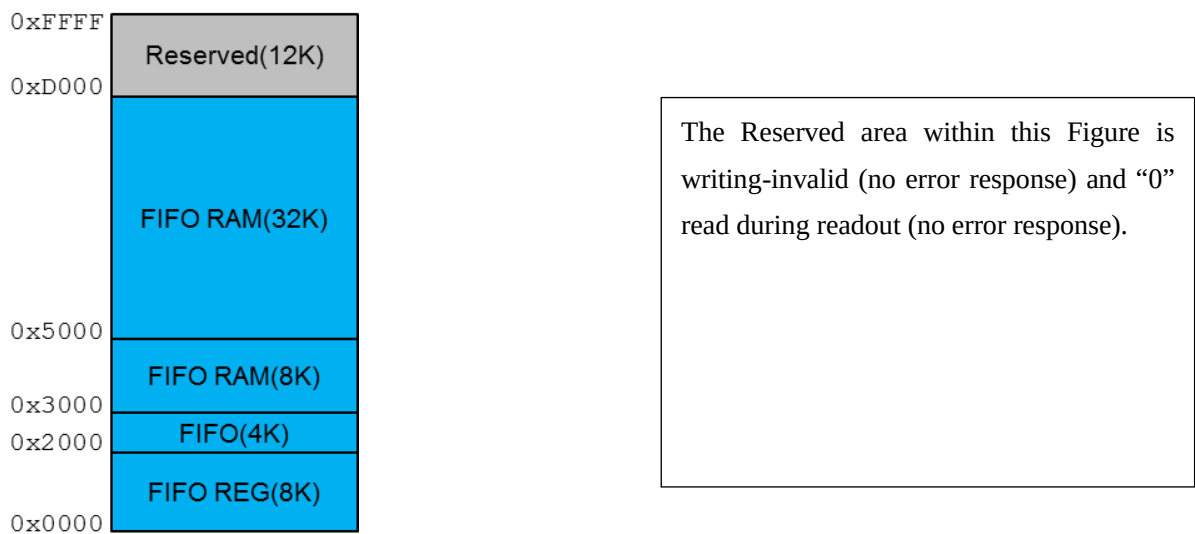


Figure SCU (Sensor Control Unit)-55 Memory Mapping as seen from the HOSTIFC

3.9.4 Clock Control

3.9.4.1 Clock Summary

Table SCU (Sensor Control Unit)-82 Clock Summary

Clock Name	Maximum Frequency (High Performance mode)	Maximum Frequency (Low Power mode)	Usage
CK_SCU_SCU	13MHz	13MHz	SCU Main
CK_SCU_SCU_SC	13MHz	13MHz	SCU Main CPU control only
CK_SCU_SCU_SPI	13MHz	13MHz	For SPI
CK_SCU_SCU_I2C0	13MHz	13MHz	For I2C0
CK_SCU_SCU_I2C1	13MHz	13MHz	For I2C1
CK_SCU_SCU_SEQ	13MHz	13MHz	For SCU internal sequencer
CK_SCU_XOSC	13MHz	13MHz	For HPADC ^(1*)
CK_SCU_RC8M	8MHz	8MHz	For HPADC ^(1*)
CK_SCU_U32KL	32kHz	32kHz	For LPADC ^(1*)
CK_SCU_U32KH	32kHz	32kHz	For HPADC ^(1*)
CK_SCU_32K	32kHz	32kHz	For PWM
CK_SCU_BRG_HCLK	13MHz	13MHz	For AHB BUS

^{1*} For details on the clocks for the HPADC and LPADC, refer to the Chapter on ADC (3.21).

3.9.4.2 Logic System (High Speed) Clocks

- CK_SCU_SCU
- CK_SCU_SCU_SC
- CK_SCU_SPI (for SPI)
- CK_SCU_I2C0 (for I2C0)
- CK_SCU_I2C1 (for I2C1)
- CK_SCU_SEQ (for SEQ)
- CK_SCU_BRG_HCLK

The above Logic System (High Speed) Clocks all have the same operating frequency (they are synchronized) but their control conditions for clock enabler are different.

The Logic System (High Speed) Clocks are generated from one of the below clock sources at CRG (Clock and Reset Generator) outside the SCU.

- RCOSC (standard operating frequency of 8.13 MHz)
- XOSC
- CK_SCU_32K (RTC clock or RCOSC divided by 250)

For the XOSC, frequency divisions of 1, 2, 3, or 4 can be selected by the CRG. However, since the maximum operating frequency of the SCU is 13 MHz, you will need to select the appropriate frequency division in accordance with the crystal oscillator that is connected from outside. Use the API to select these clock sources, the XOSC frequency division, and the source for the CK_SCU_32K.

3.9.4.3 Logic System (Low Speed) Clock

CK_SCU_32K

The Logic System (Low Speed) Clocks operate at around 32.768 kHz and are generated from one of the below clock sources.

- RTC (32.768 kHz)
- RCOSC divided by 250

Use the API to select these clock sources.

3.9.4.4 HPADC Clock and LPADC Clock

For details on the HPADC clock and LPADC clock, refer to the Chapter on ADC (3.21) clock control.

3.9.4.5 Clock Control Summary

The following table summarizes the selection of input clocks. For details on the LPADC and HPADC clocks, refer to the Chapter on ADC (3.21).

Table SCU (Sensor Control Unit)-83 Input Clock Source Selection

Clock Source Selector (*)	Frequency Division Circuit (*)	Clock Source Selector (*)	Clock Port Name	Description
• RTC • RCRTC (RCOSC divided by 250)	None (directly connected)	• RCOSC (standard operating frequency of 8.192 MHz)	CK_SCU_SCU	Main clock Can be controlled from the SCU and HOSTIFC
		• XOSC (after selecting to divide by 1, 2, 3, or 4) • The clock selected by Selector 1	CK_SCU_SCU_SC	Main clock Cannot be controlled from the SCU or HOSTIFC (supplied to the ADCIF and INTIC)

* The Clock Source Selector and frequency division circuit can be controlled from the TOPREG.

Figure 10: SCU clock configuration block diagram. The diagram illustrates the internal clock routing for the SCU. It shows the selection of clock sources (RCOSC, XOSC) and the configuration of the SCU_CKEN control signals to generate the final SCU clock outputs (CK_SCU_32K, CK_SCU_SCU, CK_SCU_BRG_HCLK, CK_SCU_SCU_SC, CK_SCU_SCU_SPI, CK_SCU_SCU_SEQ, CK_SCU_SCU_I2C1, CK_SCU_SCU_I2C0). The diagram also shows the SCU block and the SCU_CKEN control signals.

(1) control signal from the HOSTIFC sequencer
(2) control signal from the SCU sequencer

As shown in Figure SCU (Sensor Control Unit)-56, the clock signal provided to CK_SCU_SCU is controlled by the signal that is made by ORing SCU_CKEN[0]: the signal from the upper layer, the signal (1) from the internal sequencer of the HOSTIFC, and the signal (2) from the internal sequencer of the SCU. The clock signal

provided to CK_SCU_SCU_SPI, CK_SCU_SCU_I2C1, and CK_SCU_SCU_I2C0 are controlled by the signal that is made by ORing dedicated bit in the SCU_CKEN: the signal from the upper layer, and the signal (2) from the internal sequencer of the SCU. Note that each control signal from the internal sequencer that is input to each clock's control is independent.

The clock signal provided to CK_SCU_SCU_SEQ is controlled by the signal that is made by ANDing SCU_CKEN[4]: the signal from the upper layer, and the signal (2) from the internal sequencer of the SCU.

As this described, the clocks within the SCU are divided into several domains, and clock control is possible from the SYSCPU, DSP, internal sequencer of the HOSTIFC, or the internal sequencer of the SCU. In the case of controlling from multiple CPUs/internal sequencers, OR control is used.

Table SCU (Sensor Control Unit)-84 Control of each Clock

SCU Clock Name	Control from the Upper CPU	Control from Internal Sequencer of SCU	Control from Internal Sequencer of HOSTIFC
CK_SCU_SCU	possible	possible	possible
CK_SCU_SCU_SC	possible	—	—
CK_SCU_SCU_SPI	possible	possible	—
CK_SCU_SCU_I2C0	possible	possible	—
CK_SCU_SCU_I2C1	possible	possible	—
CK_SCU_SCU_SEQ	possible	possible	—

The clocks are controlled using the following registers.

Table SCU (Sensor Control Unit)-85 Clock Control Registers

Controlled from:	Block Name	Register Name	offset	Remarks
CPU	TOPREG	SCU_CKEN	0x071c	TOPREG Control Region
HOSTIFC	HOS_SEQ_REG	HOS_SCU_POWER	0x0010	HOSTIFC Register Internal Sequencer Control Region
SCU	SCU_SEQ_REG	SCU_ISOP_POWER	0x0044	SCU Register Internal Sequencer Control Region

3.9.4.6 Clock Control from Internal Sequencers

To reduce power consumption, the firmware of the internal sequencers attempts to stop as many as clocks as possible during Sleep. Also, since SPI, I2C0, and I2C1 are master devices, each of their clocks are controlled by the internal sequencers so they operate only during data transfer (Table SCU (Sensor Control Unit)-94). The CK_SCU_32K and CK_SCU_SCU_SC clocks are required for operation of the internal sequencers but since they are not controlled by the internal sequencers, they must be turned ON from the CPU for operation of the SCU.

Table SCU (Sensor Control Unit)-86 Clock Control from the Internal Sequencers

SCU Clock Name	During Internal Sequencer Sleep	During Internal Sequencer Active
CK_SCU_SCU	OFF	ON
CK_SCU_SCU_SC	Not controlled	
CK_SCU_SCU_SPI	OFF	ON only during SPI transfer, OFF all other times
CK_SCU_SCU_I2C0	OFF	ON only during I2C0 transfer, OFF all other times
CK_SCU_SCU_I2C1	OFF	ON only during I2C1 transfer, OFF all other times
CK_SCU_SCU_SEQ	OFF	ON
CK_SCU_32K	Not controlled	

3.9.4.7 Clock Control from CPU

When viewed from the SYSCPU, the ON/OFF control of the internal sequencer clocks change automatically during the operation of the internal sequencers. During the operation of the internal sequencers, ON/OFF switching of the internal sequencer clocks cannot be controlled by the SYSCPU, and is automatically performed. The CPU must supply the clocks so that the ON/OFF control of internal sequencer clocks can be properly performed (Table SCU (Sensor Control Unit)-95).

Table SCU (Sensor Control Unit)-87 Clock Control from CPU

Operation requested from CPU	CK_SCU_SCU (SYSCPU/Internal Sequencer Resource)	CK_SCU_SCU_SC (SYSCPU Resource)	CK_SCU_SCU_SPI (SYSCPU/Internal Sequencer Resource)	CK_SCU_SCU_I2C0 (SYSCPU/Internal Sequencer Resource)	CK_SCU_SCU_I2C1 (SYSCPU/Internal Sequencer Resource)	CK_SCU_SCU_SEQ (Internal Sequencer itself and Resource)	CK_SCU_XOSC (SYSCPU Resource)	CK_SCU_RC8M (SYSCPU Resource)	CK_SCU_U32KL (SYSCPU Resource)	CK_SCU_U32KH (SYSCPU Resource)	CK_SCU_32K (SYSCPU Resource)
SCU Internal Register Access (incl. FIFO)	clock ON	clock OFF	C	C	C	clock OFF	clock OFF	clock OFF	clock OFF	clock OFF	clock OFF
RAM Access ^(1*)	clock ON	clock OFF	clock OFF	clock OFF	clock OFF	W	clock OFF	clock OFF	clock OFF	clock OFF	clock OFF
ADC is used (Internal Sequencer is not used)	clock ON	clock ON	clock OFF	clock OFF	clock OFF	clock OFF	C	C	C	C	clock OFF
PWM is used (Internal Sequencer is not used)	clock ON	clock OFF	clock OFF	clock OFF	clock OFF	clock OFF	C	C	C	C	clock ON
When Internal Sequencer is used	clock OFF	clock ON	clock OFF	clock OFF	clock OFF	clock ON	C	C	C	C	clock ON

C: When using the corresponding resource, the clock must be turned ON.

W: Inhibition of automatic ON/OFF of clock (SCU_REG register: by HPADC0_ACCESS_INHIBIT_REQ)

^{1*} In addition to this method, access to the SCU_RAM is possible by turning ON the CK_SCU_SCU_SEQ clock during the assertion of an internal sequencer reset because the clock is supplied.

For information on CK_SCU_XOSC, CK_SCU_RC8M, CK_SCU_U32KL, and CK_SCU_U32KH, also refer to the ADC (3.21) Chapter.

When multiple operations coincide, the corresponding clock must be turned ON from the CPU even when one clock is “clock ON”.

3.9.5 Power Supply Control

The SCU module belongs to a power domain called PWD_SCU.

Within the PWD_SCU, there are power supply control module regions (listed below) as separate power domains. Refer to the PMU Chapter (3.4) for details on the ON/OFF control registers of these power domains.

Table SCU (Sensor Control Unit)-88 Power Supply Control Registers

Power Supply Control Target	Control Register Name
LPADC	ANA_PW_CTL
HPADC	ANA_PW_CTL
FIFO SRAM (8KByte)	SCU_RAMMODE_SEL
FIFO SRAM (32KByte)	SCU_RAMMODE_SEL
Internal Sequencer SRAM (Instruction, Data)	SCU_RAMMODE_SEL

3.9.6 Interrupt

3.9.6.1 Overview

The SCU has four lines of interrupts, which connect to the SYSCPU and DSP.

For details, refer to the Chapter on Interrupt (3.3).

The following shows the relation with the interrupt number.

Table SCU (Sensor Control Unit)-89 Interrupt Number

SCU Interrupt Name	Description
INT0	SPI interrupt
INT1	I2C0 interrupt
INT2	I2C1 interrupt
INT3	Event Interrupt

3.9.6.2 Interrupt Details

The interrupts that occur within the SCU are connected to the CPU in the SYSIOP and the CPU in the GNSS; (hereinafter referred as “upper CPUs” in the Chapter on SCU), and also notified to the internal sequencer of the SCU.

The interrupts to the upper CPUs are integrated into four interrupts at the INT_SEL module, and then output. The interrupts from the SPI, I2C0, and I2C1 are output separately from the other interrupts. Other interrupts such as LPADC, HPADC, PWM, and FIFO are ORed within the INT_SEL and combined into

one signal that is output as INT3.

An interrupt mask can be separately set for each of the interrupt factors, and the statuses before and after the masks are applied can be read out.

The Edge interrupt factor can be cleared. In addition, depending on the interrupt factor, Level/Edge selection is possible.

Figure SCU (Sensor Control Unit)-57 shows the connections of the INT_SEL.

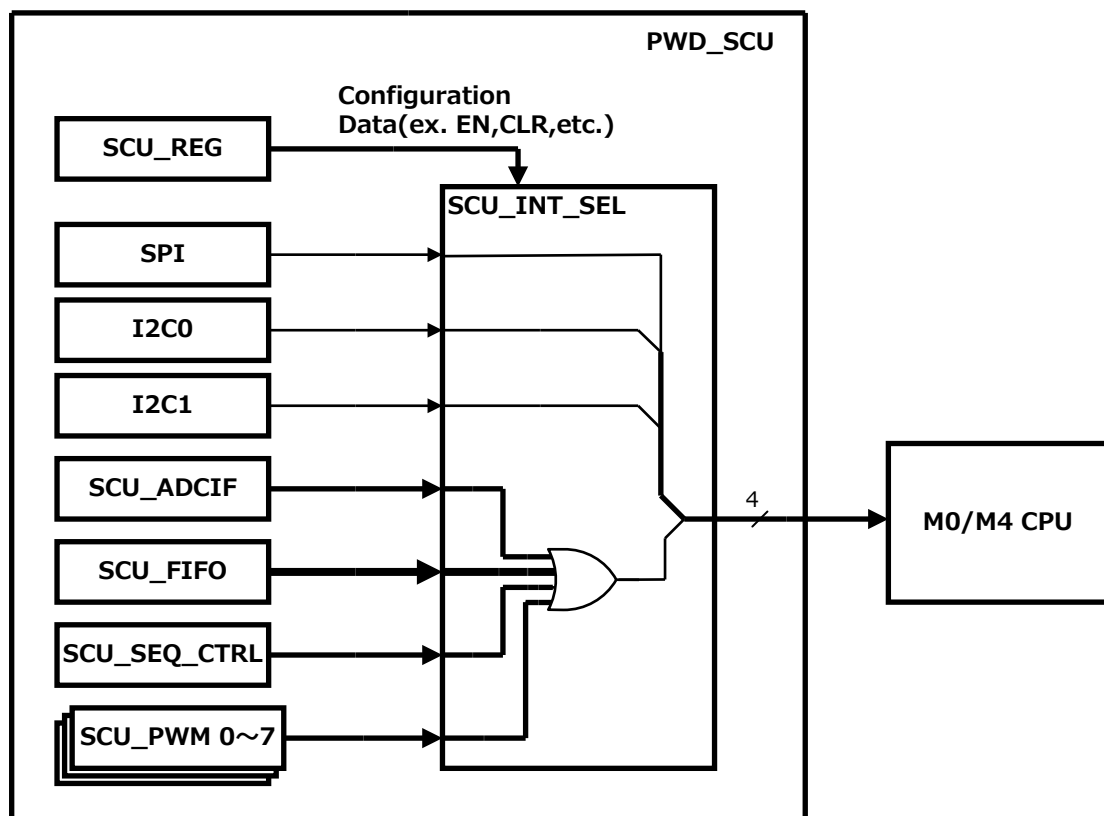


Figure SCU (Sensor Control Unit)-57 Interrupt Connections

Table SCU (Sensor Control Unit)-98 and Table SCU (Sensor Control Unit)-99 show the interrupt factors that are ORed within the SCU.

Table SCU (Sensor Control Unit)-90 Information Interrupts

Interrupt Name	Number	Description	Edge/L evel
LPADC_ALMO ST_FULLn	4 (n = 0, ..., 3) *	The data amount stored in the FIFO for the “n” th channel of the LPADC within the ADCIF has reached the Watermark	Selecta ble
HPADCn_ALM OST_FULL	2 (n = 1, 2)	The data amount stored in the FIFO for the “n” th channel of the HPADC within the ADCIF has reached the Watermark	Selecta ble
MATH_EVENT n_R	3 (n = 0, 1, 2)	Rise Event of the Math Function n within the MATH_PROC	Edge
D0_Rn_C_ALM OST_FULL	2 (n = 1, 2)	The data amount stored in the FIFO partition D0_Rn has reached the Watermark	Selecta ble
D1_Rn_C_ALM OST_FULL	2 (n = 1, 2)	The data amount stored in the FIFO partition D1_Rn has reached the Watermark	Selecta ble
Nn_R1_C_ALM OST_FULL	8 (n = 0, ..., 7)	The data amount stored in the FIFO partition Nn_R1 has reached the Watermark	Selecta ble
Dn_R3_CH_AL MOST_FULL	2 (n = 0, 1)	The data amount stored in the FIFO partition Dn_R3 has reached the Watermark	Selecta ble
ISOPn	4 (n = 0, ... 3)	Interrupt n from the internal sequencer	Selecta ble
MATH_EVENT n_F	3 (n = 0, 1, 2)	Fall Event of Math Function n within the MATH_PROC	Edge
PWMn_INVALID D_VALUE	8 (n = 0, ..., 7)	PWMn timer mode interrupt	Edge

Note: As for the name of the interrupt for LPADC ch.0, the n is not “0” but is left blank.

Table SCU (Sensor Control Unit)-91 System Error Interrupts

Interrupt Name	Number	Description	Edge/ Level
LPADC_OVE R_RUNn	4 (n = 0, ..., 3) *	The FIFO for the “n” th channel of the LPADC within the ADCIF has overflowed	Edge
HPADCn_OV ER_RUN	2 (n = 1, 2)	The FIFO for the “n” th channel of the HPADC within the ADCIF has overflowed	Edge
ADCIF_REA D_ERR	1	An abnormal readout from the FIFO within the ADCIF has occurred	Edge
D0_Rn_C_OV ER_RUN	2 (n = 1, 2)	The FIFO partition D0_Rn has overflowed	Level
D1_Rn_C_OV ER_RUN	2 (n = 1, 2)	The FIFO partition D1_Rn has overflowed	Level
Nn_R1_C_OV ER_RUN	8 (n = 0, ..., 7)	The FIFO partition Nn_R1 has overflowed	Level
Dn_R3_CH_O VER_RUN	2 (n = 0, 1)	The FIFO partition Dn_R3 has overflowed	Level
LPADC_UND ER_RUNn	4 (n = 0, ..., 3) *	The FIFO for the “n” th channel of the LPADC within the ADCIF was empty but readout	Edge
HPADCn_UN DER_RUN	2 (n = 1, 2)	The FIFO for the “n” th channel of the HPADC within the ADCIF was empty but readout	Edge
D0_Rn_C_UN DER_RUN	2 (n = 1, 2)	The FIFO partition D0_Rn was empty but readout	Level
D1_Rn_C_UN DER_RUN	2 (n = 1, 2)	The FIFO partition D1_Rn was empty but readout	Level
Nn_R1_C_UN DER_RUN	8 (n = 0, ..., 7)	The FIFO partition Nn_R1 was empty but readout	Level
Dn_R3_CH_U NDER_RUN	2 (n = 0, 1)	The FIFO partition Dn_R3 was empty but readout	Level
REQ_BEFOR E_FINISHn	10 (n = 0, ..., 9)	The execution of SEQn wasn't in time by the next execution opportunity	Level
EXE_ERRn	10 (n = 0, ..., 9)	An error occurred when executing SEQn	Level

Note: As for the name of the interrupt for LPADC ch.0, the n is not “0” but is left blank.

For the internal sequencers, interrupt signals separate from the those for the upper CPU are connected.

Table SCU (Sensor Control Unit)-100 shows the interrupt factors received by the sequencers.

Table SCU (Sensor Control Unit)-92 Interrupts for the Sequencers

Interrupt Name	Number	Description
EXE_REQ_STTn	10 (n = 0, ..., 9)	Execution request to SEQn
APB_ACCESS_INHI BIT	1	Access to the APB was prohibited by the upper CPU
I2C0_RX_ALMOST_ FULL	1	The FIFO for the data received via the I2C0 has the specified number of data
I2C0_MASTER_ON_ HOLD	1	The FIFO for the data sent via the I2C0 is empty but a STOP command has not been issued
I2C0_ACTIVE	1	The operation of the I2C0 is Active
I2C1_RX_ALMOST_ FULL	1	The FIFO for the data received via the I2C1 has the specified number of data
I2C1_MASTER_ON_ HOLD	1	The FIFO for the data sent via the I2C1 is empty but a STOP command has not been issued
I2C1_ACTIVE	1	The operation of the I2C1 is Active
LPADCn_NOT_EMP TY	4 (n = 0, ..., 3)	The FIFO for the “n” th channel of the LPADC has one or more data
HPADCn_NOT_EMP TY	2 (n = 0, 1)	The FIFO for the “n” th channel of the HPADC has one or more data
MATH_PROC_WRIT E_DATA_READY	1	Indicates whether or not writing is possible to the MATH_PROC
MATH_PROC_READ _DATA_READY	1	Indicates whether or not readout is possible from the MATH_PROC
FIFO0_ALL_ON_STT	1	Indicates that the power supply status of the FIFO SRAM (8 KByte) is All On
FIFO1_ALL_ON_STT	1	Indicates that the power supply status of the FIFO SRAM (32 KByte) is All On
TIMER_INTn	3 (n = 0, ..., 2)	Timer mode interrupt (selectable from eight lines) of PWMm (m = 0, ..., 7)

The firmware of the SCU internal sequencer notifies the CPU of the following interrupts.

Table SCU (Sensor Control Unit)-93 Internal Sequencer Interrupts

Interrupt Name	Description
iSoP0	Data was output to the Output Region 0 of the one-shot sequencer
iSoP1	Data was output to the Output Region 1 of the one-shot sequencer
iSoP2	Data was output to the Output Region 2 of the one-shot sequencer
iSoP3	A complete interrupt or suspend interrupt occurred (Synchronous communication control interrupt between the SCU and CPU)
EXE_ERR	An error occurred during execution of the sequencer

REQ_BEFORE_FINISH	This process was not in time by the next startup of the sequencer. A timeout error.

3.9.7 MATH_PROC processing

The MATH_PROC processing performs programmable arithmetic processing to the data captured by the sensors.

When using MATH_PROC processing, make sure that the data type is “Calculation Operable Sample Type”.

Calculation Operable Sample Type refers to one of the following data types.

Calculation Operable Sample Type

- 16-bit 1 axis: 1 sample = {x} format (2 Byte)
- 16-bit 2 axis: 1 sample = {x,y} format (4 Byte)
- 16-bit 3 axis: 1 sample = {x,y,z} format (6 Byte)

The following processes can be handled.

Preprocessing (For details, see Section 3.9.7.1)

- Unsigned data/signed data conversion
- Gain multiplication by vector element
- Offset addition by vector element

Decimation Processing (For details, see Section 3.9.7.2)

- Decimation
- Multiplication processing with clipping

Math Function Processing (For details, refer to Section 3.9.7.3)

- 2nd order IIR filters
- Normalization processing
- Excess detection (Event)

In the MATH_PROC processing, a total of 10 lines of executable data paths can be used by combining the above calculations. There are two types of data paths according to the differences in what they process.

- Decimation Partition Data Path ... x two lines
- Normal Sensor Partition Data Path ... x eight lines

Figure SCU (Sensor Control Unit)-58 and Figure SCU (Sensor Control Unit)-59 show the structures of each data path.

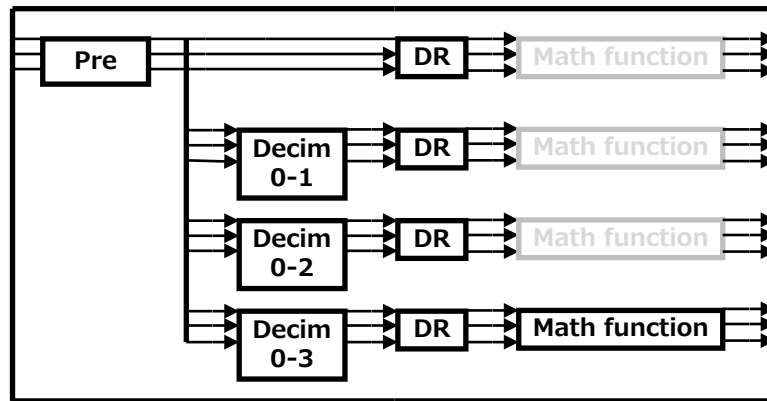


Figure SCU (Sensor Control Unit)-58 Decimation Partition Data Path

- Preprocessing can be performed to the 1, 2, or 3 axis data of the signed 16 bit.
- The data after preprocessing can be sent through three lines of Decimeters and one bypass path.
- Afterwards, Dynamic Range adjustment can be applied separately to the four lines of data.
- And then, the Math Function can be assigned.

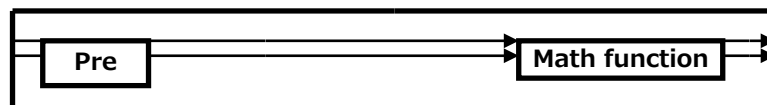


Figure SCU (Sensor Control Unit)-59 Normal Sensor Partition Data Path

- Preprocessing can be performed to the 1, 2, or 3 axis data of the signed 16bit.
- Afterwards, the Math Function can be assigned.

The Math Function processing can be inserted in up to three paths among the total of 16 paths in the MATH_PROC (four paths per Decimation Partition Data Path x two lines, 1 path per Normal Sensor Partition Data Path x eight lines). In the Decimation Partition Data Path example in Figure SCU (Sensor Control Unit)-58, the Math Function is inserted only in the Decim 0-3 lines, and the Dynamic Range adjustment (DR) output is directly connected to the direct connection/Decim 0-1/Decim 0-2 lines.

3.9.7.1 Preprocessing

The following functions can be executed for all MATH_PROC paths according to the values set in the registers.

- (1) Signed data/unsigned data conversion
- (2) Offset addition
- (3) Gain multiplication

These processes are called Preprocessing and the data flow is shown in Figure SCU (Sensor Control Unit)-60.

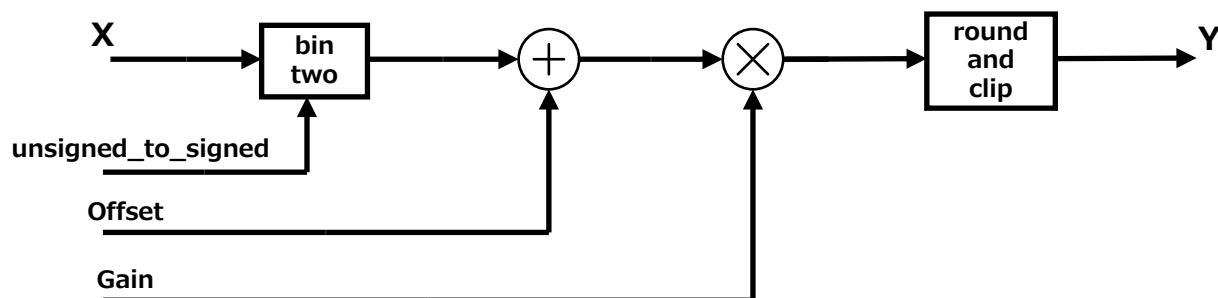


Figure SCU (Sensor Control Unit)-60 Preprocessing Data Flow

As for offset addition and gain multiplication, when the data is multiple-axis (2 axis/3 axis), settings can be made independently for each X, Y, and Z axis.

3.9.7.2 Decimation Processing

In the MATH_PROC processing, up to two lines of decimation filters (two-stage CIC filter) can be used, which can be applied to the sensor data captured by the SEQ0 sequencer and SEQ1 sequencer.

The decimation path has four output paths per each input, and $1/(2^n)$ decimation can be selected for three of them depending on the settings. A two-stage CIC filter process is applied for the decimation processing. For the three target paths of decimation, the results of decimation, the input signal in its original form, or the setting for 0-fixed output can be selected.

Also, after the decimation processing, multiplying by 2^n times with clipping is performed. In this process, a common multiplying by 2^n times coefficient is used for the X, Y, and Z axes.

Figure SCU (Sensor Control Unit)-61 shows the data flow of the decimation and multiplication processing with clipping.

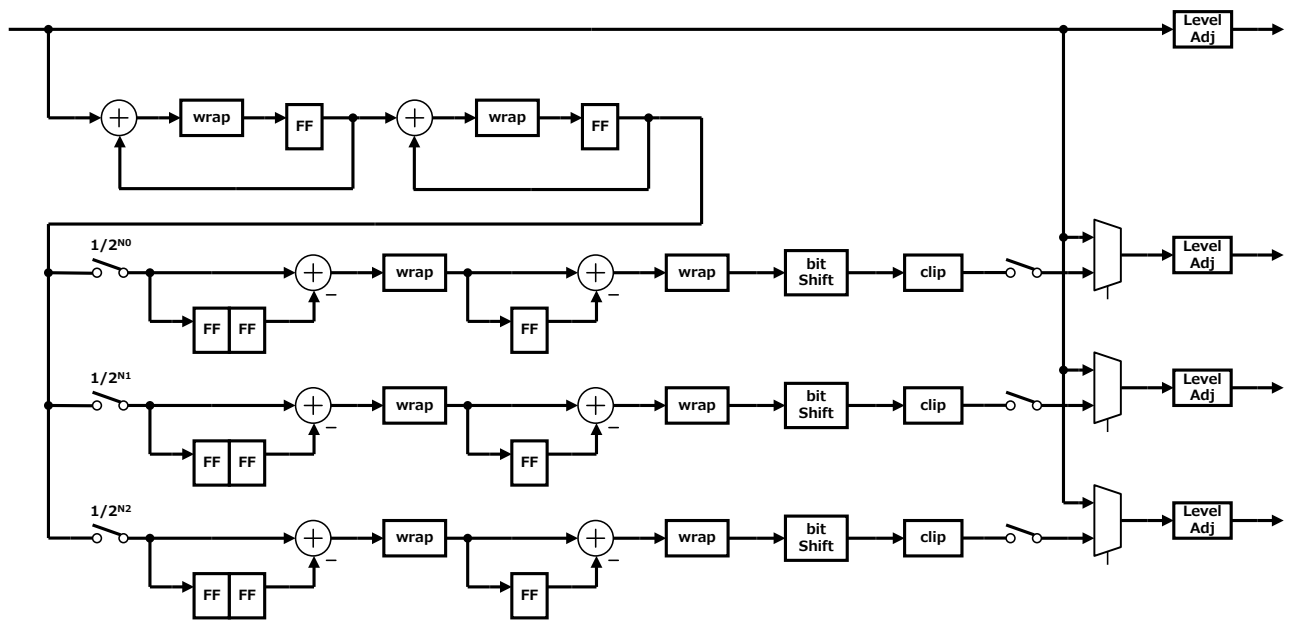


Figure SCU (Sensor Control Unit)-61 Decimation Processing Data Flow

3.9.7.3 Math Function Processing

3.9.7.3.1 2nd Order IIR Filter

The Math Function is a function block comprised of 2nd order IIR Filters, normalization processing, and excess detection.

Of the 16 paths for writing to the FIFO within the MATH_PROC, up to three can be independently inserted in arbitrary paths.

Within the Math Function, there are the two following data paths.

- (1) Path that outputs to the FIFO
- (2) Path that is input to the excess detection after the normalization processing

Figure SCU (Sensor Control Unit)-62 shows the overall data path within the Math Function.

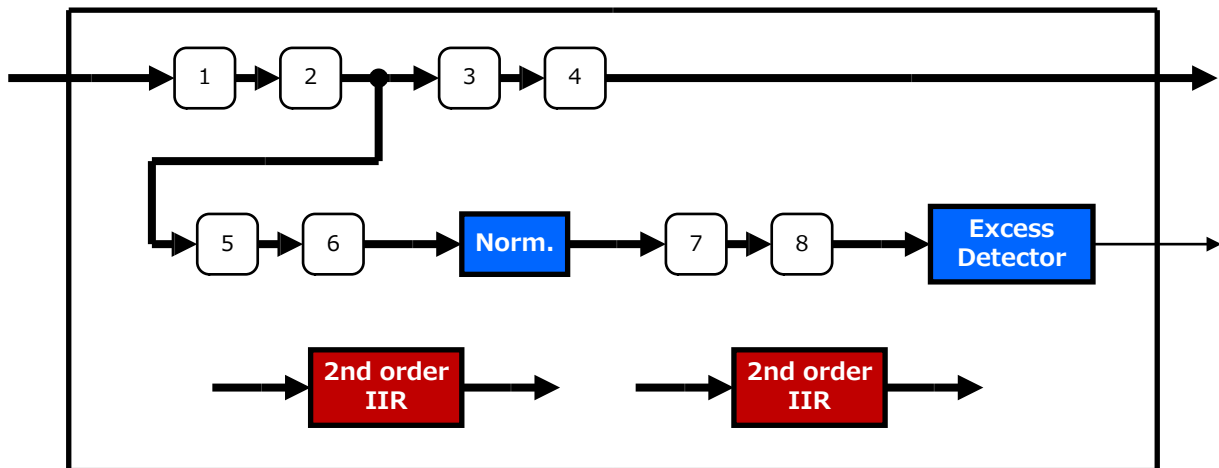


Figure SCU (Sensor Control Unit)-62 Data Flow within the Math Function

The path on the top is output to the FIFO and the path on the bottom is used for excess detection. Also, at blocks 1 through 8 in Figure SCU (Sensor Control Unit)-62, two 2nd order IIR filters can be inserted at arbitrary points by setting the registers.

Figure SCU (Sensor Control Unit)-63 shows the combination of data paths when 2nd order IIR filters are inserted.

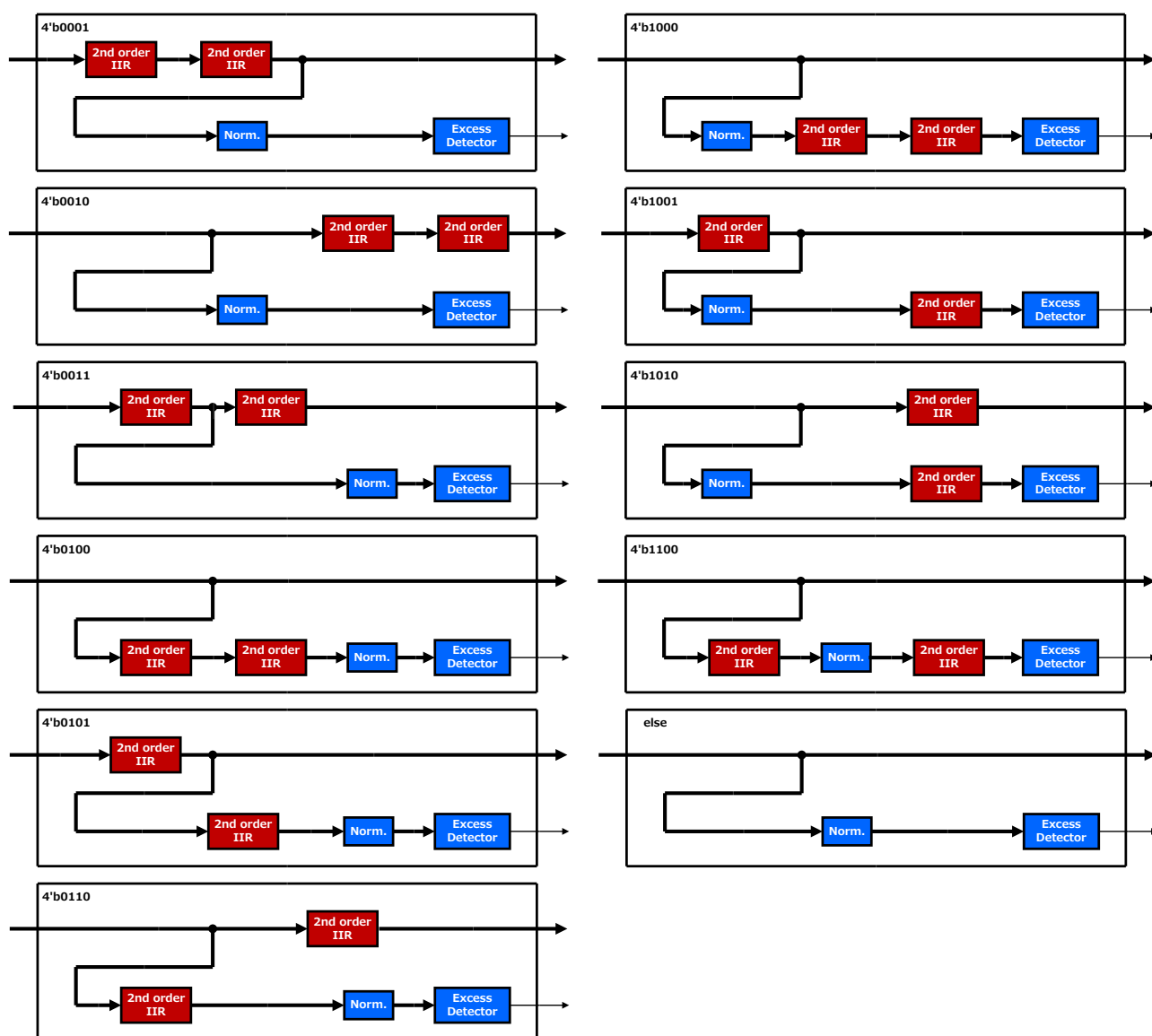


Figure SCU (Sensor Control Unit)-63 2 2nd Order IIR Filter Combinations

The 2nd order IIR Filters allows settings of five multiplication coefficients, the input, and the amount of bit shift of the output.

Figure SCU (Sensor Control Unit)-62 shows the internal data flow of the 2nd order IIR filters.

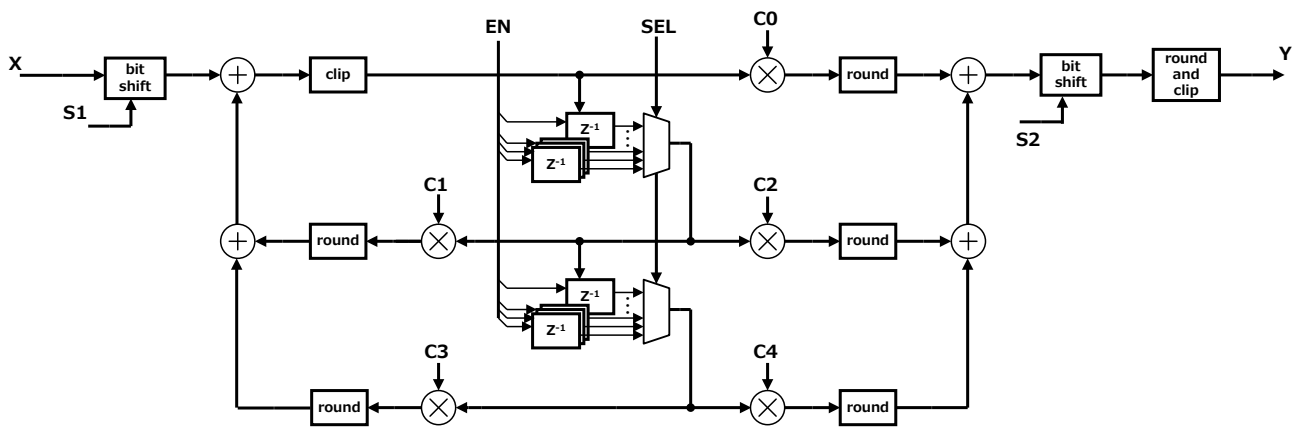


Figure SCU (Sensor Control Unit)-64 2nd Order IIR Filter Internal Data Flow

3.9.7.3.2 Normalization Processing

The normalization processing performs simplified conversion of multiple axis (2 axis/3 axis) data to single axis values.

The square sum of each axis becomes a circle when the two axes have the same values, and becomes a sphere when the three axes have the same value. However, in normalization processing, the values are calculated as approximates to a rectangular octagon when converting from two axes.

- 1st order The absolute value of the input is output as-is
Output = $|x|$
- 2nd order
Output = $123/128 \times \text{Max}(|x|, |y|) + 51/128 \times \text{Min}(|x|, |y|)$
- 3rd order
 $L1 = 120/128 \times \text{Max}(|x|, |y|) + 49/128 \times \text{Min}(|x|, |y|)$
Output = $\text{Max}(L1, |z|) + 44/128 \times \text{Min}(L1, |z|)$

Figure SCU (Sensor Control Unit)-65 shows the data flow of normalization processing.

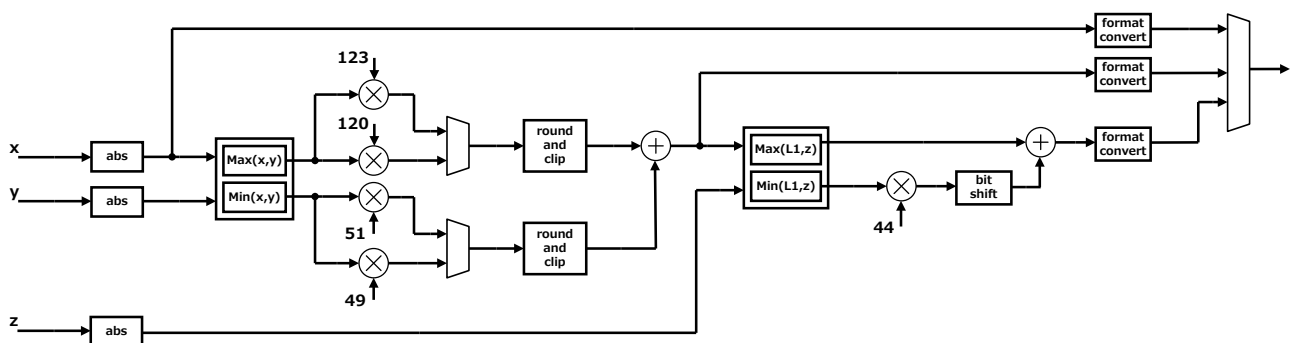


Figure SCU (Sensor Control Unit)-65 Normalization Processing Data Flow

3.9.7.3.3 Excess Detection

The Excess Detection function performs excess detection to the value converted to 1 axis at the normalization processing and then outputs an interrupt to the upper module. Also, the result of this conversion can be used for writing control to the FIFO.

There are two thresholds in the internal comparator. The comparator determines whether the target input value is bigger than top threshold or smaller than bottom threshold or not. Next to the comparator, two circuits are connected in two-step cascade connection. They detect whether the “true” result of the comparator’s determination occurs for the specified number of times in series. The output from the second circuit becomes to be the determination. By using registers, you can delay the interrupt occurrence which is output in response to the determination.

The occurrence of the two interrupts: Rise interrupt which indicates the transition from Low to High, and Fall interrupt which indicates the transition from High to Low, can be selected independently.

Figure SCU (Sensor Control Unit)-66 shows an example of the input value’s change with time and the operation of the excess detection.

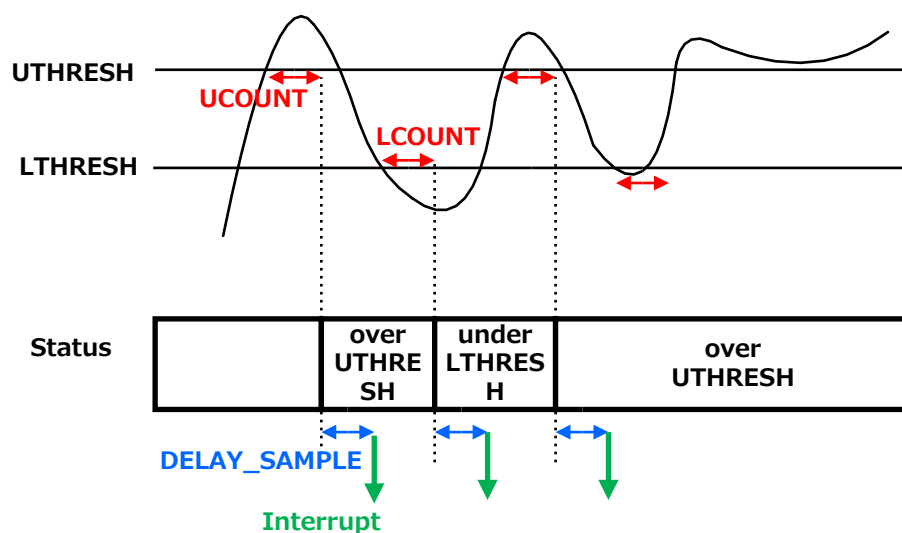


Figure SCU (Sensor Control Unit)-66 Excess Detection Operation (by a Comparator and an Excess Detector)

The Excess Detection function of the MATH_PROC actually has a different interrupt output from the above Figure because the excess detection is operated with two-step cascade connection.

Figure SCU (Sensor Control Unit)-67 shows the operation of excess detection in two-step cascade connection.

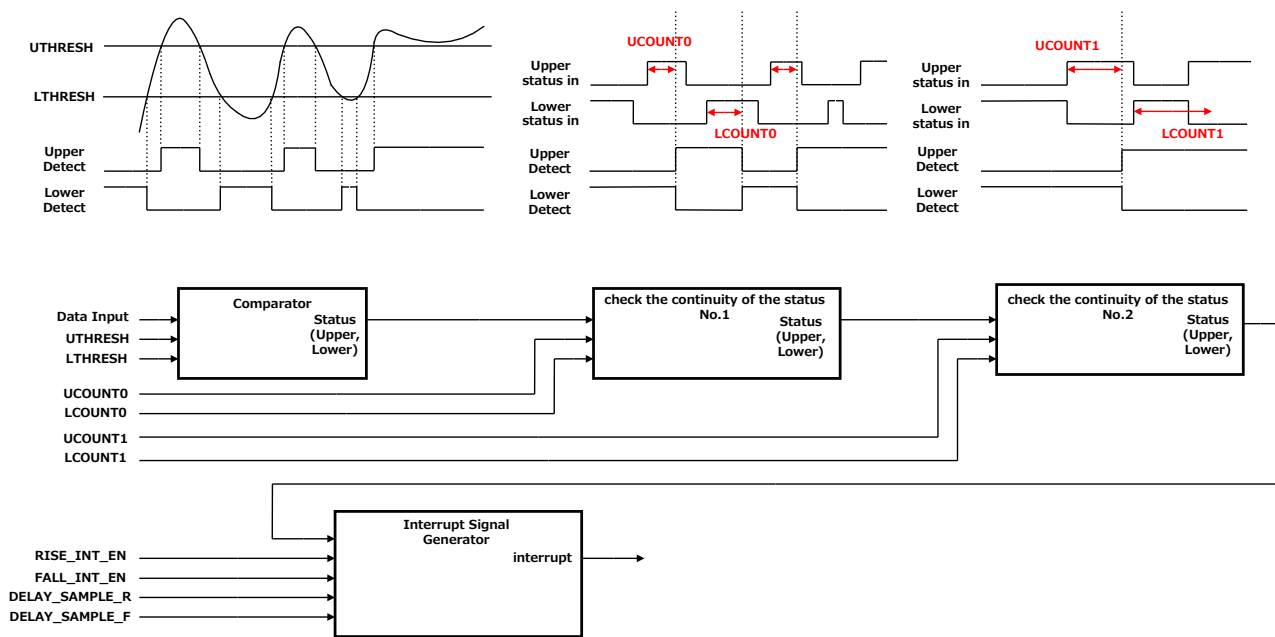


Figure SCU (Sensor Control Unit)-67 Excess Detection Operation (Two-step Cascade Connection)

In the two-step cascade connection, the first step of detection is called “Status Continuity Determination 0” and the second step is called “Continuity Determination 1”.

The following explains the details of interrupt occurrence conditions using Rise interrupt as an example.

Precondition:

UCOUNT0 ... Number of status continuity of the top threshold of the status continuity determination 0
 LCOUNT0 ... Number of status continuity of the bottom threshold of the status continuity determination 0
 UCOUNT1 ... Number of status continuity of the top threshold of the status continuity determination 1
 DELAY_SAMPLE_R ... Delay of Rise interrupt occurrence

- When $UCOUNT0 == 0$, a Rise interrupt occurs regardless of the $UCOUNT1/DELAY\_SAMPLE\_R$ setting value.
- When $UCOUNT0 \geq 1$ and $UCOUNT1 == 0$ and $DELAY\_SAMPLE\_R == 0$, a Rise interrupt occurs immediately after the detection results of continuous match detection 0 changes to upper.

E.g.: When $UCOUNT0=2/UCOUNT1=0/DELAY\_SMAPLE\_R=0$, a Rise interrupt occurs when Upper data is input two samples in a row.

- When $UCOUNT0 \geq 1$ and $UCOUNT1 \geq 1$ and $DELAY\_SAMPLE\_R == 0$, a Rise interrupt occurs when the detection results of continuous match detection 0 changes to Upper, and the results of continuous match detection 0 remain in upper state for $UCOUNT1-1$ samples.

E.g.: When $UCOUNT0==2/UCOUNT1==4/DELAY\_SMAPLE\_R==0$

A Rise interrupt occurs when Upper data is input two samples in a row, and Upper data continues for three samples after.

When Upper data is input two samples in a row, and Lower data continues for LCOUNT0 times or more within three samples, the UCOUNT conditions are not referenced and the continuous match count of UCOUNT1 returns to its initial value.

- The startup condition of the counter which counts delay time is set as shown below.
(($UCOUNT0 \geq 1$ and $UCOUNT1==0$ and the results of status continuity determination 0 is "Upper") or ($UCOUNT0 \geq 1$ and $UCOUNT1 \geq 1$ and the results of status continuity determination 1 is "Upper"))

- When $DELAY\_SAMPLE\_R \geq 1$

When the startup condition of the counter written above is satisfied, the DELAY_SAMPLE_R counter turns to operation state, and regardless of the input data, a Rise interrupt occurs after the DELAY_SAMPLE_R sample, and the DELAY_SAMPLE_R counter enters a stop state.

E.g.: When $UCOUNT0=2/UCOUNT1=0/DELAY\_SMAPLE\_R=7$ and the detection result is Lower for two consecutive times, a Rise interrupt occurs after seven sample times regardless of the detection result that follows.

E.g.: When $UCOUNT0=2/UCOUNT1=4/DELAY\_SAMPLE\_R=2$ and the detection result is Upper for two consecutive times, "Status Continuity Determination 0" is Upper and this state is held four times (after status changes to "Upper", the detection result is Upper for three consecutive times), a Rise interrupt occurs after two sample times regardless of the detection result that follows.

After Upper data is input two samples in a row, and the Lower data continues for LCOUNT0 times or more within three samples, the UCOUNT conditions are not referenced and the count of the status continuity determination of UCOUNT1 returns to its initial value.

- Delay counter startup triggers that occur during the counter operation of DELAY_SAMPLE_R are ignored.

The Fall interrupt operates in the same way (the settings are exchanged between $UCOUNT \leftrightarrow LCOUNT$, the detection results of the Upper part are re-read as Lower, and DELAY_SAMPLE_R is re-read as DELAY_SAMPLE_L).

[Caution] Do not enter a negative value for the excess detection. The detection result will be incorrect.

3.9.7.4 FIFO Writing

The following FIFO writing conditions can be set in conjunction with the interrupts generated by the excess detection function of the Math Function.

- Stop writing by generating Rise/Fall interrupt
 - Performs writing to the FIFO until an interrupt occurs, and after the interrupt, writes to the FIFO until a specified number of samples.
 - Writing is stopped from the specified number of samples +1 until the FIFO writing control interrupt is cleared.
- Start writing by generating Rise/Fall interrupt
 - Writing to the FIFO is not performed until an interrupt is generated, and writing starts from when the interrupt is generated.
- Writing continues regardless of the generation of Rise/Fall interrupts
- Writing is stopped regardless of the Rise/Fall interrupts

3.9.8 FIFO

3.9.8.1 Overview

The FIFO operation is such that the values written to the writing ports of the two SRAMs (8 KByte + 32 Kbyte each) can be readout from the readout ports in the same order. The SRAMs are divided into regions called “Partitions”, where each one can be used as FIFO. Up to 27 partitions can be used.

3.9.8.2 FIFO Writing Data Types

The data unit that can be written to the FIFO is defined as a “Sample”. Each Sample must use one of the “data types” listed below.

(1) Calculation Operable Sample Type

16-bit 1 axis: 1 Sample = {x} format	(2 Byte/Sample)
16-bit 2 axis: 1 Sample = {x,y} format	(4 Byte/Sample)
16-bit 3 axis: 1 Sample = {x,y,z} format	(6 Byte/Sample)

(2) Calculation Inoperable Sample Type

24-bit : 1 Sample format	(3 Byte/Sample)
32-bit : 1 Sample format	(4 Byte/Sample)
48-bit : 1 Sample format	(6 Byte/Sample)
64-bit : 1 Sample format	(8 Byte/Sample)
96-bit : 1 Sample format	(12 Byte/Sample)

128-bit : 1 Sample format (16 Byte/Sample)

3.9.8.3 Partition

The SRAM for the FIFO has up to 27 partitions.

The partitions are classified as follows:

- (1) Decimation Partitions ⋯ x 4 partitions x 2 sets (Total: 8 partitions)
- (2) Normal Sensor Partitions ⋯ x 8 partitions
- (3) Virtual Sensor Partitions ⋯ x 10 partitions
- (4) Random Access Partitions ⋯ x 1 partition

The region of each partition is allocated by specifying an arbitrary address size from the 40 Kbytes of SRAM. The allocation must be done under the following conditions.

- The partition regions must not overlap
- Each partition size must be equal to or larger than the value 1 and must be an integral multiple of the Sample size.
- The writing port and readout port must have a one-to-one relation, and the readout ports that are not used must be set to disable.
- When performing power supply control of the SRAM, the partition region must not be set across the 8 Kbytes and 32 Kbytes of the two SRAMs.

The number of each partition's writing ports/readout ports depends on the type of the partition. For clarification, Table SCU (Sensor Control Unit)-102 shows the mnemonics for each partition name and by each writing port/readout port.

Table SCU (Sensor Control Unit)-94 Partition Name and Writing Port/Readout* Port

Partition Type	Partition Name	Write	Read0	Read1	Read2	Read3
Decimation Partition	D0	D0_W0_S	D0_R0_H	D0_R1_C	D0_R2_C	D0_R3_CH
		D0_W1_S				
		D0_W2_S				
		D0_W3_S				
	D1	D1_W0_S	D1_R0_H	D1_R1_C	D1_R2_C	D1_R3_CH
		D1_W1_S				
		D1_W2_S				
		D1_W3_S				
Normal Sensor Partition	N0	N0_W_S	N0_R0_H	N0_R1_C	Not Available	Not Available
	N1	N1_W_S	N1_R0_H	N1_R1_C	Not Available	Not Available
	N2	N2_W_S	N2_R0_H	N2_R1_C	Not Available	Not Available

		N3	N3_W_S	N3_R0_H	N3_R1_C	Not Available	Not Available
		N4	N4_W_S	N4_R0_H	N4_R1_C	Not Available	Not Available
		N5	N5_W_S	N5_R0_H	N5_R1_C	Not Available	Not Available
		N6	N6_W_S	N6_R0_H	N6_R1_C	Not Available	Not Available
		N7	N7_W_S	N7_R0_H	N7_R1_C	Not Available	Not Available
virtual Sensor Partition	V0	V0_W_C	V0_R_H	Not Available	Not Available	Not Available	Not Available
	V1	V1_W_C	V1_R_H	Not Available	Not Available	Not Available	Not Available
	V2	V2_W_C	V2_R_H	Not Available	Not Available	Not Available	Not Available
	V3	V3_W_C	V3_R_H	Not Available	Not Available	Not Available	Not Available
	V4	V4_W_C	V4_R_H	Not Available	Not Available	Not Available	Not Available
	V5	V5_W_C	V5_R_H	Not Available	Not Available	Not Available	Not Available
	V6	V6_W_C	V6_R_H	Not Available	Not Available	Not Available	Not Available
	V7	V7_W_C	V7_R_H	Not Available	Not Available	Not Available	Not Available
	V8	V8_W_C	V8_R_H	Not Available	Not Available	Not Available	Not Available
	V9	V9_W_C	V9_R_H	Not Available	Not Available	Not Available	Not Available
Random Access Partition	R0	R0_W_CH	R0_R_CH	Not Available	Not Available	Not Available	Not Available

The one to two character suffix of the mnemonic describes the access privileges for the given writing port/readout port as follows:

- "S" For partitions that can be written to from the SCU
- "C" For partitions that can be written to/readout from the CPU
- "H" For partitions that can be readout from the Host
- "CH" For partitions that can be written to/readout from by selecting the CPU or Host

Table SCU (Sensor Control Unit)-103 shows the addresses of each partition's readout ports and writing ports.

Table SCU (Sensor Control Unit)-95 Writing Port and Readout Port Addresses

Writing Port Address	Writing Port Mnemonic	Readout Port Address	Readout Port Mnemonic	Readout Port Address	Readout Port Mnemonic
0x2000	D0_W0_S	0x2100	D0_R1_C	0x2160	V0_R_H
0x2004	D0_W1_S	0x2104	D0_R2_C	0x2164	V1_R_H
0x2008	D0_W2_S	0x2108	D1_R1_C	0x2168	V2_R_H
0x200C	D0_W3_S	0x210C	D1_R2_C	0x216C	V3_R_H
0x2010	D1_W0_S	0x2110	N0_R1_C	0x2170	V4_R_H
0x2014	D1_W1_S	0x2114	N1_R1_C	0x2174	V5_R_H
0x2018	D1_W2_S	0x2118	N2_R1_C	0x2178	V6_R_H
0x201C	D1_W3_S	0x211C	N3_R1_C	0x217C	V7_R_H
0x2020	N0_W_S	0x2120	N4_R1_C	0x2180	V8_R_H

0x2024	N1_W_S	0x2124	N5_R1_C	0x2184	V9_R_H
0x2028	N2_W_S	0x2128	N6_R1_C		
0x202C	N3_W_S	0x212C	N7_R1_C		
0x2030	N4_W_S	0x2130	D0_R3_CH		
0x2034	N5_W_S	0x2134	D1_R3_CH		
0x2038	N6_W_S	0x2138	D0_R0_H		
0x203C	N7_W_S	0x213C	D1_R1_H		
0x2040	V0_W_C	0x2140	N0_R0_H		
0x2044	V1_W_C	0x2144	N1_R0_H		
0x2048	V2_W_C	0x2148	N2_R0_H		
0x204C	V3_W_C	0x214C	N3_R0_H		
0x2050	V4_W_C	0x2150	N4_R0_H		
0x2054	V5_W_C	0x2154	N5_R0_H		
0x2058	V6_W_C	0x2158	N6_R0_H		
0x205C	V7_W_C	0x215C	N7_R0_H		
0x2060	V8_W_C				
0x2064	V9_W_C				

Among the FIFO access space (Addresses 0x2000 to 0x2FFF), the addresses not shown in Table SCU (Sensor Control Unit)-103 are Reserved and are writing-invalid (no error response) and 0 read during readout (no error response).

Since the Random Access partition has a non-FIFO structure, it does not have physical writing ports or physical readout ports.

3.9.8.4 Decimation Partition

The Decimation partition stores the data that was decimation-processed by the MATH_PROC. There are two sets of Decimation partitions, each of which is comprised of four sub-partitions.

Within each sub-partition of the Decimation partition, data can be stored as either Calculation Operable Sample Type or Calculation Inoperable Sample Type but when performing decimation or arithmetic processing, Calculation Operable Sample Type must be used.

The Decimation partition can only be written from the internal sequencer of the SCU, and writing from the CPU or Host is prohibited. The four sub-partitions within a certain Decimation partition stores sample data that differs in terms of decimation rate based on the same sample data.

The Decimation partition has four different readout ports per partition, each to which one of the four sub-partitions can be assigned according to the setting.

- CPU dedicated readout port x 2
- Host dedicated readout port x 1
- CPU or Host readout port x 1

[Caution] The writing port and readout port must have a one-to-one relation. In the reset initial state, all readout ports are connected to the same readout port Dn_W0_S (n=0,1). Therefore, be sure to make the proper settings.

3.9.8.5 Virtual Sensor Partition

The Virtual Sensor partition allows the storage of arbitrary data (Virtual Sensor data) and there are 10 of these partitions. This partition can store data as either Calculation Operable Sample Type or Calculation Inoperable Sample Type.

Writing to the Virtual Sensor partition is only possible from the CPU. Writing from the Host is prohibited. The Virtual Sensor partitions have only one readout port for the Host per partition.

3.9.8.6 Random Access Partition

The Random Access partition can be used for data communication between the Host and CPU, and only one of 27 partitions can be set as the Random Access partition. The Random Access partition has a non-FIFO structure, and data can be randomly written and readout to/from the CPU or Host.

Reading/Writing access is possible by selecting an arbitrary address from the 40 Kbytes of the SRAM. However, caution is required so that the data of other partitions is not corrupted by exceeding the region secured for the Random Access partition.

The Random Access partition is used as a buffer region for communication between the Host and CPU.

3.9.8.7 Partition Common Specifications (other than the Random Access Partition)

When writing a value to the FIFO write register (Writing Port), the value is stacked in the FIFO.

The behavior when writing data during FIFO Full can be selected from the following:

- (1) Data writing failed, and older data is stored
- (2) The oldest data is overwritten

For readout, there are either one or multiple readout ports depending on the type of the partition.

When reading out from the FIFO readout register (Readout Port), the oldest data corresponding to that port can be readout.

Each readout port has the following functions.

- Manages the readout positions separately

- Valid data amount can be readout separately
- Watermark Level (Almost Full) can be set separately
- Interrupts/DMA transfer requests such as the following can be generated separately
 - When the valid data amount becomes equal to or higher than the Watermark, an interrupt is asserted, and when it falls below the Watermark, an interrupt is negated.
 - When the valid data amount becomes equal to or higher than the Watermark, DMA_BREQ is asserted, and when 1 or larger, DMA_SREQ is asserted.
 - When the DMA_CLR from the DMAC becomes “1”, the DMA_BREQ and DMA_SREQ are once negated, and the DMA_BREQ and DMA_SREQ are asserted again in accordance with the valid data amount.
- FIFO Clear (setting is enforced as valid data amount = 0) can be performed separately
- Equips a separate time stamp readout register
- From the time stamp readout register, the value that corresponds to the below readable data can be obtained.
- The time stamp value is calculated from the following formula:
“the time stamp that corresponds to the latest value - (valid data amount - 1) x data capture interval”

3.9.8.8 Time Stamp

Each partition excluding the Random Access partition has time stamp information.

Time stamps are count values of 47 bits that are incremented at 32.768 kHz intervals. The upper 32 bits indicate “integer part of second” while the lower 15 bits are values of “second after the decimal point”.

3.9.8.8.1 Time Stamp Value Handling at the Writing Side

The partition to which data is written from the SCU (internal sequencer) is directly connected to the time stamp information supplied from the other block, and the writing side time stamp information is updated according to the data writing timing.

The partition to which data is written from the CPU has the following registers which can be set from the CPU.

- Reference time stamp value
- Writing time interval value

The CPU first writes the reference time stamp value and writing time interval value. Then, each time the CPU writes data to the FIFO, the writing time interval value is cumulatively added to the reference time stamp value. The cumulatively added time stamp value can be read out as the register value by the CPU.

Time stamp generation logic when reading out

Within the FIFO, the time stamp values of each datum are not stored together in the FIFO, instead, the writing side (latest) time stamp values and the writing time interval values are stored.

The readout side time stamps are values calculated during readout by the following equation.

Writing side (= latest) time stamp – (valid data samples – 1) x writing time interval

3.9.8.9 FIFO Block Diagram

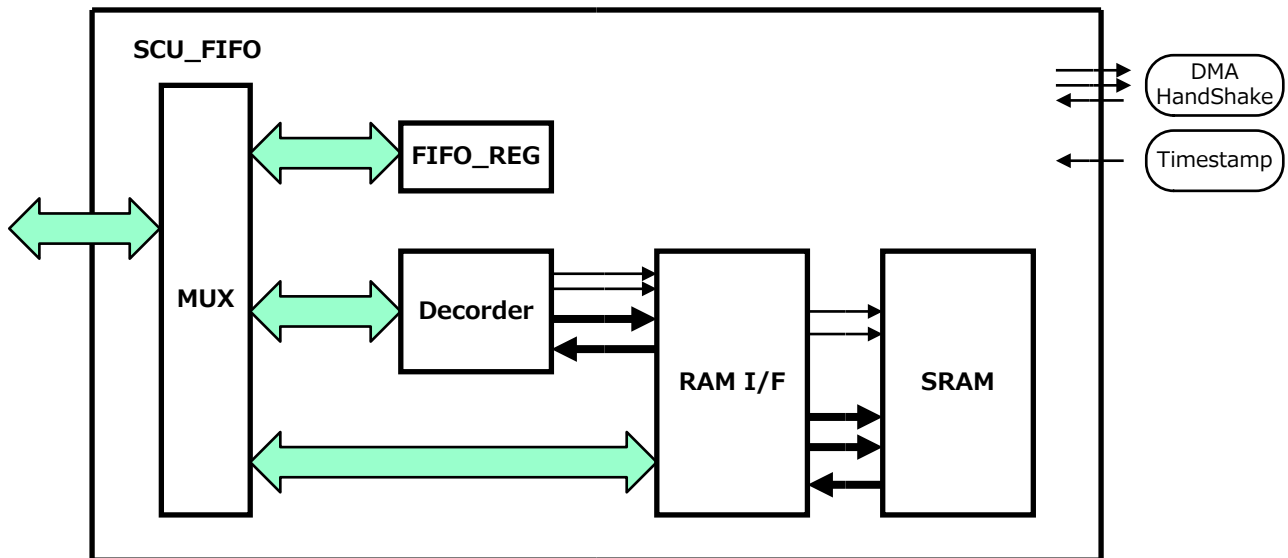


Figure SCU (Sensor Control Unit)-68 FIFO Block Diagram

3.9.8.10 FIFO Points of Attention

- The partition regions must not overlap.
- The partition size must be 1 or larger, and must be an integral multiple of the sample size.
- The writing port and readout port must have a one-to-one relation, and the readout ports that are not used must be disabled.
- When performing power supply control of the SRAM, do not set the partition region across the 8 Kbyte and 32 KByte SRAMs.
- When performing a Clear to the FIFO writing port, also make sure to perform a Clear to the corresponding readout port.
- When changing FIFO_ENABLE from Disable to Enable, make sure to perform a Clear to the FIFO readout port.
- Do not set the WATER_MARK register to “0”.

3.9.9 Sequencers

The sequencers intermittently capture sensor data from the external sensors connected to the SPI, I2C or analog input using the specified time intervals as triggers.

Data Transfer Function

- Reads the data from the I2C/SPI and transfers it to the FIFO
 - Data can be transferred periodically according to the interrupt from the SCU_CTRL.
- In accordance with the process request from the CPU, data can be read from the I2C/SPI (only one time) and transferred to the FIFO (One-shot Operation)
 - Completion of the transfer is notified when the transfer completes.
- Reads data from the ADCIF (data to which AD conversion is applied at the AD converter) and transfers it to the FIFO (AD data transfer)
- MATH_PROC processing can be performed before the data is transferred to the FIFO.
 - Inputs data to the MATH_PROC and takes out the results and writes to the FIFO
 - Judges whether or not to write to the FIFO according to the event output from the MATH_PROC

Data Duplication Function

- The ID of Write FIFO to which the data output from each sequencer is written is already specified. However, this function allows the output to be duplicated to one other Write FIFO.

Data Processing Function

- When the data is sent to the MATH_PROC, a maximum data size of 6 Bytes can be Byte Swapped or Left Bit Shifted in units of 2 Bytes before input to the MATH_PROC.
Note: Since the data processing within the MATH_PROC is performed by the hardware other than the sequencer, the internal sequencer is not involved.

Other Functions

- SCU-CPU Synchronization Function
 - When one cycle of the sequencer operation is completed, an interrupt notification is sent to the CPU (suspend interrupt)
After sending the suspend interrupt, if the CPU cannot clear the suspend interrupt request by the next time the MATH_PROC starts up, an error flag within the SCU_RAM is asserted, and the error is notified to the CPU.
 - When the sequencer's periodic startup has been completed and a separate startup request is not sent from the CPU, an interrupt notification is sent to the CPU (complete interrupt).

The following shows the five main operations of the sequencer in the order they are executed.

- (1) Startup control
 - (2) External bus transaction generation
 - (3) External data capture
 - (4) MATH_PROC processing
 - (5) FIFO writing
-

Among these processes, the Startup control is fully implemented in the hardware while the other operations are implemented in the software of the sequencer controller.

There are 10 independent sequencers within the sequencer, each to which separate startup control and sensor polling settings are possible.

Figure SCU (Sensor Control Unit)-69 shows the overall processes of the sequencers.

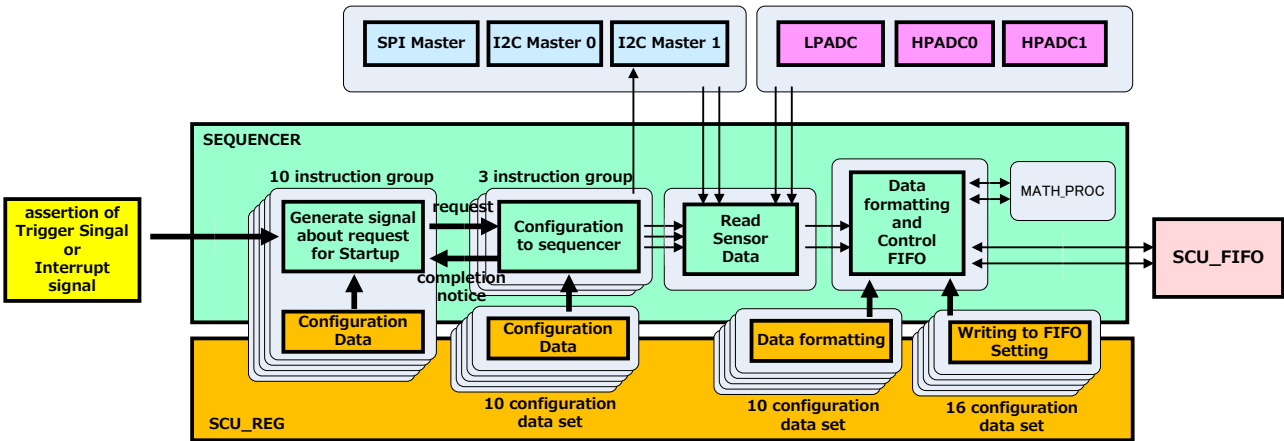


Figure SCU (Sensor Control Unit)-69 Sequencer Overall Image

Figure SCU (Sensor Control Unit)-70 shows an example of the process. The SEQ ID0 operates periodically according to the timer, and the data from the I2C is captured. The SEQ ID1 starts up by a certain trigger and captures the data of the LPADC FIFO.

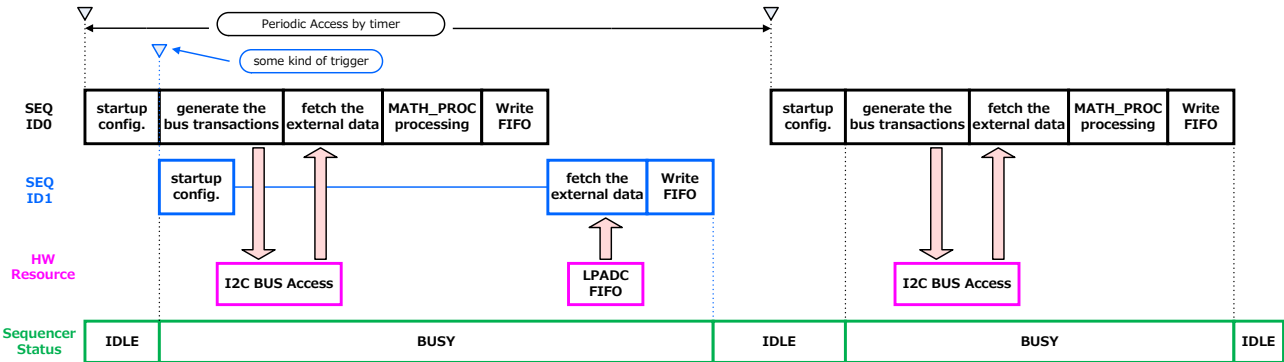


Figure SCU (Sensor Control Unit)-70 Sequencer Process Flow (Example)

The 10 sequencer requests startup independently. However, afterwards, the sequences are processed one at a time in order because each process of the external bus transaction generation, external data capture, MATH_PROC processing, and FIFO writing are executed by the sequencer software.

The normal (excluding the duplication function) data flow is shown below.

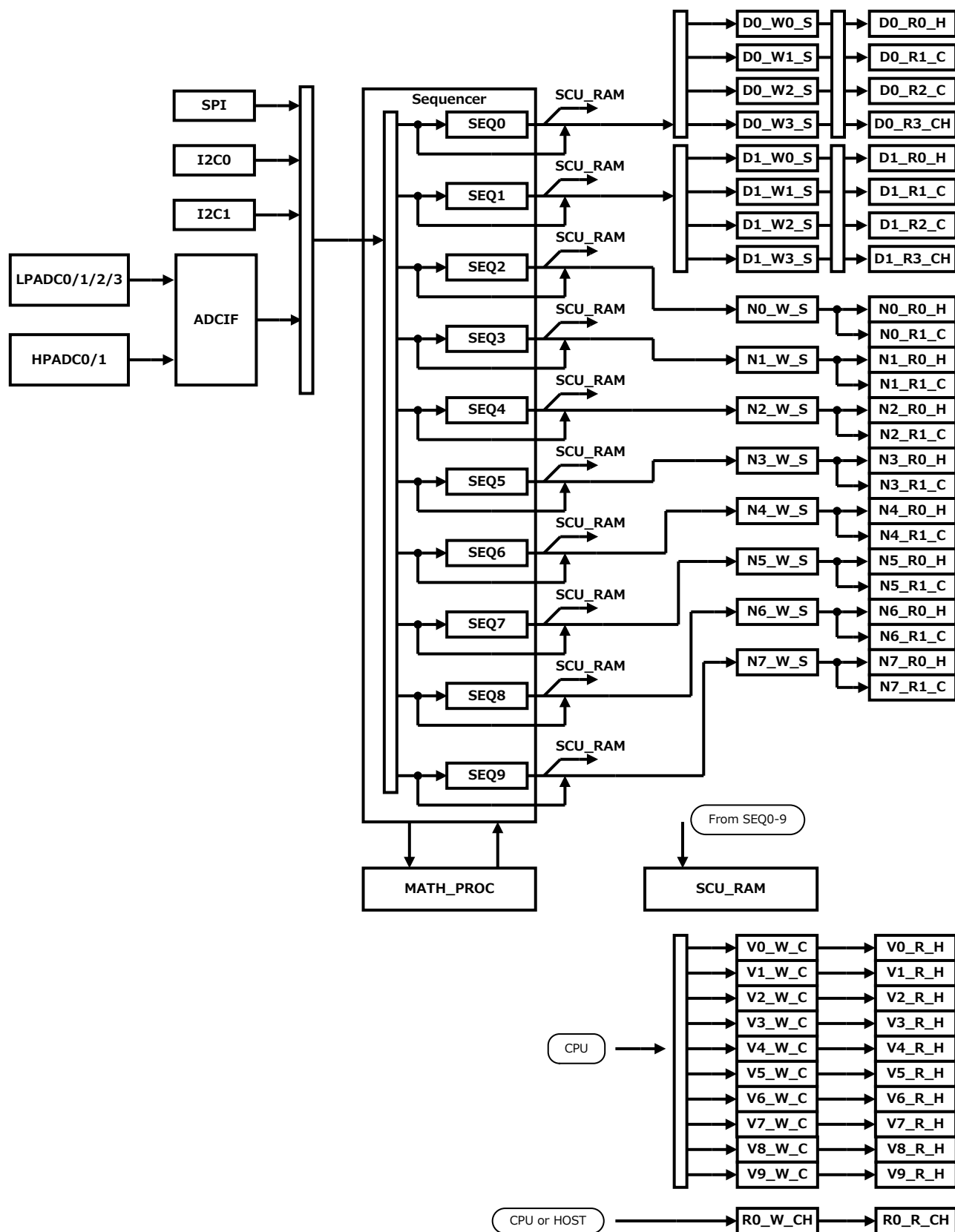


Figure SCU (Sensor Control Unit)-71 Overall Data Flow (excluding Data Duplication Function)

3.9.9.1 Startup Control

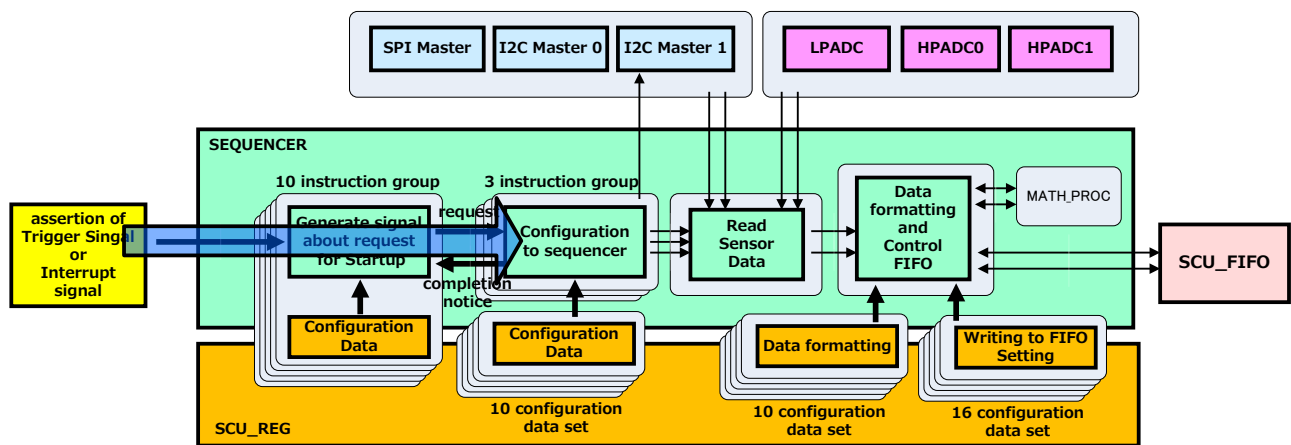


Figure SCU (Sensor Control Unit)-72 Startup Control

A startup request occurs for each SEQ_ID under any of the following conditions.

- A certain cycle by the timer
- A certain cycle by the timer after receiving an external interrupt as the trigger
- One operation using an external interrupt as the trigger
- One operation using the register writing operation as the trigger, which is from the CPU

The startup intervals by the timer can be selected using the frequency division value of the Pre Divider that determines the startup maximum frequency.

The operating frequency of each sequencer can be selected by the frequency of the 2nd power of the frequency divided by the Pre Divider.

When the sequencer is started up by the startup request, the process is branched into each physical interface shown below according to the setting value that is set on the SCU_RAM and hands over the external bus transaction process.

- SPI
- I2C0
- I2C1

When either LPADC or HPADC is selected as the physical interface, it does not branch into the external bus transaction generation process, and the sequencer control program moves to external data capture process.

3.9.9.2 External Bus Transaction Generation

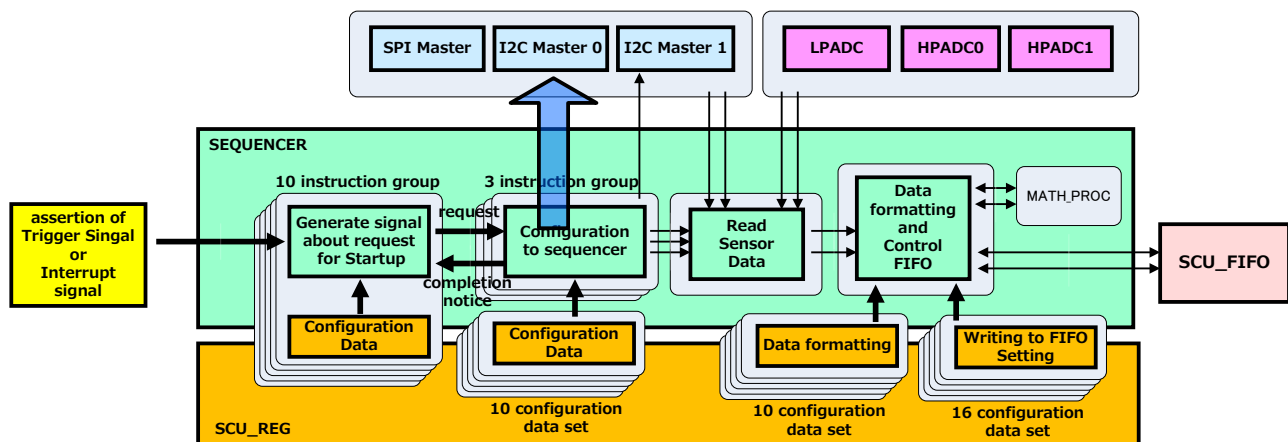


Figure SCU (Sensor Control Unit)-73 External Bus Transaction Generation

At the External Bus Transaction Generation process, the bus transaction can be controlled for each physical interface according to the setting value written on the SCU_RAM.

The SPI and I2C (I2C0, I2C1) access sequencers can be issued by combining the below sequence commands.

- TX_RX command
 - In the case of SPI, the selected data is output from the MOSI terminal and up to 8 Bytes of data are simultaneously captured from the MISO terminal.
 - In the case of IC2, the selected data is either output to the I2C bus, or up to 8 Bytes of data are captured from the I2C bus. The slave address (and R/W selected) is also output as data handled by the TX_RX command.
 - In the case of continuous transfers, the TX_RX command can be executed continuously for multiple times. You can freely select whether to turn OFF the CS in the case of SPI, or send a Stop Condition in the case of I2C.
- WAIT command
 - Waits for the specified time

These commands are interpreted by the internal sequencer, converted to the APB access processing of the SPI or I2C, to perform the actual data transfer processing.

3.9.9.3 External Data Capture

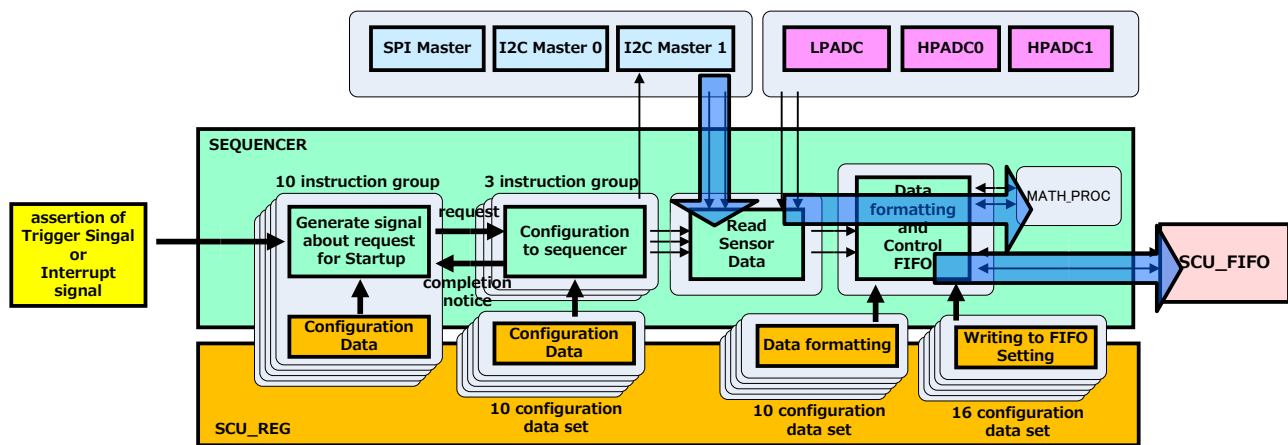


Figure SCU (Sensor Control Unit)-74 External Data Capture

At the External Data Capture processing, the data from each sensor connected to each physical interface is readout, and the data is written to the FIFO via the MATH_PROC processing, or directly from the sensor to the FIFO.

Regardless of writing the data via the MATH_PROC or directly from the sensor to the FIFO, the data type must be one of the following “Calculation Operable Sample Types” or “Calculation Inoperable Sample Types”. Other data types cannot be handled.

Also, when the data is written via the MATH_PROC processing, the data type of the sensor readout data (the data handed to the MATH_PROC) must be the Calculation Operable Sample Type.

- Calculation Operable Sample Types
 - 16-bit 1 axis: 1 Sample = {x} format (2 Byte/Sample)
 - 16-bit 2 axis: 1 Sample = {x,y} format (4 Byte/Sample)
 - 16-bit 3 axis: 1 Sample = {x,y,z} format (6 Byte/Sample)
- Calculation Inoperable Sample Types
 - 24-bit: 1 Sample format (3 Byte/Sample)
 - 32-bit: 1 Sample format (4 Byte/Sample)
 - 48-bit: 1 Sample format (6 Byte/Sample)
 - 64-bit: 1 Sample format (8 Byte/Sample)
 - 96-bit: 1 Sample format (12 Byte/Sample)
 - 128-bit: 1 Sample format (16 Byte/Sample)

From the SPI/I2C sensors, up to 16 Bytes of data can be readout in one process.

Data readout from the LPADC is treated as MSB-aligned 16 bit data.

For the data readout from the HPADC, vector mode or non-vector mode can be selected. When vector mode is

selected, the data is treated as 16 bit 2 axis data. When non-vector mode is selected, the data is treated as MSB-aligned 16 bit data for each channel. In the case of vector mode, the data readout from HPADC0 is allocated to the LSB side ({x}) and the data readout from HPADC1 is allocated to the MSB side ({y}).

You can select whether or not to apply the MATH_PROC processing by the MATH_PROC setting.

Figure SCU (Sensor Control Unit)-75 shows the flow of the sensor data when capturing the external data.

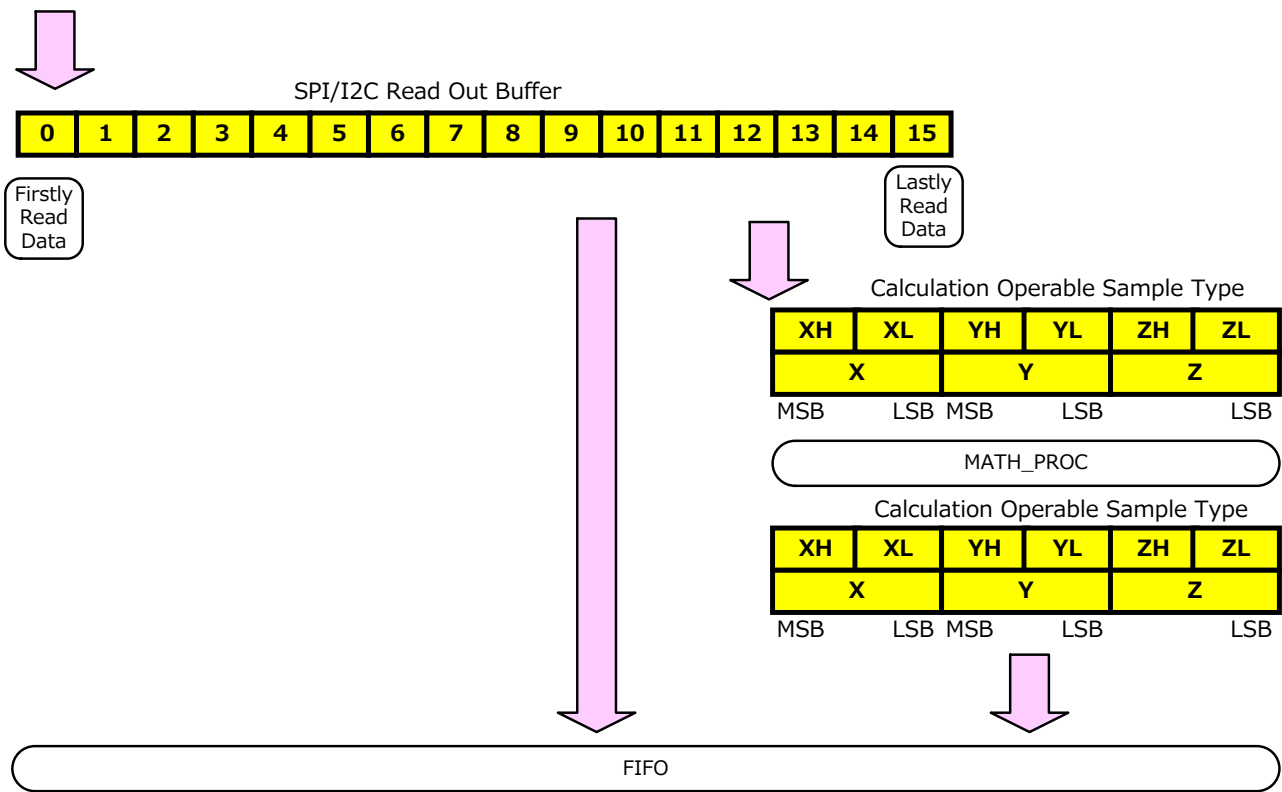


Figure SCU (Sensor Control Unit)-75 Sensor Data Flow when Capturing External Data

When the data captured by the SPI, I2C, LPADC, or HPADC is sent through the MATH_PROC, take out a maximum of 6 Bytes of continuous data from the selected capture start position, then perform Byte Swap and left shift in units of 2 Bytes (see Section 3.9.12.11.6), and perform the data normalization processing. Figure SCU (Sensor Control Unit)-76 shows an example of data normalization of transferring data 2 Bytes at a time from a 12 bit data sensor.

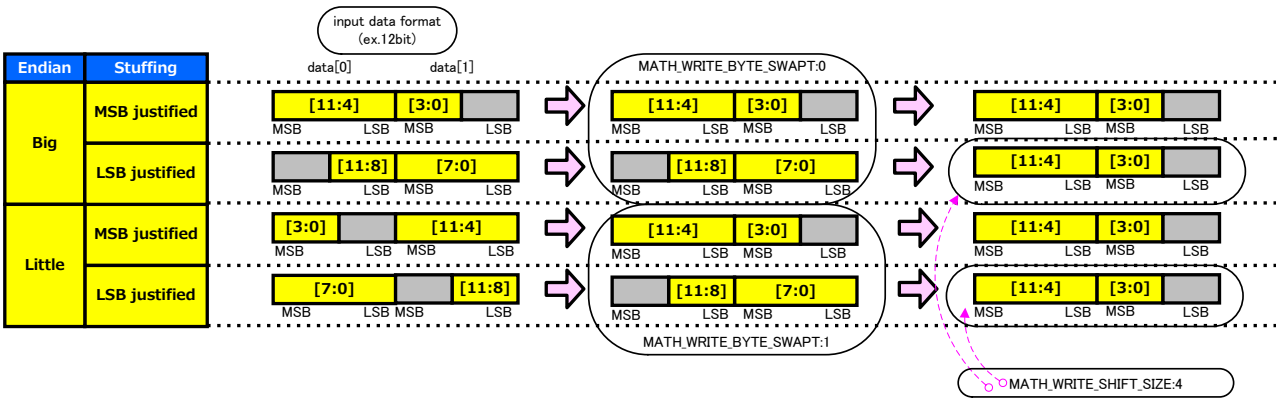


Figure SCU (Sensor Control Unit)-76 Data Normalization (Example)

When the data is not passed through the MATH_PROC, the offset and writing length can be selected for a maximum of 16 Bytes of data that was captured by the SPI, I2C, LPADC, or HPADC.

The data ultimately written to the FIFO, when not passed through the MATH_PROC, is written in the readout order from the sensor.

When passed through the MATH_PROC, you can select from 16 bits or 8 bits for each element (bits per axis). (OUTPUT_8BIT of Section 3.9.12.11.11.)

When 16 bits is selected for each element, writing is performed in the X,Y,Z order from the LSB side byte.

When 8 bits is selected for each element, the MSB side 8 bits of each X,Y, and Z are written in X,Y,Z order.

Figure SCU (Sensor Control Unit)-77 shows how the data is ultimately stacked in the FIFO.

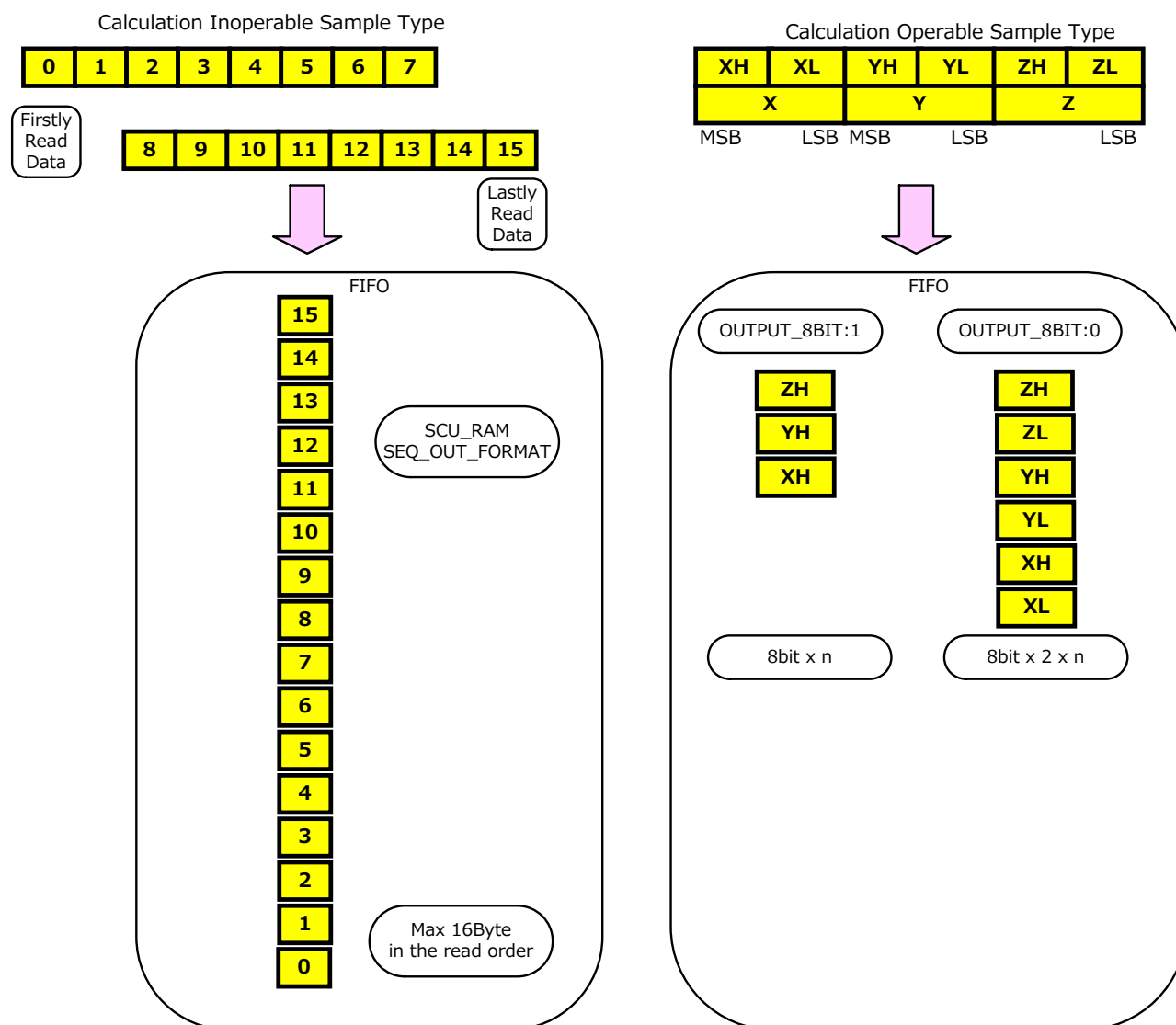


Figure SCU (Sensor Control Unit)-77 Data Stacked in the FIFO (Image)

3.9.9.4 Connectable Sequencers

3.9.9.4.1 I2C

The I2C0 and I2C1 can be connected to any sequencer from SEQ0 to SEQ9.

See Section 3.9.9.8 for the data flow.

The I2C execution command must be set beforehand in the parameter SEQ_INSTRUCTION_n (n is the instruction number, n = 0, ..., 127) within the SCU_RAM. At each sequencer, set this instruction number in the parameter SEQ_PROPERTY_n.INST_OFST (n is the sequencer number, n = 0, ..., 9) within the SCU_RAM.

For the I2C macro, set the fastest baud rate calculated from the frequency of the SCU clock, and when reading out 6 Bytes from the 3 axis sensor, use the total of approximately 2,200 clock cycles for the I2C transfer. Also,

when intentionally inserting a STOP command, an overhead of approximately 570 cycles (when RCOSC is 8.192 MHz) occurs due to resending the slave address.

3.9.9.4.2 SPI

The SPI can be connected to the any sequencer from SEQ0 to SEQ9.
For the data flow, refer to Section 3.9.9.8.

The execution command must be set beforehand in the parameter SEQ_INSTRUCTION_n (n is the instruction number, n = 0, ..., 127) within the SCU_RAM. At each sequencer, set this instruction number in the parameter SEQ_PROPERTY_n.INST_OFST (n is the sequencer number, n = 0, ..., 9) within the SCU_RAM.

3.9.9.4.3 ADC

When reading out data from the ADC, the resources of the sequencers are not used. However, the sequencers using the same FIFO numbers cannot be used, because the FIFO connected to the sequencers are occupied when the readout data is written. However, One-shot Operation using the sequencer number assigned for ADC readout is possible.

The LPADC can connect to the following FIFOs.

- D0_W0_S
- D1_W0_S
- from N0_W_S to N7_W_S

The LPADC can also connect to the following FIFOs via the MATH_PROC.

- D0_W1_S
- D0_W2_S
- D0_W3_S
- D1_W1_S
- D1_W2_S
- D1_W3_S

The HPADC can connect to the following FIFOs.

- from N0_W_S to N7_W_S

For the ADC data flow, refer to the Chapter on ADC (3.21).

3.9.9.5 One-shot Sequence

A total of three channels of One-shot Sequencer is equipped.
The instructions of the sequencer are executed only one time by the startup command from the CPU. The

operation of writing the transfer data to the SEQ_RAM_OUT_n_READ_DATA_m (n is the One-shot Sequencer number n = 0, ..., 2, m is the Byte offset of the data readout m = 0, ..., 3, refer to Table SCU (Sensor Control Unit)-690) within the SCU_RAM is called “One-shot Operation” and the block that executes this is called the “One-shot Sequencer”. The One-shot Sequencer can only be selected on the SPI or I2C.

The data cannot be passed through the MATH_PROC in One-shot Operation.

Since the One-shot Operation does not use the Write FIFO, the ADC can be assigned to the same sequencer number and used at the same time.

The execution command must be set beforehand in the parameter SEQ_INSTRUCTION_n (n is the instruction number, n = 0, ..., 127) within the SCU_RAM. After this, set the SEQ_MODEn (n = 0, ..., 9) to “2” or “3”, then set the START_INTERVALn (n = 0, ..., 9) to 0xA, and finally, write “1” to the sequencer number bit that corresponds to the SINGLE_EXE register. This will start the operation. When One-shot Operation is completed, an iSoP0/1/2 interrupt is notified in accordance with the writing region of the SCU_RAM.

3.9.9.6 Sequencer Settings

The following table shows each resource with its registers and SCU_RAM parameters. For the power supplies of the overall SCU and control of clocks, make the appropriate settings separately.

Table SCU (Sensor Control Unit)-96 Parameters of Sequencer Resources

Sub-resources	Item	Parameter	Descriptions
Sequencer	SCU_REG	START_CTRL_COMMON	Section 3.9.12.3.5
		START_MODE*	Section 3.9.12.3.6 and 3.9.12.3.7
		START_INTERVAL*	Section 3.9.12.3.8, 3.9.12.3.9, and 3.9.12.3.10
		START_PHASE*	Section 3.9.12.3.11, 3.9.12.3.12, 3.9.12.3.13, 3.9.12.3.14, and 3.9.12.3.15
		SEQ_ENABLE_ALL	Section 3.9.12.3.3
		HPADC0_ACCESS_INHIBIT_REQ	address 0x00195024 bit[4]
		HPADC1_ACCESS_INHIBIT_REQ	address 0x00195024 bit[5]
		LPADC_ACCESS_INHIBIT_REQ	address 0x00195024 bit[3] Section 3.9.12.3.4
	TOPREG	TOP_SCU_RAMMODE_STAT	address 0x0214
		SCU_CKEN	address 0x071C
	SCU_RAM	SEQ_SRC_SEL.*	Section 3.9.12.11.4
		SEQ_PROPERTY.*	Section 3.9.12.11.5
		SEQ_OUT_FORMAT.*	Section 3.9.12.11.6
		SEQ_RAM_OUT*	Section 3.9.12.11.13
MATH_PROC	SCU_REG	OFST_GAIN_EN	Section 3.9.12.3.20

		UNSIGNED_TO_SIGNED	Section 3.9.12.3.21
		DEC_CLR	Section 3.9.12.3.22
		MATHFUNC_CLR	Section 3.9.12.3.23
		DECIMATION_PARAM*	Section 3.9.12.3.25 and 3.9.12.3.26
		MATHFUNC_SEL	Section 3.9.12.3.27
		MATHFUNC_POS*	Section 3.9.12.3.28, 3.9.12.3.29, and 3.9.12.3.30
		MATHFUNC_PARAM_*	Section 3.9.12.3.31 to 3.9.12.3.96
		EVENT_PARAM0_THRESH	Section 3.9.12.3.97
		EVENT_PARAM0_COUNT*	Section 3.9.12.3.98, 3.9.12.3.99, and 3.9.12.3.100
		EVENT_PARAM1_THRESH	Section 3.9.12.3.101
		EVENT_PARAM1_COUNT*	Section 3.9.12.3.102, 3.9.12.3.103, and 3.9.12.3.104
		EVENT_PARAM2_THRESH	Section 3.9.12.3.105
		EVENT_PARAM2_COUNT*	Section 3.9.12.3.106, 3.9.12.3.107, and 3.9.12.3.108
	SCU_RAM	SEQ_MATH_PROC_OFST_GAIN	Section 3.9.12.11.7
FIFO	SCU_RAM	FIFO_WRITE_EVENT_CTRL.*	Section 3.9.12.11.11
		FIFO_SRAM_POWER_CTRL.*	Section 3.9.12.11.12
ADC	SCU_RAM	ADC_PROPERTY.*	Section 3.9.12.11.9
		HPADC0_ENABLE	Section 3.9.12.11.9
		HPADC1_ENABLE	Section 3.9.12.11.9
		LPADC_ENABLE	Section 3.9.12.11.9
		ADC_MATH_PROC_OFST_GAIN.*	Section 3.9.12.11.10

Table SCU (Sensor Control Unit)-97 Parameters of ADC Resources

Sub-resource	Item	Parameter	Descriptions
LPADC	ADCIF_REG	LPADC_A*	Refer to the Chapter on ADC (3.21).
		LPADC_D*	
HPADC	ADCIF_REG	HPADC0_A*	
		HPADC0_D*	
		HPADC1_A*	
		HPADC1_D*	

Table SCU (Sensor Control Unit)-98 Parameters of FIFO Resources

Sub-resource	Item	Parameter	Descriptions
FIFO	FIFO_REG	D0_W0_S_CTRL*	Section 3.9.12.10.1 and 3.9.12.10.2
		D0_W1_S_CTRL*	Section 3.9.12.10.6 and 3.9.12.10.7
		D0_W2_S_CTRL*	Section 3.9.12.10.11 and 3.9.12.10.12
		D0_W3_S_CTRL*	Section 3.9.12.10.16 and 3.9.12.10.17
		D1_W0_S_CTRL*	Section 3.9.12.10.21 and 3.9.12.10.22

	D1_W1_S_CTRL*	Section 3.9.12.10.26 and 3.9.12.10.27
	D1_W2_S_CTRL*	Section 3.9.12.10.31, and 3.9.12.10.32
	D1_W3_S_CTRL*	Section 3.9.12.10.36 and 3.9.12.10.37
	N0_W_S_CTRL*	Section 3.9.12.10.41 and 3.9.12.10.42
	N1_W_S_CTRL*	Section 3.9.12.10.46 and 3.9.12.10.47
	N2_W_S_CTRL*	Section 3.9.12.10.51 and 3.9.12.10.52
	N3_W_S_CTRL*	Section 3.9.12.10.56 and 3.9.12.10.57
	N4_W_S_CTRL*	Section 3.9.12.10.61 and 3.9.12.10.62
	N5_W_S_CTRL*	Section 3.9.12.10.66 and 3.9.12.10.67
	N6_W_S_CTRL*	Section 3.9.12.10.71 and 3.9.12.10.72
	N7_W_S_CTRL*	Section 3.9.12.10.76 and 3.9.12.10.77
	V0_W_C_CTRL*	Section 3.9.12.10.81 and 3.9.12.10.82
	V1_W_C_CTRL*	Section 3.9.12.10.88 and 3.9.12.10.89
	V2_W_C_CTRL*	Section 3.9.12.10.95 and 3.9.12.10.96
	V3_W_C_CTRL*	Section 3.9.12.10.102 and 3.9.12.10.103
	V4_W_C_CTRL*	Section 3.9.12.10.109 and 3.9.12.10.110
	V5_W_C_CTRL*	Section 3.9.12.10.116 and 3.9.12.10.117
	V6_W_C_CTRL*	Section 3.9.12.10.123 and 3.9.12.10.124
	V7_W_C_CTRL*	Section 3.9.12.10.130 and 3.9.12.10.131
	V8_W_C_CTRL*	Section 3.9.12.10.137 and 3.9.12.10.138
	V9_W_C_CTRL*	Section 3.9.12.10.144 and 3.9.12.10.145
	V0_W_C_TIMESTAMP_SET*	Section 3.9.12.10.86 and 3.9.12.10.87
	V1_W_C_TIMESTAMP_SET*	Section 3.9.12.10.93 and 3.9.12.10.94
	V2_W_C_TIMESTAMP_SET*	Section 3.9.12.10.100 and 3.9.12.10.101
	V3_W_C_TIMESTAMP_SET*	Section 3.9.12.10.107 and 3.9.12.10.108
	V4_W_C_TIMESTAMP_SET*	Section 3.9.12.10.114 and 3.9.12.10.115
	V5_W_C_TIMESTAMP_SET*	Section 3.9.12.10.121 and 3.9.12.10.122
	V6_W_C_TIMESTAMP_SET*	Section 3.9.12.10.128 and 3.9.12.10.129
	V7_W_C_TIMESTAMP_SET*	Section 3.9.12.10.135 and 3.9.12.10.136
	V8_W_C_TIMESTAMP_SET*	Section 3.9.12.10.142 and 3.9.12.10.143
	V9_W_C_TIMESTAMP_SET*	Section 3.9.12.10.149 and 3.9.12.10.150
	V0_W_C_STATUS	Section 3.9.12.10.83
	V1_W_C_STATUS	Section 3.9.12.10.90
	V2_W_C_STATUS	Section 3.9.12.10.97
	V3_W_C_STATUS	Section 3.9.12.10.104
	V4_W_C_STATUS	Section 3.9.12.10.111
	V5_W_C_STATUS	Section 3.9.12.10.118
	V6_W_C_STATUS	Section 3.9.12.10.125

		V7_W_C_STATUS	Section 3.9.12.10.132
		V8_W_C_STATUS	Section 3.9.12.10.139
		V9_W_C_STATUS	Section 3.9.12.10.146
	SCU_REG	D0_R1_C_ALMOST_FULL	Section 3.9.12.3.125
		D0_R2_C_ALMOST_FULL	
		D1_R1_C_ALMOST_FULL	
		D1_R2_C_ALMOST_FULL	
		N0_R1_C_ALMOST_FULL	
		N1_R1_C_ALMOST_FULL	
		N2_R1_C_ALMOST_FULL	
		N3_R1_C_ALMOST_FULL	
		N4_R1_C_ALMOST_FULL	
		N5_R1_C_ALMOST_FULL	
		N6_R1_C_ALMOST_FULL	
		N7_R1_C_ALMOST_FULL	
		D0_R3_CH_ALMOST_FULL	
		D1_R3_CH_ALMOST_FULL	
		D0_R1_C_OVER_RUN	Section 3.9.12.3.131
		D0_R2_C_OVER_RUN	
		D1_R1_C_OVER_RUN	
		D1_R2_C_OVER_RUN	
		N0_R1_C_OVER_RUN	
		N1_R1_C_OVER_RUN	
		N2_R1_C_OVER_RUN	
		N3_R1_C_OVER_RUN	
		N4_R1_C_OVER_RUN	
		N5_R1_C_OVER_RUN	
		N6_R1_C_OVER_RUN	
		N7_R1_C_OVER_RUN	
		D0_R3_CH_OVER_RUN	
		D1_R3_CH_OVER_RUN	
		D0_R1_C_UNDER_RUN	Section 3.9.12.3.136
		D0_R2_C_UNDER_RUN	
		D1_R1_C_UNDER_RUN	
		D1_R2_C_UNDER_RUN	
		N0_R1_C_UNDER_RUN	
		N1_R1_C_UNDER_RUN	
		N2_R1_C_UNDER_RUN	

		N3_R1_C_UNDER_RUN	
		N4_R1_C_UNDER_RUN	
		N5_R1_C_UNDER_RUN	
		N6_R1_C_UNDER_RUN	
		N7_R1_C_UNDER_RUN	
		D0_R3_CH_UNDER_RUN	
		D1_R3_CH_UNDER_RUN	

Table SCU (Sensor Control Unit)-99 Parameters of I2C Resources

Sub-resource	Item	Parameter	Descriptions
I2C	I2C_REG	-----	Refer to the I2C (3.7) Chapter for information including the Parameters.

Table SCU (Sensor Control Unit)-100 Parameters of SPI Resources

Sub-resource	Item	Parameter	Descriptions
SPI	SPI_REG	-----	Refer to the SPI (3.10) Chapter for information including the Parameters.

3.9.9.7 Sequencer Priority

The sequencers are executed in the following priority.

SEQ0 (highest) > SEQ1 > SEQ2 > SEQ3 > SEQ4 > SEQ5 > SEQ6 > SEQ7 > SEQ8 > SEQ9 (lowest)

The data capture sequence with higher sampling frequencies must be assigned to sequencers with higher priority. This is because sequencers with higher sampling frequencies require higher precision for time stamps.

Since an execution flag check is performed for each sequencer number after a task is executed, sequencers with lower priority may be executed earlier depending on the execution order of the task.

Also, when a sequence with higher priority interrupts during periodic execution of a low priority sequencer, the lower priority sequencer is executed in the next main loop, causing a shift in the time stamp.

Also, multiple sequencers are not executed in the main loop at one time, since priority must be given in a uniform way to other processes such as the ADC.

3.9.9.8 Data Flow

There are 10 channels of sequencers built into the SCU. Each sequencer can be assigned to I2C/SPI transfers. The following shows the data flow of the sequencers.

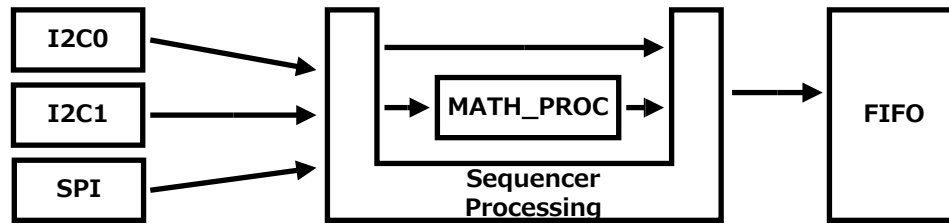


Figure SCU (Sensor Control Unit)-78 Sequencer Data Flow

Within the main loop, when a task of the I2C is called up for example, the I2C task will be executed as long as the sequencer number assigned to the I2C task is active.

3.9.9.9 MATH_PROC Processing

The SCU internal sequencer writes data to the MATH_PROC when there is a request from the MATH_PROC. Then, when the data is output from the MATH_PROC, the processing takes place in accordance with the internal setting.

The presence of a request is judged by reading out the MATH_PROC_EXE register within the SCU_MATH_PROC_REG by the internal sequencer.

The requests from the MATH_PROC occur under the following conditions. These are all controlled from the settings of the CPU.

- SEQ0 or SEQ1 (decimation filter is used)
When any of the following conditions are “true”
 - (1) Any of the OFST_GAIN_EN* in the OFST_GAIN_EN{0x5070} of the MATHID within the SCU_REG is set to “1”
 - (2) Any from among MATHF_EN0, MAYHF_EN1, and MATHF_EN2 in the MATHFUNC_SEL{0x508c} of the MATHID within the SCU_REG is set
 - (3) Any from among N1, N2, and N3 in the DECIMATION_PARAM0/1{0x5084/0x5088} of the MATHID within the SCU_REG is set to 9 or lower
- SEQ2 to SEQ9 (Normal partition)
When one of the two conditions is “true”
 - (1) Any of the OFST_GAIN_EN* in the OFST_GAIN_EN{0x5070} of the MATHID within the SCU_REG is set to “1”
 - (2) Any from among MATHF_EN0, MAYHF_EN1, and MATHF_EN2 in the MATHFUNC_SEL{0x508c} of the MATHID setting within the SCU_REG is set

When FIFO writing happens because of the event, the internal sequencer writes to the FIFO with the highest priority.

3.9.9.10 Data Duplication Function

By writing the COPY_ID as the copy destination and the COPY_ENALBE to the SCU_FIFO_COPY_INFO_n (n is sequencer number, 0 to 9) within SCU_RAM, the data is duplicated to the specified Write FIFO.

The atomicity of the 3 axis data does not corrupt even when the duplication destination FIFO is dynamically switched during operation of the corresponding sequencer. (part of X, Y, Z is not lost at the duplication destination)

3.9.9.11 Interrupt Notification

The internal sequencers notify the CPU of interrupts. For details, refer to Table SCU (Sensor Control Unit)-100.

3.9.9.12 SCU-CPU Synchronous Communication

With some exceptions, the firmware parameters of the SCU internal sequencer and the SCU hardware parameters can only be re-written when their corresponding functions are not operating. (Refer to Section 3.9.12 for information on which registers can be written or not during operation of functions.) For the parameters within the SCU_RAM, refer to Section 3.9.12.11.

For the CPU to recognize whether the operation of a sequencer has completely finished or whether the operation has been suspended during intermittent operations of data capture from sensors, etc., the completion or suspension of the operation must be notified to the CPU. The SCU-CPU Synchronous Communication System notifies this by use of an interrupt.

The following defines the meanings of “suspension” and “completion” of the operation.

- “Operation Completed” refers to cases when either the operation of a sequencer or ADC completes, and the next operation does not start until a startup request is received from the CPU (Figure SCU (Sensor Control Unit)-79).

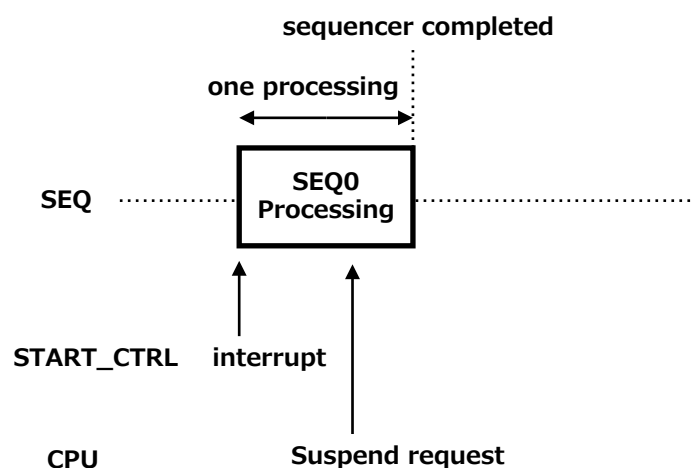


Figure SCU (Sensor Control Unit)-79 Sequencer Completed

- “Operation suspended” refers to cases when one sequencer completes the processing of one main loop and waits for the next startup request (Figure SCU (Sensor Control Unit)-80).

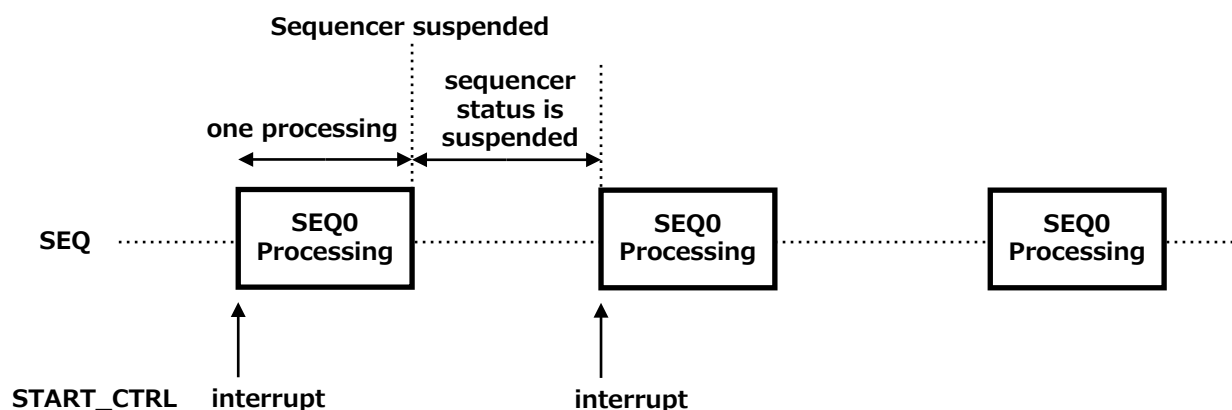


Figure SCU (Sensor Control Unit)-80 Sequencer Suspended

3.9.9.12.1 Completion Judgement

The following events notify the CPU of the completion of operations.

- The ADC has been completed
- One of the SEQ0 to SEQ9 has been completed

The CPU requests the completion of operations to each sequencer.

Multiple complete requests are not issued simultaneously, therefore, each judgement of sequencers SEQ0 to SEQ9 is not needed. Judgement conditions to the complete request can be set as “judging whether (OR judgement) one of the sequencers or ADC processing has been completed”.

In completion judgement, there is no need to judge whether the main loop was operating before. (state

transition does not have to be checked). The judgement is “true” if the corresponding sequencer or ADC has been completed in accordance with the CPU request.

3.9.9.12.2 Suspension Judgement

The following event notifies the suspension of operations.

- SEQ0 to 9 has completed one main loop’s worth of processing and the operation has suspended.

This function is for changing settings (mainly the Decimator’s dynamic connection) from the CPU during the suspension state of the MATH_PROC (when the data that was input to the MATH_PROC is output, and the internal sequencer is transferred to the FIFO). The following describes an example of changing setting of MATH_PROC by using this suspension judgement.

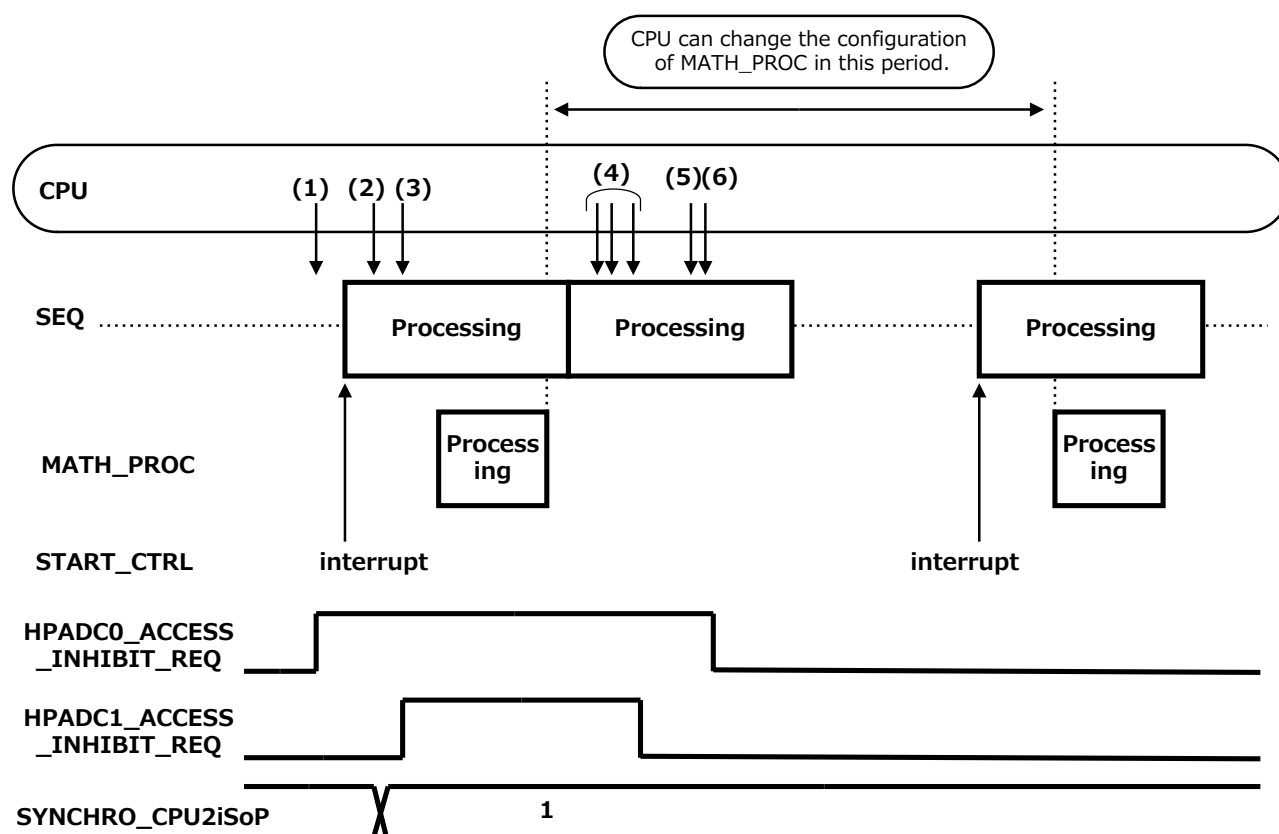


Figure SCU (Sensor Control Unit)-81 MATH_PROC Parameter Change (Example)

In the above Figure, the CPU performs the following controls.

- (1) Sets HPADC0_ACCESS_INHIBIT_REQ to “1” (release and inhibition of SCU SLEEP).
- (2) Completes the sequencer within the SCU_RAM and sets the suspend request sequencer number (SYNCHRO_CPU2iSoP, refer to Section 3.9.12.11.14.)
- (3) Sets the HPADC1_ACCESS_INHIBIT_REQ to “1” (suspend interrupt request), clears the interrupt factor,

disables the IRQ3 interrupt mask, and waits for an interrupt.

(4) Clears the interrupt factor, sets the IRQ3 interrupt mask, and sets HPADC1_ACCESS_INHIBIT_REQ to “0”.

(5) Checks that the error flag (SCU_RAM internal parameter SYNCHRO_iSoP2CPU (refer to Section 3.9.12.11)) is not “1”.

(If the value is “1”, there is an error. Performs readout twice, and after checking, clears to “0”.)

(6) Sets HPADC0_ACCESS_INHIBIT_REQ to “0” (SLEEP enable)

The setting changes of MATH_PROC can be made when the MATH_PROC calculation finishes after controlling the above (1) to (3).

The suspension judgement is performed separately for each sequencer. (If it is decided that OR judgment can be done at the loop-end in the same way as suspension judgment, for example, when the process of a sequencer other than the sequencer of suspension judgement takes time, the suspend notification to the CPU shortens, meaning there is less time for the CPU to make setting changes.)

Also, suspend interrupt cannot be used in the ADC.

3.9.9.12.3 Interrupt Requests and Notification

By setting the SYNCHRO_CPU2iSoP parameter on the SCU_RAM, the sequencers which issue sequencer complete/suspend request interrupts can be selected. The interrupt requests are controlled from the SEQ_ACCESS_INHIBIT_REQ register (refer to Section 3.9.12.3.4) within the SCU_REG.

However, regarding the LPADC_ACCESS_INHIBIT_REQ, the conventional INHIBIT request function (related operations do not function during INHIBIT requests) of the LPADC has been removed from the register. When you need to use the LPADC not being under the CPU’s control, set LPADC0_ENABLE of the ADC_PROPERTY parameter within the SCU_RAM to “0”. In the same way, the conventional INHIBIT request function has been removed from the HPADC0_ACCESS_INHIBIT_REQ and

HPADC1_ACCESS_INHIBIT_REQ registers. When you need to use the HPADC0 not being under the CPU’s control, set HPADC0_ENABLE of the ADC_PROPERTY parameter within the SCU_RAM to “0” since the ADC readout from the firmware controlling the sequencer must be suspended.

When you need to use the HPADC1 not being under the CPU’s control, set HPADC1_ENABLE to “0”.

For the control items of HPADC0_ACCESS_INHIBIT_REQ, refer to Section 3.9.9.13.

The firmware of the SCU internal sequencer performs an interrupt notification to the CPU when the corresponding completion or suspension judgement turns to “true”. It uses an iSoP3 interrupt. (Refer to Section 3.9.6 for details on interrupt numbers from the internal sequencers.)

For the procedure on interrupt notification requests, refer to SYNCHRO_CPU2iSoP (Section 3.9.12.11.14).

3.9.9.12.4 Error Notification

Error detection is performed when a suspend interrupt request is issued, and an error flag is set to the parameter (SYNCHRO_iSoP2CPU (refer to Section 3.9.12.11)) within the SCU_RAM when an error occurs.

The conditions for error detection are as follows:

- (1) A suspend interrupt request is not cancelled
- (2) The MATH_PROC of the sequencer corresponding to the suspend interrupt request has started

When an error is detected, there are cases when the sampled data is not written to the FIFO.

The sequencer complete interrupt requests and suspend interrupt requests from the CPU are performed for each source, and the next request is performed after confirming the interrupt from the SCU.

The setting of the MATH_PROC cannot be re-written until the MATH_PROC is executed with the given settings at least once.

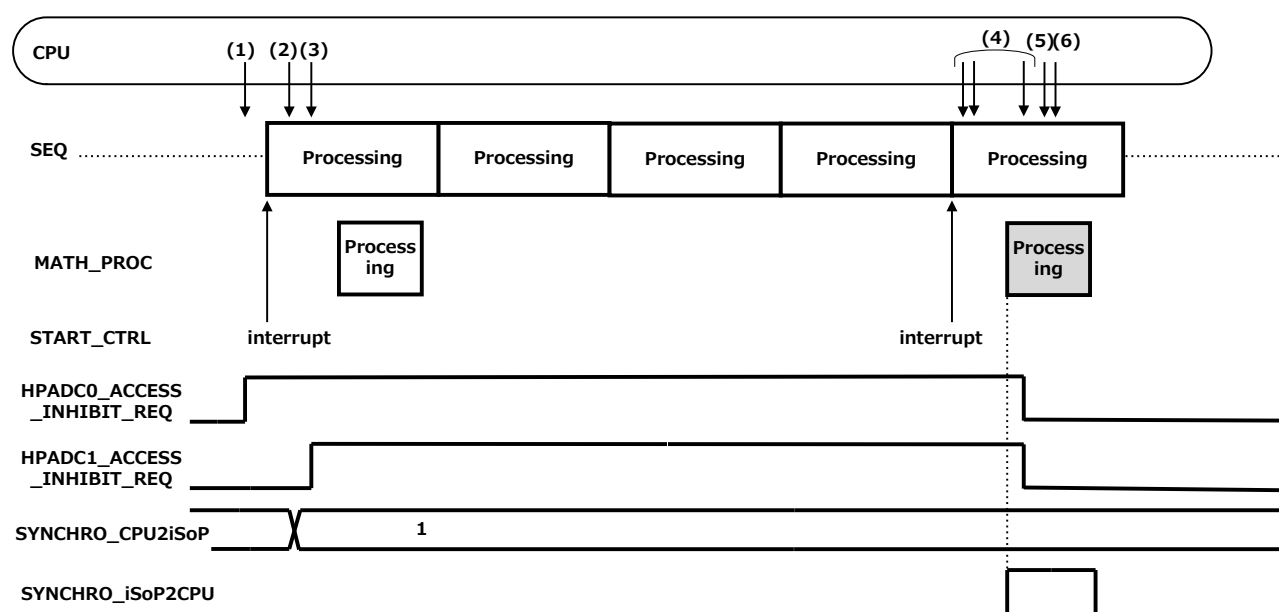


Figure SCU (Sensor Control Unit)-82 Error Notification (Example)

The controls of (1) to (6) in the above Figure are the same as Figure SCU (Sensor Control Unit)-81. During the control of (4), the MATH_PROC started, causing the SYNCHRO_iSoP2CPU to be set to “1”. Note that the transition of the SYNCHRO_iSoP2CPU from “1” to “0” must be controlled by the CPU. When the sequencer detects an error, it sets the SYNCHRO_iSoP2CPU to “1”, but does not set it back to “0”.

3.9.9.13 SLEEP

When the internal sequencer has nothing to process, it automatically enters SLEEP. Sequencers in SLEEP will

WAKEUP when the sequencer conditions are met. It is also possible to inhibit sequencers from entering SLEEP. The following shows the conditions of SLEEP, WAKEUP, and SLEEP inhibition.

SLEEP Conditions

The internal sequencer enters SLEEP when it satisfies all conditions below.

- (1) A sequencer execution request has not been received
- (2) The FIFO of the ADC in operation is "NOT_EMPTY" (Readout entirely)
- (3) A suspend interrupt or complete interrupt request is not in progress

WAKEUP Conditions

The internal sequencer Wakes up when it satisfies the condition below.

- (1) An interrupt raised from the VIC

When you need to Wake up a sequencer from the outside of the SCU, set the HPADC0_ACCESS_INHIBIT_REQ (refer to Section 3.9.12.3.4) register to "1". Note that the sequencer will not automatically enter SLEEP unless you set the HPADC0_ACCESS_INHIBIT_REQ register back to "0".

SLEEP Inhibition

SLEEP can be inhibited by setting the HPADC0_ACCESS_INHIBIT_REQ register within the SCU_REG to "1".

3.9.9.14 Manual Mode

The SCU assumes the reduction of CPU load using the sequencers, but you can also choose not to use sequencers. In such case, the CPU will set all (accessible) control registers as appropriate to realize each function (Manual Mode).

When controlling the SCU in Manual Mode, do not change the reset (XRST_SCU_ISOP) setting of the internal sequencer setting from "1'b0".

For the FIFO within the SCU, use the virtual sensor partition.

3.9.10 DMA

The DMA handshake signal is synchronized at the DMA_SEL block within the SCU.

There are 26 sets of signal lines, each which comprises two lines of output from the SCU and one line of input to the SCU.

The destination DMAC is placed outside the SCU, to which all 26 sets of signals are connected.

Figure SCU (Sensor Control Unit)-83 shows the connection of the DMA handshake signals.

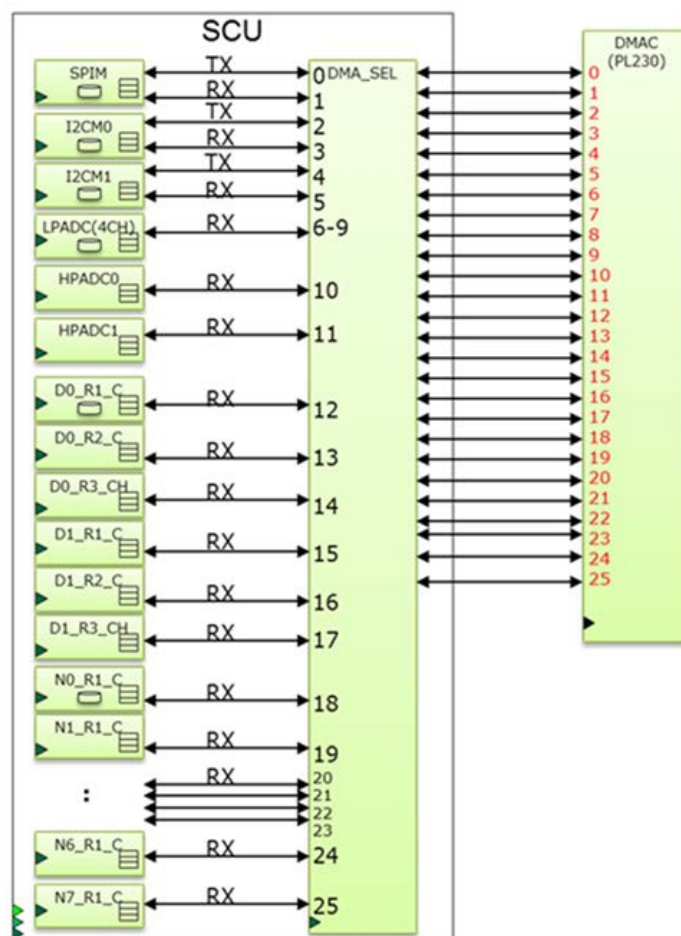


Figure SCU (Sensor Control Unit)-83 DMA Handshake Signal Connections

Table SCU (Sensor Control Unit)-109 shows the relation between the DMA request factors within the SCU and the 26 sets of handshake signals.

Table SCU (Sensor Control Unit)-101 DMA Handshake Signals and Connection Destination DMAC ch IDs

DMA Request Factor	Connection Destination DMAC ch ID	DMA Request Factor	Connection Destination DMAC ch ID
SPI (M) Tx	ch0	FIFO Rx (D0_R1_C)	ch12
SPI (M) Rx	ch1	FIFO Rx (D0_R2_C)	ch13
I2C0 (M) Tx	ch2	FIFO Rx (D0_R3_CH)	ch14
I2C0 (M) Rx	ch3	FIFO Rx (D1_R1_C)	ch15
I2C1 (M) Tx	ch4	FIFO Rx (D1_R2_C)	ch16
I2C1 (M) Rx	ch5	FIFO Rx (D1_R3_CH)	ch17
LPADC (Ch.0)	ch6	FIFO Rx (N0_R1_C)	ch18

LPADC (Ch.1)	ch7	FIFO Rx (N1_R1_C)	ch19
LPADC (Ch.2)	ch8	FIFO Rx (N2_R1_C)	ch20
LPADC (Ch.3)	ch9	FIFO Rx (N3_R1_C)	ch21
HPADC (Ch.0)	ch10	FIFO Rx (N4_R1_C)	ch22
HPADC (Ch.1)	ch11	FIFO Rx (N5_R1_C)	ch23
		FIFO Rx (N6_R1_C)	ch24
		FIFO Rx (N7_R1_C)	ch25

3.9.11 PWM

3.9.11.1 PWM Overview

The PWM repeats the output of High/Low at the specified cycle and the specified duty. There are eight channels of the PWM, each which has the following functions.

- Operating Frequency, Number of Channels
 - Operates (when prescaler is 1/1) by the SCU clock (max. 13 MHz), total of eight channels equipped
 - Up to four external output terminals (selected from internal PWM 8ch or combined for output)
 - Each channel equips a prescaler (1/1 to 1/256)
 - The PWM has a 15 bit resolution (1/32768 to 32767/32768), the cycle and output H width are freely selectable within this range
- Function for synchronization with ADC
 - The PWM can be output using the data fix signal of any ADC channel as a reference
 - ADC data can be captured after a specified duration from the rising edge of the PWM output
- Synchronization function between PWM channels
 - The PWM output can be synchronized between arbitrary PWM channels (including phase adjustment)
- Combining function of external output signals
 - Multiple channels can be arbitrarily selected and combined by OR or AND for each output terminal (total of 4)
- Timer function
 - Can be used as a general-purpose timer when not used as a PWM, allowing readout of count values
 - Can output interrupts to both the SCU internal sequencer and upper CPUs
 - Interrupt is reflected in "INT_ENABLE_ERR_0"

3.9.11.2 PWM Control

The basic settings for the PWM channels n ($n = 0, \dots, 7$) are made using the following registers. Also refer to information after Section 3.9.12.3.154.

-
• PWMn_PARAM register	PWMn_CYCLE field	... sets the cycle
• PWMn_PARAM register	PWMn_THRESH field	... sets the duty (L width)
• PWMn_EN register	PWMn_EN field	... selects the permission of operation
• PWMn_EN register	PWM_SELLn field[2:0]	... selects the ADC channel used as the reference
• PWMn_EN register	PWM_SELLn field[5:3]	... selects the PWM used as the reference
• PWMn_UPDATE register	PWMn_UPDATE field	... reflects the setting update*
• PWM_PASEn register	PWM_DELAYn field	... selects the number of clocks for phase adjustment
• PWM_PASExx register	PWM_CNTENn field[15:8]	... sets the capture start position (from 3 to 255)
• PWM_PASExx register	PWM_CNTENn field[7:4]	... sets the number of captures (from 1 to 15)
• PWM_PASEn register	PWM_CNTENn field[3:0]	... sets the frequency division of the prescaler
• PWM_FUCN2 register	PWM_SEL_DISm field	... selects the PWM channels used for combining
• PWM_FUNCSEL0 register	PWM_SEL_INVm field	... selects whether or not to invert the PWM polarity
• PWM_FUNC4 register	PWM_SELm field	... “0” selects AND combining/“1” selects OR combining

Note: The PWMn_UPDATE must be written in any of the following cases.

- When the PWM_CYCLE value is changed
- To synchronize with other PWMs
- To synchronize with the ADC

The following table shows the maximum and minimum setting range of the output for representative clock settings.

Table SCU (Sensor Control Unit)-102 PWM Maximum and Minimum Setting Range

SCU Frequency (representative example)	Prescaler Setting	Output Variable Range (Setting Example)		
		Maximum Frequency (Duty 50%)	Longest Cycle	Pulse Width Accuracy
13 MHz	1/1	6.5 MHz (154 ns)	396.7 Hz (2.521 ms)	76.9 ns/step
	1/128	50.7 kHz (19692 ns)	3.099 Hz (322.6 ms)	9846 ns/step
8.192 MHz	1/1	4.096 MHz (244 ns)	250 Hz (4 ms)	122 ns/step
	1/128	32 kHz (31250 ns)	1.953 Hz (512 ms)	15625 ns/step
32.768 kHz	1/1	16.384 kHz (61 μs)	1 Hz (1 s)	30.5 μs/step
	1/128	128 Hz (7812.5 μs)	0.0078 Hz (128 s)	3906.25 μs/step

3.9.11.2.1 PWM Cycle Calculation Formula

$PWM\ cycle = UPWM\_CYCLE / (SCU\_CLK \gg PWM\_CNTENn)$

When prescaler is set to 1/1 ($PWM\_CNTENn == 0$)

$UPWM\_CYCLE = PWMn\_CYCLE + 1$

Restriction: $PWMn\_CYCLE > 0$

When prescaler is set to 1/2 or higher ($PWM\_CNTENn \geq 1$)

$UPWM\_CYCLE = PWMn\_CYCLE$

Restriction: $PWMn\_CYCLE > 1$

3.9.11.2.2 PWM Output Duty (High time/cycle) Calculation Formula

$DUTY = 1 - (UPWM\_THRESH / (UPWM\_CYCLE))$

When prescaler is set to 1/1 ($PWM\_CNTENn == 0$)

$UPWM\_CYCLE = PWMn\_CYCLE + 1$

$UPWM\_THRESH = PWMn\_THRESH$

Restriction: $PWMn\_CYCLE > 0, PWMn\_CYCLE \geq PWMn\_THRESH$

When prescaler is set to 1/2 or higher ($PWM\_CNTENn \geq 1$)

$UPWM\_CYCLE = PWMn\_CYCLE \ll PWM\_CNTENn$

$UPWM\_THRESH = (PWMn\_THRESH \ll PWM\_CNTENn) - 1$

Restriction: $PWMn\_CYCLE > 1, PWMn\_THRESH > 1, PWMn\_CYCLE \geq PWMn\_THRESH$

3.9.11.2.3 Special Settings (Fixed Output)

- Setting to make PWM Output fixed status (control by each PWM)
fixed to High Level

$PWMn\_CYCLE$ "1" or higher

Set PWMn_THRESH to “0” and select ENABLE + UPDATE

fixed to Low Level

Set ENABLE to “0”

- Setting to make PMW Output fixed status (control at PWM combining point)

Paste to H

Set PWM_SEL_INVn to “0x1” and PWM_SEL_DISn to “0x1”

Paste to L

Set PWM_SEL_INVn to “0x0” and PWM_SEL_DISn to “0x1”

3.9.11.3 Function for Synchronization with ADC (PWM to ADC)

This mode performs output of the PWM using the valid signal for the ADC output (synchronization signal) from the ADC (LPADC/HPADC) as a reference. The following is an overview.

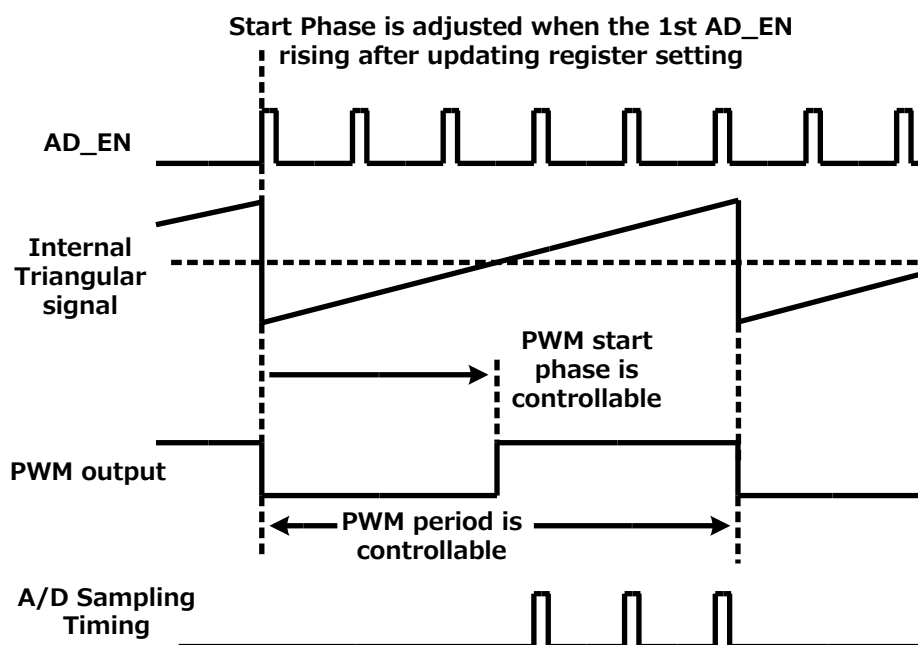


Figure SCU (Sensor Control Unit)-84 PWM Output Mode using ADC Timing as a Reference

When setting the PWM channel n ($n = 0, \dots, 7$), set the following registers in addition to the basic operation settings.

- PWMn_EN register
PWM_SELLn field[2:0] ... selects the ADC channel used as the reference
PWM_SELLn field[5:3] ... fixed to “0”
- PWM_PASEn register
PWM_DELAYn field ... selects the number of clocks for phase adjustment

Enable control of this synchronization function is controlled by the PWMn_EN field of the PWMn_EN register and synchronization operation starts by using the Writing to the PWMn_UPDATE register as a trigger. The following is an example of the settings.

[1]PWM start setting (first time)

PWM0_PARAM = 0x00070007

PWM_PASE0 = 0x00000001

PWM0_EN = 0x0000000x (selection of ADC synchronization source | 0x1[EN])

PWM0_UPDATE = 0x00000001

[2]ADC sampling start

Executes ADC sampling of the SensorDriver

[3]PWM suspend setting

PWM0_EN = 0x00000000

PWM0_UPDATE = 0x00000001

[4]ADC sampling suspension

Suspends by HPADC0_A1 LV_ADC0_EN /HPADC1_A1 LV_ADC1_EN/ LPADC_A0 LV_ADC_EN

Note: The data strobe signal connected to the PWM cannot be controlled by the HPADC0_D2.DECIFIFO_EN/ HPADC1_D2.DECI FIFO_EN/ LPADC_D2 FIFO_EN.

The ADC channels used as the reference can be selected as follows.

Table SCU (Sensor Control Unit)-103 Reference ADC Channel Selection

PWM_SELLn[2:0]	AD Selection
0	Does not synchronize with ADC (free run mode)
1	Synchronizes with HPADC0
2	Synchronizes with HPADC1
3	Reserved
4, 5, 6, and 7	Synchronizes with LPADC0, LPADC1, LPADC2 and LPADC3

3.9.11.3.1 Phase Difference Calculation Formula

When prescaler is set to 1/1

Phase difference (number of SCU_CLOCK) = PWM_DELAYn + 1

When prescaler is set to 1/2 or higher

Phase difference (number of SCU_CLOCK) = PWM_DELAYn x (2^PWM_CNTENn) - α

Range which α may take

The maximum shift width of the Phase difference shift is determined by the prescaler setting value.

α minimum value = 0

α maximum value = $(2^{\text{PWM\_CNTENn}}) - 1$

(1/2 --> 1[clk], 1/4 --> 3[clk], ..., 1/256 --> 255[clk])

Note: This shift occurs randomly and cannot be controlled.

3.9.11.3.2 ADC-PWM Synchronization Settings Procedure (when you do not want to suspend ADC)

[1]ADC Sampling Start

ADC_EN ON

[2]PWM Start Settings (for 2nd time on) PWM0_PARAM = 0x00070007

PWM_PASE0 = 0x00000001 (must be 1 or larger)

PWM0_EN = 0x0000000x (Selection of ADC synchronization source | 0x1[EN])

PWM0_UPDATE = 0x00000001

[3]PWM suspend settings

PWM0_EN = 0x00000000

PWM0_UPDATE = 0x00000001

[4]ADC Sampling Start (same as [2])

ADC_EN ON

[5]PWM Start Settings (from 2nd time on)

PWM_PASE0 = 0x0000ffff

PWM0_PARAM = 0x00070007

PWM0_EN = 0x0000000x (Selection of ADC synchronization source | 0x1[EN])

PWM0_UPDATE = 0x00000001

PWM_PASE0 = 0x00000001

3.9.11.4 Function for Synchronization with ADC (ADC to PWM)

Using the rising edge of the PWM output as a reference timing, this mode controls the timing that the ADC data is captured within the SCU.

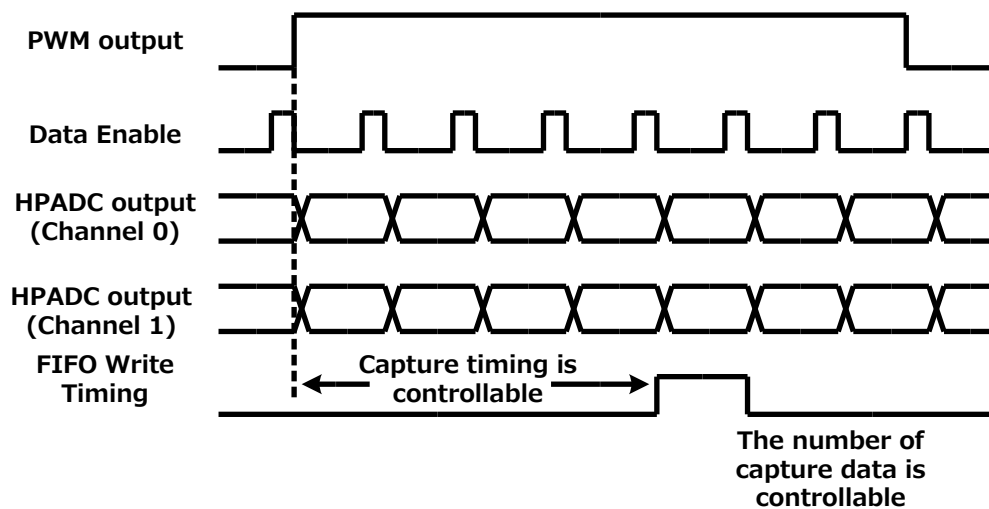


Figure SCU (Sensor Control Unit)-85 ADC Data Capture Mode using the PWM Output Timing as a Reference

When setting the PWM channel n ($n = 0, \dots, 7$), set the following registers in addition to the basic operation settings.

- PWM_PASExx register
PWM_CNTENn field[15:8] ... sets the capture start position (3 to 255)
- PWM_PASExx register
PWM_CNTENn field[7:4]... sets the number of captures (1 to 15)
 - PWMn_EN register
PWM_SELLn field [2:0] ... selects the ADC channel used as the reference
PWM_SELLn field [5:3]...fixed to "0"

Enable control of this synchronization function is controlled by the PWMn_EN field of the PWMn_EN register and synchronization operation starts by using the Writing to the PWMn_UPDATE register as a trigger. The following is an example of the basic settings.

[1]Setting of the PWM to which data capture timing of the ADC is synchronized

HPADC0_D1 DECI_RATIO2 /HPADC1_D1 DECI_RATIO2/LPADC_D0

DECI_RATIO2/LPADC_D1 DECI_RATIO2/LPADC_D2 DECI_RATIO2/LPADC_D3 DECI_RATIO2

[2] Setting the number of data captured by the ADC

PWM_PASExx PWM_CNTENn [15:8] and [7:4] must not be "0"

[3]The Synchronization ADC is set

PWMn_EN PWM_SELLn Synchronization ADC channel setting

[4]The PWM starts

PWMxx_EN/PWMcxx_UPDATE is executed

The selection of which channel's signal of the PWM to assign to each ADC channel is set by the registers on

the ADC side.

Table SCU (Sensor Control Unit)-104 ADC Channels and PWM Assignment

Register Name	Field Name	Target ADC
LPADC_D1[20:12]	DECI_RATIO2	LPADC0
LPADC_D4[20:12]	DECI_RATIO2	LPADC1
LPADC_D5[20:12]	DECI_RATIO2	LPADC2
LPADC_D6[20:12]	DECI_RATIO2	LPADC3
HPADC_D0_D1[20:12]	DECI_RATIO2	HPADC0
HPADC_D1_D1[20:12]	DECI_RATIO2	HPADC1

The synchronization function becomes valid when bit 8 of each register's DECI_RATIO2 is set to "1". The PWM channel of each synchronization target is selected by bit0 to 7, and by setting each one to "1", the synchronization signals PWM0 to 7 become valid.

3.9.11.5 Synchronization Function between PWM Channels

This mode synchronizes the timing between any PWM channels. It is also possible to operate multiple PWMs in a chain sequence. When setting the PWM channel n ($n = 0, \dots, 7$), set the following registers in addition to the basic operation settings.

- PWMn_EN register
 PWM_SELLn field [5:3] ... sets channel (m) of the PWM you want to synchronize
 - PWM_PASEn register
 PWM_DELAYn field ... selects the number of clocks for phase adjustment

After making the settings, perform the additional setting on the PWM channel m which you want to synchronize. That is to say, write "1" on the PWMm_UPDATE field of the PWMm_EN register. By this additional setting, the PWM channel n synchronizes with the PWM channel m . The following is an example setting of synchronizing channel 0 with channel 1.

<Example of Procedures>

[1] Ch0 set

```
PWM0_PARAM  = 0x00070007
PWM_PASE0   = 0x00000001
PWM0_EN     = 0x00000011
PWM0_UPDATE = 0x00000001
```

[2] Ch1 set

```
PWM1_PARAM  = 0x00040007
PWM_PASE1   = 0x00000000
PWM1_EN     = 0x00000001
PWM1_UPDATE = 0x00000001 (Ch1 & Ch0 output start)
```

[3] Ch0 suspend

PWM0_EN = 0x00000010

PWM0_UPDATE = 0x00000001

[4] Ch1 suspend

PWM1_EN = 0x00000000

PWM1_UPDATE = 0x00000001

[5] Ch0 suspend and then process

PWM_PASE0[15:0] = 0xffff

[6] PWM another setting (if you want)

The settings for the PWM you want to synchronize can be selected as follows:

Table SCU (Sensor Control Unit)-105 Settings for Synchronization between PWMs

PWM_SE LLn[5:3]	PWM0	PWM1	PWM2	PWM3	PWM4	PWM5	PWM6	PWM7
0	No Synchroni zation	No Synchroni zation	No Synchroni zation	No Synchroni zation	No Synchroni zation	No Synchroni zation	No Synchroni zation	No Synchroni zation
1	PWM1	PWM0	PWM0	PWM0	PWM0	PWM0	PWM0	PWM0
2	PWM2	PWM2	PWM1	PWM1	PWM1	PWM1	PWM1	PWM1
3	PWM3	PWM3	PWM3	PWM2	PWM2	PWM2	PWM2	PWM2
4	PWM4	PWM4	PWM4	PWM4	PWM3	PWM3	PWM3	PWM3
5	PWM5	PWM5	PWM5	PWM5	PWM5	PWM4	PWM4	PWM4
6	PWM6	PWM6	PWM6	PWM6	PWM6	PWM6	PWM5	PWM5
7	PWM7	PWM7	PWM7	PWM7	PWM7	PWM7	PWM7	PWM6

3.9.11.5.1 PWM Output Phase Calculation Formula

When prescaler is set to 1/1

Phase difference (number of SCU_CLOCK) = PWM_DELAY_n + 1

When prescaler is set to 1/2 or higher

Phase difference (number of SCU_CLOCK) = PWM_DELAY_n × (2^{PWM_CNTEN_n}) - α

Range which α may take

The maximum shift width of the Phase difference shift α is determined by the prescaler setting.

α minimum value = 0

α maximum value = (2^{PWM_CNTEN_n}) - 1

For the prescaler 1/2 setting, this is 1[clk]. For the prescaler 1/4 setting, it is 3[clk], and then, at the 1/256 setting, it is 255[clk].

Note: This shift occurs randomly and cannot be controlled.

3.9.11.5.2 PWM Output Synchronization Initialization Procedures

Note 1: Do not set PWM_PASEn[15:0] to “0xffff” nor “0x0000”.

Note 2: “0xffff” is a setting for clear, and actual phase setting is not permitted.

[1]PWM suspend setting

PWM0_EN = 0x00000000

PWM0_UPDATE = 0x00000001

[2]Phase Setting

PWM_PASEn[15:0] = 0xffff

[3]PWM another setting (if you want)

3.9.11.6 External Output Signal Combining Function

By combining the internal PWM signal, the waveform output from the external PWM terminal can be combined. AND or OR can be used for the combining.

Setting example:

Terminal PWM0ch = PWM0 & PWM1 & PWM2 & PWM3 & PWM4 & PWM5 & PWM6 & PWM7

Terminal PWM1ch = PWM0 | PWM1 | PWM2 | PWM3 | PWM4 | PWM5 | PWM6 | PWM7

When setting the output terminal PWMm (m = 0, ..., 3), set the following registers in addition to the basic operation settings.

- PWM_FUCN2 register
PWM_SEL_DISm field ... selects the PWM channel used for the combining
- PWM_FUNCSEL0 register
PWM_SEL_INVm field ... selects whether or not to invert the PWM polarity
- PWM_FUNC4 register
PWM_SELm field ... “0” selects AND combining/“1” selects OR combining

The setting of the PWM channel used for combining can be selected as follows:

Table SCU (Sensor Control Unit)-106 Setting of PWM Channels to be Combined

PWM_SEL_DISm[7:0] PWM_SEL_INVm[7:0]	PWM0 Terminal	PWM1 Terminal	PWM2 Terminal	PWM3 Terminal
bit 0	PWM0	PWM1	PWM2	PWM3
bit 1	PWM1	PWM0	PWM0	PWM0
bit 2	PWM2	PWM2	PWM1	PWM1
bit 3	PWM3	PWM3	PWM3	PWM2
bit 4	PWM4	PWM4	PWM4	PWM4
bit 5	PWM5	PWM5	PWM5	PWM5
bit 6	PWM6	PWM6	PWM6	PWM6
bit 7	PWM7	PWM7	PWM7	PWM7

Regarding the PWM_SEL_DISm, when bit0 is “0”, the corresponding PWM becomes valid, when “1”, the corresponding PWM becomes invalid.

Regarding bit 1 to bit 7, when they are “1”, the corresponding PWM becomes valid, when “0”, the corresponding PWM becomes invalid. In either case, the PWM channels that were made invalid are treated as “1” output.

Regarding the PWM_SEL_INVm, the PWM channels corresponding to each bit are inverted by “1”.

When performing OR combining by the PWM_SELm field setting, disable the channels that are not used by PWM_SEL_DISm and then also make an invert setting for PWM_SEL_INVm (input “0” at the OR combining stage).

Note that at the reset initial state, these registers are All 0 and the output terminal PWMm (m = 0, ..., 3) is in a state that the internal PWMm can be output without being combined and inverted.

3.9.11.7 PWM_TIMER

Channels that are not used as the PWM function can be used as general-purpose timers. The settings are the same as PWM.

Also, interrupts can be generated at the timing of each falling edge of the PWM output (PWM cycle).

Note that for the internal sequencer, a total of three signals are generated by ORing arbitrarily selected eight channels and provided as interrupt signals.

For the upper CPU, each of eight channels of PMW timer interrupt is output via the INT_SEL module. Please also refer to Section 3.9.6.2.

3.9.12 SCU Register Details

3.9.12.1 Address Offset

The following shows 32 bit address offset from the CPU. Add the following address to the offsets in the table to calculate the address from the CPU.

Offset: 0x00190000 (Mirror: 0x04190000)

3.9.12.2 SCU_REG Internal Memory List

Table SCU (Sensor Control Unit)-107 SCU Internal Memory

Offset (Transaction Port)	Address	Name	Size (bits)	Description
0x0000 .. 0x3FFC		SEQ_IRAM	32	Inst Ram Array Internal Sequencer Instruction Ram Array
0x4000 .. 0x4FFC		SEQ_DRAM(SCU_RAM)	32	Internal Sequencer Data Ram Array

3.9.12.3 SCU_REG Register List

Note: Some offset addresses are listed irregularly. Be careful when you set address by calculating with the SW. The Reserved regions are secured in the 0x50AC to 0x50AF, and 0x50C0 to 0x50CF offset addresses shown in the following list.

Table SCU (Sensor Control Unit)-108 SCU Register List

Offset Address (Transaction Port)	Name	Type	Size (bit)	Description	Reset Value
0x5018	I2C0	RO	32	Monitors SCL/SDA/internal status of the IP for I2C0	0x00000000
0x501C	I2C1	RO	32	Monitors SCL/SDA/internal status of the IP for I2C1	0x00000000
0x5020	SEQ_ENABLE_ALL	RW	32	Permission/prohibition setting for operations of whole sequencers can be collectively controlled 0: operation is prohibited 1: operation is permitted	0x00000000

				When the bit is “0”, the operation of all sequencers is suspended. When the bit is “1”, the operation of each sequencer is performed according to the permission of each sequencer.	
0x5024	SEQ_ACCESS_INHIBIT	RW	32		0x00000000
0x5028	START_CTRL_COMMON	RW	32		0x0000FF00
0x502C	START_MODE0	RW	32		0x00000000
0x5030	START_MODE1	RW	32	0: Operation suspended 1: A certain cycle startup by the timer 2: One startup after the external interrupt occurrence 3: A certain cycle startup by the timer after the external interrupt occurrence	0x00000000
0x5034	START_INTERVAL3_0	RW	32		0x00000000
0x5038	START_INTERVAL7_4	RW	32		0x00000000
0x503C	START_INTERVAL9_8	RW	32		0x00000000
0x5040	START_PHASE1_0	RW	32		0x00000000
0x5044	START_PHASE3_2	RW	32		0x00000000
0x5048	START_PHASE5_4	RW	32		0x00000000
0x504C	START_PHASE7_6	RW	32		0x00000000
0x5050	START_PHASE9_8	RW	32		0x00000000
0x5054	SINGLE_EXE	RW	32		0x00000000
0x5058	START_CTRL_STT0	RO	32		0x00000000
0x505C	START_CTRL_STT1	RO	32		0x00000000
0x5060	DEBUG_CTRL	RW	32		0x00000000
0x5070	OFST_GAIN_EN	RW	32		0x00000000
0x5074	UNSIGNED_TO_SIGNED	RW	32		0x00000000
0x5078	DEC_CLR	WO	32		0x00000000
0x507C	MATHFUNC_CLR	WO	32		0x00000000
0x5080	EVENT_STT	WO	32		0x00000000
0x5084	DECIMATION_PARAM0	RW	32		0x00000000
0x5088	DECIMATION_PARAM1	RW	32		0x00000000
0x508C	MATHFUNC_SEL	RW	32	0: D0_W0_S 1: D0_W1_S 2: D0_W2_S 3: D0_W3_S 4: D1_W0_S	0x00000000

				5: D1_W1_S 6: D1_W2_S 7: D1_W3_S 8: N0_W_S 9: N1_W_S 10: N2_W_S 11: N3_W_S 12: N4_W_S 13: N5_W_S 14: N6_W_S 15: N7_W_S	
0x5090	MATHFUNC_POS0	RW	32		0x00000000
0x5094	MATHFUNC_POS1	RW	32		0x00000000
0x5098	MATHFUNC_POS2	RW	32		0x00000000
0x50A0	MATHFUNC_PARAM_0_0	RW	32		0x00000000
0x50A4	MATHFUNC_PARAM_C0_0_0_MSB	RW	32		0x00000000
0x50A8	MATHFUNC_PARAM_C0_0_0_LSB	RW	32		0x00000000
0x50AC to 0x50AF	Reserved			Reserved	
0x50B0	MATHFUNC_PARAM_C1_0_0_MSB	RW	32		0x00000000
0x50B4	MATHFUNC_PARAM_C1_0_0_LSB	RW	32		0x00000000
0x50B8	MATHFUNC_PARAM_C2_0_0_MSB	RW	32		0x00000000
0x50BC	MATHFUNC_PARAM_C2_0_0_LSB	RW	32		0x00000000
0x50C0 to 0x50CF	Reserved			Reserved	
0x50D0	MATHFUNC_PARAM_C3_0_0_MSB	RW	32		0x00000000
0x50D4	MATHFUNC_PARAM_C3_0_0_LSB	RW	32		0x00000000
0x50D8	MATHFUNC_PARAM_C4_0_0_MSB	RW	32		0x00000000
0x50DC	MATHFUNC_PARAM_C4_0_0_LSB	RW	32		0x00000000

	0_LSB				
0x50E0	MATHFUNC_PARAM_0_1	RW	32		0x00000000
0x50E4	MATHFUNC_PARAM_C0_0_1_MSB	RW	32		0x00000000
0x50E8	MATHFUNC_PARAM_C0_0_1_LSB	RW	32		0x00000000
0x50EC	MATHFUNC_PARAM_C1_0_1_MSB	RW	32		0x00000000
0x50F0	MATHFUNC_PARAM_C1_0_1_LSB	RW	32		0x00000000
0x50F4	MATHFUNC_PARAM_C2_0_1_MSB	RW	32		0x00000000
0x50F8	MATHFUNC_PARAM_C2_0_1_LSB	RW	32		0x00000000
0x50FC	MATHFUNC_PARAM_C3_0_1_MSB	RW	32		0x00000000
0x5100	MATHFUNC_PARAM_C3_0_1_LSB	RW	32		0x00000000
0x5104	MATHFUNC_PARAM_C4_0_1_MSB	RW	32		0x00000000
0x5108	MATHFUNC_PARAM_C4_0_1_LSB	RW	32		0x00000000
0x510C	MATHFUNC_PARAM_1_0	RW	32		0x00000000
0x5110	MATHFUNC_PARAM_C0_1_0_MSB	RW	32		0x00000000
0x5114	MATHFUNC_PARAM_C0_1_0_LSB	RW	32		0x00000000
0x5118	MATHFUNC_PARAM_C1_1_0_MSB	RW	32		0x00000000
0x511C	MATHFUNC_PARAM_C1_1_0_LSB	RW	32		0x00000000
0x5120	MATHFUNC_PARAM_C2_1_0_MSB	RW	32		0x00000000
0x5124	MATHFUNC_PARAM_C2_1_0_LSB	RW	32		0x00000000
0x5128	MATHFUNC_PARAM_C3_1_0_MSB	RW	32		0x00000000
0x512C	MATHFUNC_PARAM_C3_1_0_LSB	RW	32		0x00000000

	0_LSB				
0x5130	MATHFUNC_PARAM_C4_1_0_MSB	RW	32		0x00000000
0x5134	MATHFUNC_PARAM_C4_1_0_LSB	RW	32		0x00000000
0x5138	MATHFUNC_PARAM_1_1	RW	32		0x00000000
0x513C	MATHFUNC_PARAM_C0_1_1_MSB	RW	32		0x00000000
0x5140	MATHFUNC_PARAM_C0_1_1_LSB	RW	32		0x00000000
0x5144	MATHFUNC_PARAM_C1_1_1_MSB	RW	32		0x00000000
0x5148	MATHFUNC_PARAM_C1_1_1_LSB	RW	32		0x00000000
0x514C	MATHFUNC_PARAM_C2_1_1_MSB	RW	32		0x00000000
0x5150	MATHFUNC_PARAM_C2_1_1_LSB	RW	32		0x00000000
0x5154	MATHFUNC_PARAM_C3_1_1_MSB	RW	32		0x00000000
0x5158	MATHFUNC_PARAM_C3_1_1_LSB	RW	32		0x00000000
0x515C	MATHFUNC_PARAM_C4_1_1_MSB	RW	32		0x00000000
0x5160	MATHFUNC_PARAM_C4_1_1_LSB	RW	32		0x00000000
0x5164	MATHFUNC_PARAM_2_0	RW	32		0x00000000
0x5168	MATHFUNC_PARAM_C0_2_0_MSB	RW	32		0x00000000
0x516C	MATHFUNC_PARAM_C0_2_0_LSB	RW	32		0x00000000
0x5170	MATHFUNC_PARAM_C1_2_0_MSB	RW	32		0x00000000
0x5174	MATHFUNC_PARAM_C1_2_0_LSB	RW	32		0x00000000
0x5178	MATHFUNC_PARAM_C2_2_0_MSB	RW	32		0x00000000
0x517C	MATHFUNC_PARAM_C2_2_0_LSB	RW	32		0x00000000

	0_LSB				
0x5180	MATHFUNC_PARAM_C3_2_0_MSB	RW	32		0x00000000
0x5184	MATHFUNC_PARAM_C3_2_0_LSB	RW	32		0x00000000
0x5188	MATHFUNC_PARAM_C4_2_0_MSB	RW	32		0x00000000
0x518C	MATHFUNC_PARAM_C4_2_0_LSB	RW	32		0x00000000
0x5190	MATHFUNC_PARAM_2_1	RW	32		0x00000000
0x5194	MATHFUNC_PARAM_C0_2_1_MSB	RW	32		0x00000000
0x5198	MATHFUNC_PARAM_C0_2_1_LSB	RW	32		0x00000000
0x519C	MATHFUNC_PARAM_C1_2_1_MSB	RW	32		0x00000000
0x51A0	MATHFUNC_PARAM_C1_2_1_LSB	RW	32		0x00000000
0x51A4	MATHFUNC_PARAM_C2_2_1_MSB	RW	32		0x00000000
0x51A8	MATHFUNC_PARAM_C2_2_1_LSB	RW	32		0x00000000
0x51AC	MATHFUNC_PARAM_C3_2_1_MSB	RW	32		0x00000000
0x51B0	MATHFUNC_PARAM_C3_2_1_LSB	RW	32		0x00000000
0x51B4	MATHFUNC_PARAM_C4_2_1_MSB	RW	32		0x00000000
0x51B8	MATHFUNC_PARAM_C4_2_1_LSB	RW	32		0x00000000
0x51BC	EVENT_PARAM0_THRESH	RW	32		0x00000000
0x51C0	EVENT_PARAM0_COUNT0	RW	32		0x00000000
0x51C4	EVENT_PARAM0_COUNT1	RW	32		0x00000000
0x51C8	EVENT_PARAM0_COUNT2	RW	32		0x00000000
0x51CC	EVENT_PARAM1_THRESH	RW	32		0x00000000
0x51D0	EVENT_PARAM1_COUNT0	RW	32		0x00000000
0x51D4	EVENT_PARAM1_COUNT1	RW	32		0x00000000
0x51D8	EVENT_PARAM1_COUNT2	RW	32		0x00000000

0x51DC	EVENT_PARAM2_THRESH	RW	32		0x00000000
0x51E0	EVENT_PARAM2_COUNT0	RW	32		0x00000000
0x51E4	EVENT_PARAM2_COUNT1	RW	32		0x00000000
0x51E8	EVENT_PARAM2_COUNT2	RW	32		0x00000000
0x51EC	EVENT_PARAM0_DELAY_S AMPLE	RW	32		0x00000000
0x51F0	EVENT_PARAM1_DELAY_S AMPLE	RW	32		0x00000000
0x51F4	EVENT_PARAM2_DELAY_S AMPLE	RW	32		0x00000000
0x5200	EVENT_TIMESTAMP0_R_M SB	RO	32		0x00000000
0x5204	EVENT_TIMESTAMP0_R_LS B	RO	32		0x00000000
0x5208	EVENT_TIMESTAMP1_R_M SB	RO	32		0x00000000
0x520C	EVENT_TIMESTAMP1_R_LS B	RO	32		0x00000000
0x5210	EVENT_TIMESTAMP2_R_M SB	RO	32		0x00000000
0x5214	EVENT_TIMESTAMP2_R_LS B	RO	32		0x00000000
0x5218	EVENT_TIMESTAMP0_F_M SB	RO	32		0x00000000
0x521C	EVENT_TIMESTAMP0_F_LS B	RO	32		0x00000000
0x5220	EVENT_TIMESTAMP1_F_M SB	RO	32		0x00000000
0x5224	EVENT_TIMESTAMP1_F_LS B	RO	32		0x00000000
0x5228	EVENT_TIMESTAMP2_F_M SB	RO	32		0x00000000
0x522C	EVENT_TIMESTAMP2_F_LS B	RO	32		0x00000000
0x5230	FIFO_WRITE_CTRL	RW	32		0x00000000
0x5300	Reserved			Reserved	
0x5400	INT_ENABLE_MAIN	RW	32		0x00000000
0x5404	INT_DISABLE_MAIN	RW	32		0x00000000

0x5408	INT_CLEAR_MAIN	WO	32		0x00000000
0x540C	LEVEL_SEL_MAIN	RW	32		0x00000000
0x5410	INT_RAW_STT_MAIN	RO	32		0x00000000
0x5414	INT_MASKED_STT_MAIN	RO	32		0x00000000
0x5420	INT_ENABLE_ERR_0	RW	32		0x00000000
0x5424	INT_DISABLE_ERR_0	RW	32		0x00000000
0x5428	INT_CLEAR_ERR_0	WO	32		0x00000000
0x542C	INT_RAW_STT_ERR_0	RO	32		0x00000000
0x5430	INT_MASKED_STT_ERR_0	RO	32		0x00000000
0x5440	INT_ENABLE_ERR_1	RW	32		0x00000000
0x5444	INT_DISABLE_ERR_1	RW	32		0x00000000
0x5448	INT_CLEAR_ERR_1	WO	32		0x00000000
0x544C	INT_RAW_STT_ERR_1	RO	32		0x00000000
0x5450	INT_MASKED_STT_ERR_1	RO	32		0x00000000
0x5460	INT_ENABLE_ERR_2	RW	32		0x00000000
0x5464	INT_DISABLE_ERR_2	RW	32		0x00000000
0x5468	INT_CLEAR_ERR_2	WO	32		0x00000000
0x546C	INT_RAW_STT_ERR_2	RO	32		0x00000000
0x5470	INT_MASKED_STT_ERR_2	RO	32		0x00000000
0x5500	RAM_TEST	RW	32		0x00000000
0x5510	SCU_POWER	RO	32	Clock status controlled by the SCU internal sequencer 0: CK_SCU 1: CK_SCU_SPI 2: CK_SCU_I2C0 3: CK_SCU_I2C1	0x00000000
0x5520	INT_ENABLE_MAIN_AD	RW	32		0x00000000
0x5524	INT_DISABLE_MAIN_AD	RW	32		0x00000000
0x5528	INT_CLEAR_MAIN_AD	WO	32		0x00000000
0x552C	LEVEL_SEL_MAIN_AD	RW	32		0x00000000
0x5530	INT_RAW_STT_MAIN_AD	RO	32		0x00000000
0x5534	INT_MASKED_STT_MAIN_AD	RO	32		0x00000000
0x5600	PWM0_PARAM	RW	32	PWM0 Pulse period/width setting	0x00000000
0x5604	PWM0_EN	RW	32		0x00000000
0x5608	PWM0_UPDATE	RW	32		0x00000000
0x560C	PWM1_PARAM	RW	32	PWM1	0x00000000

				Pulse period/width setting	
0x5610	PWM1_EN	RW	32		0x00000000
0x5614	PWM1_UPDATE	RW	32		0x00000000
0x5618	PWM2_PARAM	RW	32		0x00000000
0x561C	PWM2_EN	RW	32		0x00000000
0x5620	PWM2_UPDATE	RW	32		0x00000000
0x5624	PWM3_PARAM	RW	32		0x00000000
0x5628	PWM3_EN	RW	32		0x00000000
0x562C	PWM3_UPDATE	RW	32		0x00000000
0x5630	PWM_PASE0	RW	32		0x00000000
0x5634	PWM_PASE1	RW	32		0x00000000
0x5638	PWM_PASE2	RW	32		0x00000000
0x563C	PWM_PASE3	RW	32		0x00000000
0x5640	PWM4_PARM	RW	32		0x00000000
0x5644	PWM4_EN	RW	32		0x00000000
0x5648	PWM4_UPDATE	RW	32		0x00000000
0x564C	PWM5_PARAM	RW	32		0x00000000
0x5650	PWM5_EN	RW	32		0x00000000
0x5654	PWM5_UPDATE	RW	32		0x00000000
0x5658	PWM6_PARAM	RW	32		0x00000000
0x565C	PWM6_EN	RW	32		0x00000000
0x5660	PWM6_UPDATE	RW	32		0x00000000
0x5664	PWM7_PARAM	RW	32		0x00000000
0x5668	PWM7_EN	RW	32		0x00000000
0x566C	PWM7_UPDATE	RW	32		0x00000000
0x5670	PWM_PASE4	RW	32		0x00000000
0x5674	PWM_PASE5	RW	32		0x00000000
0x5678	PWM_PASE6	RW	32		0x00000000
0x567C	PWM_PASE7	RW	32		0x00000000
0x5680	PWM_TIMER01	RO	32		0x00000000
0x5684	PWM_TIMER23	RO	32		0x00000000
0x5688	PWM_TIMER45	RO	32		0x00000000
0x568C	PWM_TIMER67	RO	32		0x00000000
0x5690	PWM_FUNCSEL0	RW	32		0x00000000
0x5694	PWM_FUNC1	RW	32		0x00000000
0x5698	PWM_FUCN2	RW	32		0x00000000
0x569C	PWM_FUNC3	RW	32		0x00000000
0x56A0	PWM_FUNC4	RW	32		0x00000000

0x56A4	POWER_EN	RW	32		0x0000FFFF

3.9.12.3.1 {0x5018} I2C0 Details

Table SCU (Sensor Control Unit)-109

Local Address: 0x5018																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														FSM				Reserved				SDA		SCL							
Bits		Name				Type	Reset Value				Description																				
31..13		Reserved				RO	0x00000				Reserved																				
12..8		FSM				RO	0x00				The internal status of the IP for I2C0 can be monitored.																				
7..2		Reserved				RO	0x00				Reserved																				
1		SDA				RO	0x0				Input status of the signal in the SDA of the IP for I2C0 can be monitored.																				
0		SCL				RO	0x0				Input status of the signal in the SCL of the IP for I2C0 can be monitored.																				

3.9.12.3.2 {0x501C} I2C1 Details

Table SCU (Sensor Control Unit)-110

Local Address: 0x501C																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														FSM				Reserved				SDA		SCL							
Bits		Name			Type	Reset Value			Description																						
31..13		Reserved			RO	0x00000			Reserved																						
12..8		FSM			RO	0x00			The internal status of the IP for I2C1 can be monitored.																						
7..2		Reserved			RO	0x00			Reserved																						
1		SDA			RO	0x0			Input status of the signal in the SDA of the IP for I2C1 can be monitored.																						
0		SCL			RO	0x0			Input status of the signal in the SCL of the IP for I2C1can be monitored.																						

3.9.12.3.3 {0x5020} SEQ_ENABLE_ALL Details

Permission/prohibition setting for operations of whole sequencers can be collectively controlled

0: operation is prohibited

1: operation is permitted

When the bit is “0”, the operation of all sequencers is suspended.

When the bit is “1”, the operation of each sequencer is performed according to the permission of each sequence.

Table SCU (Sensor Control Unit)-111

Local Address: 0x5020																						Register Type: RW (read/write)															
																						Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																														ENABLE_READY	ENABLE_ALL_SEQ						
Bits		Name						Type	Reset Value						Description																						
31..2		Reserved						RO	0x00000000						Reserved																						
1		ENABLE_READY						RO	0x0						Indicates that the sequence operation is ready. Write “1” on ENABLE_ALL_SEQ after the bit becomes “1”.																						
0		ENABLE_ALL_SEQ						RW	0x0						Permission/prohibition setting for operations of whole sequencers can be collectively controlled																						

3.9.12.3.4 {0x5024} SEQ_ACCESS_INHIBIT Details

Table SCU (Sensor Control Unit)-112

Local Address: 0x5024																Register Type: RW (read/write) Reset Value: 0x00000000																																																																																																																																																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																																																																																																																																															
Reserved																LPADC_ACCESS_INHIBIT_ACK3								LPADC_ACCESS_INHIBIT_ACK2								LPADC_ACCESS_INHIBIT_ACK1								LPADC_ACCESS_INHIBIT_REQ3								LPADC_ACCESS_INHIBIT_REQ2								LPADC_ACCESS_INHIBIT_REQ1								HPADC1_ACCESS_INHIBIT_ACK								HPADC0_ACCESS_INHIBIT_ACK								LPADC_ACCESS_INHIBIT_ACK								I2C1_ACCESS_INHIBIT_ACK								I2C0_ACCESS_INHIBIT_ACK								SPI_ACCESS_INHIBIT_ACK								Reserved								HPADC1_ACCESS_INHIBIT_REQ								HPADC0_ACCESS_INHIBIT_REQ								LPADC_ACCESS_INHIBIT_REQ								I2C1_ACCESS_INHIBIT_REQ								I2C0_ACCESS_INHIBIT_REQ								SPI_ACCESS_INHIBIT_REQ							
																Bits	Name							Type	Reset Value	Description																																																																																																																																													
																31..20								Reserved							RO	0x000							Reserved																																																																																																																																
																19								LPADC_ACCESS_I NHIBIT_ACK3							RO	0x0							-																																																																																																																																
																18								LPADC_ACCESS_I NHIBIT_ACK2							RO	0x0							-																																																																																																																																
																17								LPADC_ACCESS_I NHIBIT_ACK1							RO	0x0							-																																																																																																																																
																16								LPADC_ACCESS_I NHIBIT_REQ3							RW	0x0																																																																																																																																							
																15								LPADC_ACCESS_I NHIBIT_REQ2							RW	0x0																																																																																																																																							
																14								LPADC_ACCESS_I NHIBIT_REQ1							RW	0x0							-																																																																																																																																
																13								HPADC1_ACCESS_ INHIBIT_ACK							RO	0x0							-																																																																																																																																
																12								HPADC0_ACCESS_ INHIBIT_ACK							RO	0x0							-																																																																																																																																
																11								LPADC_ACCESS_I NHIBIT_ACK							RO	0x0							-																																																																																																																																

10	I2C1_ACCESS_INHIBIT_ACK	RO	0x0	After "I2C1_ACCESS_INHIBIT_REQ==1" is detected, if you stop the I2C1 slave access, the sequencer sets "1" on this bit. You must read or write on the register for I2C1 slave after the bit becomes "1".
9	I2C0_ACCESS_INHIBIT_ACK	RO	0x0	After "I2C0_ACCESS_INHIBIT_REQ==1" is detected, if you stop the I2C0 slave access, the sequencer sets "1" on this bit. You must read or write on the register for I2C0 slave after the bit becomes "1".
8	SPI_ACCESS_INHIBIT_ACK	RO	0x0	After "SPI_ACCESS_INHIBIT_REQ==1" is detected, if you stop the SPI slave access, the sequencer sets "1" on this bit. You must read or write on the register for the SPI slave after the bit becomes "1".
7..6	Reserved	RO	0x0	Reserved
5	HPADC1_ACCESS_INHIBIT_REQ	RW	0x0	When the sequencer is requested to be suspended Suspend interrupt is requested and canceled to the internal sequencer. "1" is set when the sequencer is requested to be suspended. "0" is set in the interrupt context. Refer to Section 3.9.9.12.3
4	HPADC0_ACCESS_INHIBIT_REQ	RW	0x0	When the sequencer is requested to be completed or suspended Release and inhibition of the SLEEP for the internal sequencer is performed. "1" is set when the sequencer is requested to be completed/suspended. "0" is set after the request is done. Refer to Section 3.9.9.13.
3	LPADC_ACCESS_INHIBIT_REQ	RW	0x0	When the sequencer is requested to be completed Complete interrupt is requested and canceled to the internal sequencer. "1" is set when the sequencer is requested to be completed. "0" is set in the interrupt context. Refer to Section 3.9.9.12.3.

2	I2C1_ACCESS_INHIBIT_REQ	RW	0x0	When the CPU directly accesses I2C1, “1” is set on this bit. SEQ_CTRL holds the access to I2C1 while the bit is “1”. Note that if this bit is set “1” for longer time than the sequencer’s access cycle using I2C1 from SEQ_CTRL, the bit of EXE_ERR_STT will become “1”.
1	I2C0_ACCESS_INHIBIT_REQ	RW	0x0	When the CPU directly accesses I2C0, “1” is set on this bit. SEQ_CTRL holds the access to I2C0 while the bit is “1”. Note that if this bit is set “1” for longer time than the sequencer’s access cycle using I2C0 from SEQ_CTRL, the bit of EXE_ERR_STT will become “1”.
0	SPI_ACCESS_INHIBIT_REQ	RW	0x0	When the CPU directly accesses SPI, “1” is set on this bit. SEQ_CTRL holds the access to SPI while the bit is “1”. Note that if this bit is set “1” for longer time than the sequencer’s access cycle using SPI from SEQ_CTRL, the bit of EXE_ERR_STT will become “1”.

3.9.12.3.5 {0x5028} START_CTRL_COMMON Details

Table SCU (Sensor Control Unit)-113

Local Address: 0x5028																Register Type: RW (read/write)																					
																Reset Value: 0x0000FF00																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																PRE_DIVIDER								Reserved								EXT_INT_POL					
Bits	Name							Type	Reset Value	Description																											
31..16	Reserved							RO	0x0000	Reserved																											
15..8	PRE_DIVIDER							RW	0xFF	Maximum frequency setting for starting data capturing common to all sequencers 32.768 kHz/(PRE_DIVIDER+1) is the maximum frequency for data capturing common to all sequencers. For example, if you have a sensor which must sample at maximum 1 kHz, the frequency is 32.768/ (31 + 1) = 1024, and the value of PRE_DIVIDER is 31. For the sensor’s maximum sampling ability, refer to the Chapter of ADC (3.21).																											
7..1	Reserved							RO	0x00	Reserved																											
0	EXT_INT_POL							RW	0x0	Polarity setting for the external interrupt input signal 0: rising edge of the interrupt signal 1: falling edge of the interrupt signal																											

3.9.12.3.6 {0x502C} START_MODE0 Details

Table SCU (Sensor Control Unit)-114

Local Address: 0x502C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																START_ENABLE9	START_ENABLE8	START_ENABLE7	START_ENABLE6	START_ENABLE5	START_ENABLE4	START_ENABLE3	START_ENABLE2	START_ENABLE1	START_ENABLE0						
Bits	Name				Type	Reset Value	Description																								
31..10	Reserved				RO	0x000000	Reserved																								
9	START_ENABLE9				RW	0x0	This designates permission/prohibition of the Sequencer 9's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.																								
8	START_ENABLE8				RW	0x0	This designates permission/prohibition of the Sequencer 8's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.																								
7	START_ENABLE7				RW	0x0	This designates permission/prohibition of the Sequencer 7's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.																								
6	START_ENABLE6				RW	0x0	This designates permission/prohibition of the Sequencer 6's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.																								
5	START_ENABLE5				RW	0x0	This designates permission/prohibition of the Sequencer 5's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.																								

4	START_ENABLE4	RW	0x0	This designates permission/prohibition of the Sequencer 4's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.
3	START_ENABLE3	RW	0x0	This designates permission/prohibition of the Sequencer 3's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.
2	START_ENABLE2	RW	0x0	This designates permission/prohibition of the Sequencer 2's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.
1	START_ENABLE1	RW	0x0	This designates permission/prohibition of the Sequencer 1's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.
0	START_ENABLE0	RW	0x0	This designates permission/prohibition of the Sequencer 0's operation. Even if the operation is permitted, when ENABLE_ALL is prohibited, the operation will not start.

3.9.12.3.7 {0x5030} START_MODE1 Details

Table SCU (Sensor Control Unit)-115

Local Address: 0x5030																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								START_MODE9	START_MODE8	START_MODE7	START_MODE6	START_MODE5	START_MODE4	START_MODE3	START_MODE2	START_MODE1	START_MODE0														
Bits	Name		Type	Reset Value	Description																										
31..20	Reserved		RO	0x000	Reserved																										
19..18	START_MODE9		RW	0x0	This designates the Sequencer 9’s starting mode. 0: Operation suspended 1: A certain cycle startup by the timer 2: One startup after the external interrupt occurrence 3: after the external interrupt occurrence																										
17..16	START_MODE8		RW	0x0	This designates the Sequencer 8’s starting mode. For the control specifications, refer to START_MODE9.																										
15..14	START_MODE7		RW	0x0	This designates the Sequencer 7’s starting mode. For the control specifications, refer to START_MODE9.																										
13..12	START_MODE6		RW	0x0	This designates the Sequencer 6’s starting mode. For the control specifications, refer to START_MODE9.																										
11..10	START_MODE5		RW	0x0	This designates the Sequencer 5’s starting mode. For the control specifications, refer to START_MODE9.																										
9..8	START_MODE4		RW	0x0	This designates the Sequencer 4’s starting mode. For the control specifications, refer to START_MODE9.																										
7..6	START_MODE3		RW	0x0	This designates the Sequencer 3’s starting mode. For the control specifications, refer to START_MODE9.																										
5..4	START_MODE2		RW	0x0	This designates the Sequencer 2’s starting mode. For the control specifications, refer to START_MODE9.																										
3..2	START_MODE1		RW	0x0	This designates the Sequencer 1’s starting mode. For the control specifications, refer to START_MODE9.																										
1..0	START_MODE0		RW	0x0	This designates the Sequencer 0’s starting mode. For the control specifications, refer to START_MODE9.																										

3.9.12.3.8 {0x5034} START_INTERVAL3_0 Details

Table SCU (Sensor Control Unit)-116

Local Address: 0x5034																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved				START_INTERVAL3				Reserved				START_INTERVAL2				Reserved				START_INTERVAL1				Reserved				START_INTERVAL0									
Bits	Name			Type	Reset Value	Description																															
31..28	Reserved			RO	0x0	Reserved																															
27..24	START_INTERVAL3			RW	0x0	This designates Sequencer 3’s timer operating frequency division value. When SEQ_MODE is “0” or “1”, the set value is referred. $32.768 \text{ kHz}/(\text{PRE\_DIVIDER}+1)/(2^{\text{START\_INTERVAL3}})$ is Sequencer 3’s operating frequency division value. The value range that can be set to SEQ_INTERVAL3 is from 0 to 9. When using a One-shot Sequencer corresponding to the register, 0xA must be set.																															
23..20	Reserved			RO	0x0	Reserved																															
19..16	START_INTERVAL2			RW	0x0	This designates Sequencer 2’s timer operating frequency division value. When SEQ_MODE is “0” or “1”, this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	START_INTERVAL1			RW	0x0	This designates Sequencer 1’s timer operating frequency division value. When SEQ_MODE1 is “0” or “1”, this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.																															

7..4	Reserved	RO	0x0	Reserved
3..0	START_INTERVAL0	RW	0x0	This designates Sequencer 0's timer operating frequency division value. When SEQ_MODE0 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.

3.9.12.3.9 {0x5038} START_INTERVAL7_4 Details

Table SCU (Sensor Control Unit)-117

Local Address: 0x5038																Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved				START_INTERVAL7				Reserved				START_INTERVAL6				Reserved				START_INTERVAL5				Reserved				START_INTERVAL4					
Bits	Name			Type	Reset Value	Description																											
31..28	Reserved			RO	0x0	Reserved																											
27..24	START_INTERVAL7			RW	0x0	This designates Sequencer 7's timer operating frequency division value. When SEQ_MODE7 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.																											
23..20	Reserved			RO	0x0	Reserved																											
19..16	START_INTERVAL6			RW	0x0	This designates Sequencer 6's timer operating frequency division value. When SEQ_MODE6 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.																											
15..12	Reserved			RO	0x0	Reserved																											

11..8	START_INTERVAL5	RW	0x0	This designates Sequencer 5's timer operating frequency division value. When SEQ_MODE5 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.
7..4	Reserved	RO	0x0	Reserved
3..0	START_INTERVAL4	RW	0x0	This designates Sequencer 4's timer operating frequency division value. When SEQ_MODE4 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.

3.9.12.3.10 {0x503C} START_INTERVAL9_8 Details

Table SCU (Sensor Control Unit)-118

Local Address: 0x503C																Register Type: RW (read/write) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved																START_INTERVAL9				Reserved				START_INTERVAL8									
Bits	Name			Type	Reset Value	Description																											
31..12	Reserved			RO	0x00000	Reserved																											
11..8	START_INTERVAL9			RW	0x0	This designates Sequencer 9’s timer operating frequency division value. When SEQ_MODE9 is “0” or “1”, this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.																											
7..4	Reserved			RO	0x0	Reserved																											

3..0	START_INTERVAL8	RW	0x0	This designates Sequencer 8's timer operating frequency division value. When SEQ_MODE8 is "0" or "1", this set value is referred. As for the calculating formula of the operating frequency, the range of values that can be set, and set values when using the One-shot Sequencer, refer to START_INTERVAL3.

3.9.12.3.11 {0x5040} START_PHASE1_0 Details

Table SCU (Sensor Control Unit)-119

Local Address: 0x5040																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								START_PHASE1								Reserved								START_PHASE0							
Bits		Name						Type		Reset Value		Description																			
31..25		Reserved						RO		0x00		Reserved																			
24..16		START_PHASE1						RW		0x000		This designates Sequencer 1’s timer startup phase. When SEQ_MODE1 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL1 corresponds to SEQ_PHASE1, a request to start sequencer operation occurs.																			
15..9		Reserved						RO		0x00		Reserved																			
8..0		START_PHASE0						RW		0x000		This designates Sequencer 0’s timer startup phase. When SEQ_MODE0 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL0 corresponds to SEQ_PHASE0, a request to start sequencer operation occurs.																			

3.9.12.3.12 {0x5044} START_PHASE3_2 Details

Table SCU (Sensor Control Unit)-120

Local Address: 0x5044																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								START_PHASE3								Reserved								START_PHASE2							
Bits				Name				Type				Reset Value				Description															
31..25				Reserved				RO				0x00				Reserved															
24..16				START_PHASE3				RW				0x000				This designates Sequencer 3’s timer startup phase. When SEQ_MODE3 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL3 corresponds to SEQ_PHASE3, a request to start sequencer operation occurs.															
15..9				Reserved				RO				0x00				Reserved															
8..0				START_PHASE2				RW				0x000				This designates Sequencer 2’s timer startup phase. When SEQ_MODE2 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL2 corresponds to SEQ_PHASE2, a request to start sequencer operation occurs.															

3.9.12.3.13 {0x5048} START_PHASE5_4 Details

Table SCU (Sensor Control Unit)-121

Local Address: 0x5048																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								START_PHASE5								Reserved								START_PHASE4							
Bits		Name				Type		Reset Value		Description																					
31..25		Reserved				RO		0x00		Reserved																					
24..16		START_PHASE5				RW		0x000		This designates Sequencer 5’s timer startup phase. When SEQ_MODE5 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL5 corresponds to SEQ_PHASE5, a request to start sequencer operation occurs.																					
15..9		Reserved				RO		0x00		Reserved																					
8..0		START_PHASE4				RW		0x000		This designates Sequencer 4’s timer startup phase. When SEQ_MODE4 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL4 corresponds to SEQ_PHASE4, a request to start sequencer operation occurs.																					

3.9.12.3.14 {0x504C} START_PHASE7_6 Details

Table SCU (Sensor Control Unit)-122

Local Address: 0x504C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								START_PHASE7								Reserved								START_PHASE6							
Bits				Name				Type				Reset Value				Description															
31..25				Reserved				RO				0x00				Reserved															
24..16				START_PHASE7				RW				0x000				This designates Sequencer 7's timer startup phase. When SEQ_MODE7 is "0" or "1", this set value is referred. When the value of the internal counter SEQ_INTERVAL7 corresponds to SEQ_PHASE7, a request to start sequencer operation occurs.															
15..9				Reserved				RO				0x00				Reserved															
8..0				START_PHASE6				RW				0x000				This designates Sequencer 6's timer startup phase. When SEQ_MODE1 is "0" or "1", this set value is referred. When the value of the internal counter SEQ_INTERVAL6 corresponds to SEQ_PHASE6, a request to start sequencer operation occurs.															

3.9.12.3.15 {0x5050} START_PHASE9_8 Details

Table SCU (Sensor Control Unit)-123

Local Address: 0x5050																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								START_PHASE9								Reserved								START_PHASE8							
Bits		Name			Type		Reset Value		Description																						
31..25		Reserved			RO		0x00		Reserved																						
24..16		START_PHASE9			RW		0x000		This designates Sequencer 9’s timer startup phase. When SEQ_MODE9 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL9 corresponds to SEQ_PHASE9, a request to start sequencer operation occurs.																						
15..9		Reserved			RO		0x00		Reserved																						
8..0		START_PHASE8			RW		0x000		This designates Sequencer 8’s timer startup phase. When SEQ_MODE8 is “0” or “1”, this set value is referred. When the value of the internal counter SEQ_INTERVAL8 corresponds to SEQ_PHASE8, a request to start sequencer operation occurs.																						

3.9.12.3.16 {0x5054} SINGLE_EXE Details

Table SCU (Sensor Control Unit)-124

Local Address: 0x5054																						Register Type: RW (read/write)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved																						REQ9	REQ8	REQ7	REQ6	REQ5	REQ4	REQ3	REQ2	REQ1	REQ0	
Bits	Name		Type	Reset Value	Description																											
31..10	Reserved		RO	0x000000	Reserved																											
9	REQ9		WO	0x0	By writing “1”, Sequencer 9’s execution request is issued only once. When the corresponding START_ENABLE bit is “0”, this register is not active. When SEQ_MODE9 is “2” or “3”, this set value is referred.																											
8	REQ8		WO	0x0	By writing “1”, Sequencer 8’s execution request is issued only once. When the corresponding START_ENABLE bit is “0”, this register is not active. When SEQ_MODE8 is “2” or “3”, this set value is referred.																											
7	REQ7		WO	0x0	By writing “1”, Sequencer 7’s execution request is issued only once. When the corresponding START_ENABLE bit is “0”, this register is not active. When SEQ_MODE7 is “2” or “3”, this set value is referred.																											
6	REQ6		WO	0x0	By writing “1”, Sequencer 6’s execution request is issued only once. When the corresponding START_ENABLE bit is “0”, this register is not active. When SEQ_MODE6 is “2” or “3”, this set value is referred.																											
5	REQ5		WO	0x0	By writing “1”, Sequencer 5’s execution request is issued only once. When the corresponding START_ENABLE bit is “0”, this register is not active. When SEQ_MODE5 is “2” or “3”, this set value is referred.																											

4	REQ4	WO	0x0	By writing "1", Sequencer 4's execution request is issued only once. When the corresponding START_ENABLE bit is "0", this register is not active. When SEQ_MODE4 is "2" or "3", this set value is referred.
3	REQ3	WO	0x0	By writing "1", Sequencer 3's execution request is issued only once. When the corresponding START_ENABLE bit is "0", this register is not active. When SEQ_MODE3 is "2" or "3", this set value is referred.
2	REQ2	WO	0x0	By writing "1", Sequencer 2's execution request is issued only once. When the corresponding START_ENABLE bit is "0", this register is not active. When SEQ_MODE2 is "2" or "3", this set value is referred.
1	REQ1	WO	0x0	By writing "1", Sequencer 1's execution request is issued only once. When the corresponding START_ENABLE bit is "0", this register is not active. When SEQ_MODE1 is "2" or "3", this set value is referred.
0	REQ0	WO	0x0	By writing "1", Sequencer 0's execution request is issued only once. When the corresponding START_ENABLE bit is "0", this register is not active. When SEQ_MODE0 is "2" or "3", this set value is referred.

3.9.12.3.17 {0x5058} START_CTRL_STT0 Details

Table SCU (Sensor Control Unit)-125

Local Address: 0x5058																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP_MSB																															
Bits		Name		Type	Reset Value		Description																								
31..0		TIME_STAMP_MSB		RO	0x00000000		The time stamp value at the time of being read out can be read out. Note that the value can be changed when reading out the TIME_STAMP_LSB. Therefore, read out TIME_STAMP_MSB and TIME_STAMP_LSB, and do the same again to confirm that the second values are not changed from the first.																								

3.9.12.3.18 {0x505C} START_CTRL_STT1 Details

Table SCU (Sensor Control Unit)-126

Local Address: 0x505C																		Register Type: RO (read only)															
																		Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved								EXE_REQ_STT								Reserved	TIME_STAMP_LSB																
Bits		Name						Type		Reset Value		Description																					
31..26		Reserved						RO		0x00		Reserved																					
25..16		EXE_REQ_STT						RO		0x000		This indicates the request status of the sequencers. 1: request issued or request in processing bit 16: Sequencer 0 bit 17: Sequencer 1 bit 18: Sequencer 2 bit 19: Sequencer 3 bit 20: Sequencer 4 bit 21: Sequencer 5 bit 22: Sequencer 6 bit 23: Sequencer 7 bit 24: Sequencer 8 bit 25: Sequencer 9																					
15		Reserved						RO		0x0		Reserved																					
14..0		TIME_STAMP_LSB						RO		0x0000		The execution request value at the time of being read out can be read out. Note that the value can be changed when reading out the TIME_STAMP_MSB. Therefore, read out TIME_STAMP_MSB and TIME_STAMP_LSB, and do the same again to confirm that the second values are not changed from the first.																					

3.9.12.3.19 {0x5060} DEBUG_CTRL Details

Table SCU (Sensor Control Unit)-127

Local Address: 0x5060																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
EXT_INT_REQ	Reserved				DONE_REQ								Reserved				MONSEL				Reserved				EXT_INT_REQ_DBG_EN	DONE_REQ_DBG_EN					
Bits	Name				Type	Reset Value	Description																								
31	EXT_INT_REQ				WO	0x0	This forces an external interrupt to occur from the CPU.																								
30..26	Reserved				RO	0x00	Reserved																								
25..16	DONE_REQ				WO	0x000	This forces an execution completed to occur from the CPU.																								
15..12	Reserved				RO	0x0	Reserved																								
11..8	MONSEL				RW	0x0	Selecting monitor output signals																								
7..2	Reserved				RO	0x00	Reserved																								
1	EXT_INT_REQ_DBG_EN				RW	0x0	This enables EXE_INT_REQ.																								
0	DONE_REQ_DBG_EN				RW	0x0	This enables DONE_REQ.																								

3.9.12.3.20 {0x5070} OFST_GAIN_EN Details

Table SCU (Sensor Control Unit)-128

Local Address: 0x5070																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved																OFST_GAIN_EN15	OFST_GAIN_EN14	OFST_GAIN_EN13	OFST_GAIN_EN12	OFST_GAIN_EN11	OFST_GAIN_EN10	OFST_GAIN_EN9	OFST_GAIN_EN8	Reserved				OFST_GAIN_EN4	Reserved				OFST_GAIN_EN0				
Bits	Name		Type	Reset Value	Description																																
31..16				Reserved	RO	0x0000				Reserved																											
15				OFST_GAIN_EN15	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 9. If “0” is designated, the value of OFST_GAIN9 is ignored.																											
14				OFST_GAIN_EN14	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 8. If “0” is designated, the value of OFST_GAIN8 is ignored.																											
13				OFST_GAIN_EN13	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 7. If “0” is designated, the value of OFST_GAIN7 is ignored.																											
12				OFST_GAIN_EN12	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 6. If “0” is designated, the value of OFST_GAIN6 is ignored.																											
11				OFST_GAIN_EN11	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 5. If “0” is designated, the value of OFST_GAIN5 is ignored.																											
10				OFST_GAIN_EN10	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 4. If “0” is designated, the value of OFST_GAIN4 is ignored.																											
9				OFST_GAIN_EN9	RW	0x0				Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 3. If “0” is designated, the value of OFST_GAIN3 is ignored.																											

8	OFST_GAIN_EN8	RW	0x0	Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 2. If “0” is designated, the value of OFST_GAIN2 is ignored.
7..5	Reserved	RO	0x0	Reserved
4	OFST_GAIN_EN4	RW	0x0	Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 1. If “0” is designated, the value of OFST_GAIN1 is ignored.
3..1	Reserved	RO	0x0	Reserved
0	OFST_GAIN_EN0	RW	0x0	Designate “1” to perform offset addition processing and gain multiplication processing for MATH_PROC of Sequencer 0. If “0” is designated, the value of OFST_GAIN0 is ignored.

3.9.12.3.21 {0x5074} UNSIGNED_TO_SIGNED Details

Table SCU (Sensor Control Unit)-129

Local Address: 0x5074																Register Type: RW (read/write) Reset Value: 0x00000000																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0															
Reserved																UNSIGNED_TO_SIGNED15	UNSIGNED_TO_SIGNED14	UNSIGNED_TO_SIGNED13	UNSIGNED_TO_SIGNED12	UNSIGNED_TO_SIGNED11	UNSIGNED_TO_SIGNED10	UNSIGNED_TO_SIGNED9	UNSIGNED_TO_SIGNED8	Reserved				UNSIGNED_TO_SIGNED4				Reserved				UNSIGNED_TO_SIGNED0			
Bits				Name				Type		Reset Value		Description																											
31..16				Reserved				RO		0x0000		Reserved																											
15				UNSIGNED_TO_SIGNED15				RW		0x0		When “1” is designated, before performing offset addition processing and gain multiplication processing of Sequencer 9, the input data format must be regarded as offset binary and converted into two’s complement format. The offset binary format’s offset is [(maximum value of input value binary + 1)/2]. When “0” is designated, code conversion is not performed.																											
14				UNSIGNED_TO_SIGNED14				RW		0x0		This controls processing of Sequencer 8. As for specifications, refer to UNSIGNED_TO_SIGNED15.																											
13				UNSIGNED_TO_SIGNED13				RW		0x0		This controls processing of Sequencer 7. As for specifications, refer to UNSIGNED_TO_SIGNED15.																											
12				UNSIGNED_TO_SIGNED12				RW		0x0		This controls processing of Sequencer 6. As for specifications, refer to UNSIGNED_TO_SIGNED15.																											
11				UNSIGNED_TO_SIGNED11				RW		0x0		This controls processing of Sequencer 5. As for specifications, refer to UNSIGNED_TO_SIGNED15.																											
10				UNSIGNED_TO_SIGNED10				RW		0x0		This controls processing of Sequencer 4. As for specifications, refer to UNSIGNED_TO_SIGNED15.																											
9				UNSIGNED_TO_SIGNED9				RW		0x0		This controls processing of Sequencer 3. As for specifications, refer to UNSIGNED_TO_SIGNED15																											

8	UNSIGNED_TO_SIGNED8	RW	0x0	This controls processing of Sequencer 2. As for specifications, refer to UNSIGNED_TO_SIGNED15.
7..5	Reserved	RO	0x0	Reserved
4	UNSIGNED_TO_SIGNED4	RW	0x0	This controls processing of Sequencer 1. As for specifications, refer to UNSIGNED_TO_SIGNED15.
3..1	Reserved	RO	0x0	Reserved
0	UNSIGNED_TO_SIGNED0	RW	0x0	This controls processing of Sequencer 0. As for specifications, refer to UNSIGNED_TO_SIGNED15.

3.9.12.3.22 {0x5078} DEC_CLR Details

Table SCU (Sensor Control Unit)-130

Local Address: 0x5078																Register Type: WO (write only) Reset Value: 0x00000000																																							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
Reserved																								DEC1_N2_CLR				DEC1_N1_CLR				DEC1_N0_CLR				DEC1_COMMON_CLR				DEC0_N2_CLR				DEC0_N1_CLR				DEC0_N0_CLR				DEC0_COMMON_CLR			
Bits	Name							Type	Reset Value							Description																																							
31..8	Reserved							WO	0x000000							Reserved																																							
7	DEC1_N2_CLR							WO	0x0							DEC1 synchronous reset (to FF in the differentiating circuit for N2)																																							
6	DEC1_N1_CLR							WO	0x0							DEC1 synchronous reset (to FF in the differentiating circuit for N1)																																							
5	DEC1_N0_CLR							WO	0x0							DEC1 synchronous reset (to FF in the differentiating circuit for N0)																																							
4	DEC1_COMMON_CLR							WO	0x0							DEC1 synchronous reset																																							
3	DEC0_N2_CLR							WO	0x0							DEC0 synchronous reset (to FF in the differentiating circuit for N2)																																							
2	DEC0_N1_CLR							WO	0x0							DEC0 synchronous reset (to FF in the differentiating circuit for N1)																																							
1	DEC0_N0_CLR							WO	0x0							DEC0 synchronous reset (to FF in the differentiating circuit for N0)																																							
0	DEC0_COMMON_CLR							WO	0x0							DEC0 synchronous reset (to FF in the integrating circuit)																																							

3.9.12.3.23 {0x507C} MATHFUNC_CLR Details

Table SCU (Sensor Control Unit)-131

Local Address: 0x507C																						Register Type: WO (write only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																												MATHFUNC2_CLR	MATHFUNC1_CLR	MATHFUNC0_CLR							
Bits	Name							Type	Reset Value							Description																					
31..3	Reserved							WO	0x00000000							Reserved																					
2	MATHFUNC2_CLR							WO	0x0							MATHFUNC2 synchronous reset																					
1	MATHFUNC1_CLR							WO	0x0							MATHFUNC1 synchronous reset																					
0	MATHFUNC0_CLR							WO	0x0							MATHFUNC0 synchronous reset																					

3.9.12.3.24 {0x5080} EVENT_STT Details

Table SCU (Sensor Control Unit)-132

Local Address: 0x5080																		Register Type: WO (write only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																												CLR							
Bits		Name						Type	Reset Value						Description																				
31..3		Reserved						WO	0x00000000						Reserved																				
2..0		CLR						WO	0x0						Clear of the internal status for the event detection																				

3.9.12.3.25 {0x5084} DECIMATION_PARAM0 Details

Table SCU (Sensor Control Unit)-133

Local Address: 0x5084																Register Type: RW (read/write) Reset Value: 0x00000000																																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																																			
FORCE_THROUGH3				Reserved				LEVEL_ADJ_3				N3				FORCE_THROUGH2				Reserved				LEVEL_ADJ_2				N2				FORCE_THROUGH1				Reserved				LEVEL_ADJ_1				N1				Reserved				LEVEL_ADJ_0				Reserved			
Bits		Name						Type		Reset Value		Description																																															
31		FORCE_THROUGH3						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N3 value.																																															
30		Reserved						RO		0x0		Reserved																																															
29..28		LEVEL_ADJ_3						RW		0x0		Level adjust value setting with clipping for D0_W3_S. 0: once 1: twice 2: four times 3: eight times																																															
27..24		N3						RW		0x0		Decimation ratio for D0_W3_S. 0 to 9: Frequency is divided by 1/(2^n) using n as a designated value. 10 to 15: Decimation is not performed, and data are not output.																																															
23		FORCE_THROUGH2						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N2 value.																																															
22		Reserved						RO		0x0		Reserved																																															
21..20		LEVEL_ADJ_2						RW		0x0		Level adjust value setting with clipping for D0_W2_S. As for specifications, refer to LEVEL_ADJ_3.																																															
19..16		N2						RW		0x0		Decimation ratio for D0_W3_S. As for specifications, refer to N3.																																															
15		FORCE_THROUGH1						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N1 value.																																															
14		Reserved						RO		0x0		Reserved																																															

13..12	LEVEL_ADJ_1	RW	0x0	Level adjust value setting with clipping for D1_W1_S. As for specifications, refer to LEVEL_ADJ_3.
11..8	N1	RW	0x0	Decimation ratio for D0_W1_S. As for specifications, refer to N3.
7..6	Reserved	RO	0x0	Reserved
5..4	LEVEL_ADJ_0	RW	0x0	Level adjust value setting with clipping for D0_W0_S. As for specifications, refer to LEVEL_ADJ_3.
3..0	Reserved	RO	0x0	Reserved

3.9.12.3.26 {0x5088} DECIMATION_PARAM1 Details

Table SCU (Sensor Control Unit)-134

Local Address: 0x5088																Register Type: RW (read/write) Reset Value: 0x00000000																																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																																			
FORCE_THROUGH7				Reserved				LEVEL_ADJ_7				N7				FORCE_THROUGH6				Reserved				LEVEL_ADJ_6				N6				FORCE_THROUGH5				Reserved				LEVEL_ADJ_5				N5				Reserved				LEVEL_ADJ_4				Reserved			
Bits		Name						Type		Reset Value		Description																																															
31		FORCE_THROUGH7						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N7 value.																																															
30		Reserved						RO		0x0		Reserved																																															
29..28		LEVEL_ADJ_7						RW		0x0		Level adjust value setting with clipping for D1_W3_S. 0: once 1: twice 2: four times 3: eight times																																															
27..24		N7						RW		0x0		Decimation ratio for D1_W3_S. 0 to 9: Frequency is divided by 1/(2^n) using n as a designated value. 10 to 15: Decimation is not performed, and data are not output.																																															
23		FORCE_THROUGH6						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N6 value.																																															
22		Reserved						RO		0x0		Reserved																																															
21..20		LEVEL_ADJ_6						RW		0x0		Level adjust value setting with clipping for D1_W2_S. As for specifications, refer to LEVEL_ADJ_7.																																															
19..16		N6						RW		0x0		Decimation ratio for D0_W2_S. As for specifications, refer to N7.																																															
15		FORCE_THROUGH5						RW		0x0		When “1” is set, input data is forced to output directly regardless of the N5 value.																																															

14	Reserved	RO	0x0	Reserved
13..12	LEVEL_ADJ_5	RW	0x0	Level adjust value setting with clipping for D1_W1_S. As for specifications, refer to LEVEL_ADJ_7.
11..8	N5	RW	0x0	Decimation ratio for D1_W1_S. As for specifications, refer to N7.
7..6	Reserved	RO	0x0	Reserved
5..4	LEVEL_ADJ_4	RW	0x0	Level adjust value setting with clipping for D1_W0_S. As for specifications, refer to LEVEL_ADJ_7.
3..0	Reserved	RO	0x0	Reserved

3.9.12.3.27 {0x508C} MATHFUNC_SEL Details

0: D0_W0_S 8: N0_W_S
 1: D0_W1_S 9: N1_W_S
 2: D0_W2_S 10: N2_W_S
 3: D0_W3_S 11: N3_W_S
 4: D1_W0_S 12: N4_W_S
 5: D1_W1_S 13: N5_W_S
 6: D1_W2_S 14: N6_W_S
 7: D1_W3_S 15: N7_W_S

Table SCU (Sensor Control Unit)-135

Local Address: 0x508C																				Register Type: RW (read/write)													
																				Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved								MATHF_EN2	WID2							Reserved	MATHF_EN1	WID1							Reserved	MATHF_EN0	WID0						
Bits		Name						Type	Reset Value							Description																	
31..21		Reserved						RO	0x000							Reserved																	
20		MATHF_EN2						RW	0x0							Operation permission of Math Function 2																	
19..16		WID2						RW	0x0							FIFO Partition ID setting value allocated to Math Function 2: 0 to 15																	
15..13		Reserved						RO	0x0							Reserved																	
12		MATHF_EN1						RW	0x0							Operation permission of Math Function 1																	
11..8		WID1						RW	0x0							FIFO Partition ID setting value allocated to Math Function 1: 0 to 15																	
7..5		Reserved						RO	0x0							Reserved																	
4		MATHF_EN0						RW	0x0							Operation permission of Math Function 0																	
3..0		WID0						RW	0x0							FIFO Partition ID setting value allocated to Math Function 0: 0 to 15																	

3.9.12.3.28 {0x5090} MATHFUNC_POS0 Details

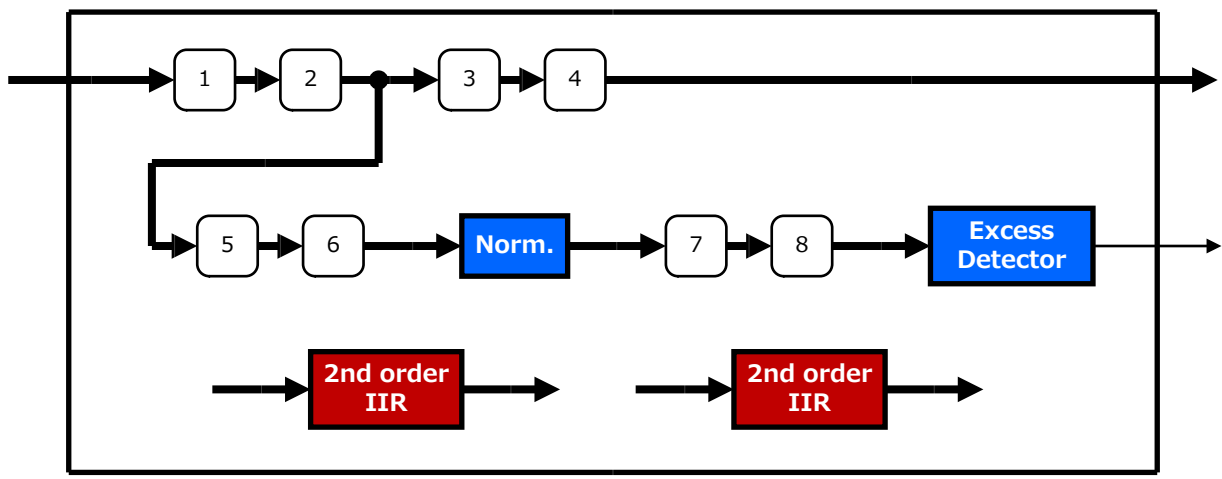


Figure SCU (Sensor Control Unit)-86 Processing Block Overview

In Figure SCU (Sensor Control Unit)-86, we call insertion IIR on the left side “IIR0”, insertion IIR on the right side “IIR1”.

The positions where IIRs are inserted are as follows:

- 4'b0001:{(1), (2)}
- 4'b0011:{(1), (3)}
- 4'b0101:{(1), (5)}
- 4'b1001:{(1), (7)}
- 4'b0010:{(3), (4)}
- 4'b0110:{(3), (5)}
- 4'b1010:{(3), (7)}
- 4'b0100:{(5), (6)}
- 4'b1100:{(5), (7)}
- 4'b1001:{(7), (8)}

Table SCU (Sensor Control Unit)-136

Local Address: 0x5090																Register Type: RW (read/write)															
Reset Value: 0x00000000																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												POS_0			
Bits		Name				Type		Reset Value				Description																			

31..4	Reserved	RO	0x00000000	Reserved
3..0	POS_0	RW	0x0	This designates the position where the IIR of Math Function 0 is inserted.

3.9.12.3.29 {0x5094} MATHFUNC_POS1 Details

As for the positions where the IIRs are inserted, refer to Section 3.9.12.3.28 {0x5090} MATHFUNC_POS0.

Table SCU (Sensor Control Unit)-137

Local Address: 0x5094																Register Type: RW (read/write) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved																												POS_1					
Bits		Name				Type		Reset Value				Description																					
31..4		Reserved				RO		0x00000000				Reserved																					
3..0		POS_1				RW		0x0				This designates the position where the IIR of Math Function 1 is inserted.																					

3.9.12.3.30 {0x5098} MATHFUNC_POS2 Details

As for the positions where the IIRs are inserted, refer to Section 3.9.12.3.28 {0x5090} MATHFUNC_POS0.

Table SCU (Sensor Control Unit)-138

Local Address: 0x5098																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										POS_2					
Bits		Name				Type	Reset Value				Description																				
31..4		Reserved				RO	0x00000000				Reserved																				
3..0		POS_2				RW	0x0				This designates the position where the IIR of Math Function 2 is inserted.																				

3.9.12.3.31 {0x50A0} MATHFUNC_PARAM_0_0 Details

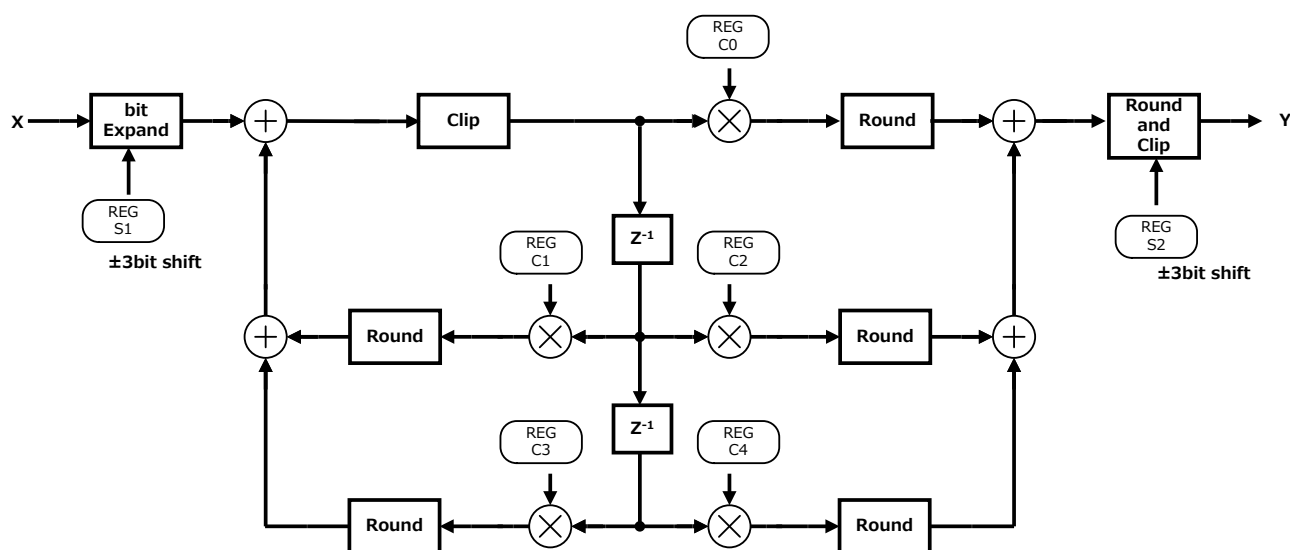


Figure SCU (Sensor Control Unit)-87 Filter Overview

Table SCU (Sensor Control Unit)-139

Local Address: 0x50A0																		Register Type: RW (read/write)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		S2				Reserved				S1					
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0				The IIR parameter for Math Function 0 ±3 bit shift at IIR0 outlet port Changing the setting value is prohibited during operation.																				
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0				The IIR parameter for Math Function 0 ±3 bit shift at IIR0 outlet port Changing the setting value is prohibited during operation.																				

3.9.12.3.32 {0x50A4} MATHFUNC_PARAM_C0_0_0_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-140

Local Address: 0x50A4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0																															
Bits		Name				Type	Reset Value				Description																				
31..0		C0				RW	0x00000000				Coefficient setting for IIR0 REG: C0 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.33 {0x50A8} MATHFUNC_PARAM_C0_0_0_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-141

Local Address: 0x50A8																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C0				RW	0x0				Coefficient setting for IIR0 REG: C0 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.34 {0x50B0} MATHFUNC_PARAM_C1_0_0_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-142

Local Address: 0x50B0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1																															
Bits		Name				Type	Reset Value				Description																				
31..0		C1				RW	0x00000000				Coefficient setting for IIR0 REG: C1 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.35 {0x50B4} MATHFUNC_PARAM_C1_0_0_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-143

Local Address: 0x50B4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C1				RW	0x0				Coefficient setting for IIR0 REG: C1 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.36 {0x50B8} MATHFUNC_PARAM_C2_0_0_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-144

Local Address: 0x50B8																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000				Coefficient setting for IIR0 REG: C2 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.37 {0x50BC} MATHFUNC_PARAM_C2_0_0_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-145

Local Address: 0x50BC																		Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
C2		Reserved																																	
Bits		Name						Type		Reset Value						Description																			
31..30		C2						RW		0x0						Coefficient setting for IIR0 REG: C2 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																			
29..0		Reserved						RO		0x00000000						Reserved																			

3.9.12.3.38 {0x50D0} MATHFUNC_PARAM_C3_0_0_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-146

Local Address: 0x50D0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type	Reset Value				Description																				
31..0		C3				RW	0x00000000				Coefficient setting for IIR0 REG: C3 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.39 {0x50D4} MATHFUNC_PARAM_C3_0_0_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-147

Local Address: 0x50D4																		Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
C3		Reserved																																	
Bits				Name				Type		Reset Value				Description																					
31..30				C3				RW		0x0				Coefficient setting for IIR0 REG: C3 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																					
29..0				Reserved				RO		0x00000000				Reserved																					

3.9.12.3.40 {0x50D8} MATHFUNC_PARAM_C4_0_0_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-148

Local Address: 0x50D8																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4																															
Bits		Name				Type	Reset Value				Description																				
31..0		C4				RW	0x00000000				Coefficient setting for IIR0 REG: C4 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.41 {0x50DC} MATHFUNC_PARAM_C4_0_0_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-149

Local Address: 0x50DC																		Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
C4		Reserved																																	
Bits				Name				Type		Reset Value				Description																					
31..30				C4				RW		0x0				Coefficient setting for IIR0 REG: C4 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																					
29..0				Reserved				RO		0x00000000				Reserved																					

3.9.12.3.42 {0x50E0} MATHFUNC_PARAM_0_1 Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-150

Local Address: 0x50E0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																S2		Reserved					S1								
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0				The IIR parameter for Math Function 0 ±3 bit shift at IIR1 outlet port Changing the setting value is prohibited during operation.																				
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0				The IIR parameter for Math Function 0 ±3 bit shift at IIR1 outlet port Changing the setting value is prohibited during operation.																				

3.9.12.3.43 {0x50E4} MATHFUNC_PARAM_C0_0_1_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-151

Local Address: 0x50E4																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0																															
Bits		Name				Type		Reset Value				Description																			
31..0		C0				RW		0x00000000				Coefficient setting for IIR0 REG: C0 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																			

3.9.12.3.44 {0x50E8} MATHFUNC_PARAM_C0_0_1_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-152

Local Address: 0x50E8																		Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0															
C0		Reserved																																					
Bits				Name				Type		Reset Value				Description																									
31..30				C0				RW		0x0				Coefficient setting for IIR0 REG: C0 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																									
29..0				Reserved				RO		0x00000000				Reserved																									

3.9.12.3.45 {0x50EC} MATHFUNC_PARAM_C1_0_1_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-153

Local Address: 0x50EC																				Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
C1																																			
Bits		Name						Type	Reset Value						Description																				
31..0		C1						RW	0x00000000						Coefficient setting for IIR0 REG: C1 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.46 {0x50F0} MATHFUNC_PARAM_C1_0_1_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-154

Local Address: 0x50F0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C1				RW	0x0				Coefficient setting for IIR0 REG: C1 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.47 {0x50F4} MATHFUNC_PARAM_C2_0_1_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-155

Local Address: 0x50F4																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000				Coefficient setting for IIR0 REG: C2 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																				

3.9.12.3.48 {0x50F8} MATHFUNC_PARAM_C2_0_1_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-156

Local Address: 0x50F8																		Register Type: RW (read/write) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
C2		Reserved																																	
Bits		Name				Type	Reset Value				Description																								
31..30		C2				RW	0x0				Coefficient setting for IIR0 REG: C2 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																								
29..0		Reserved				RO	0x00000000				Reserved																								

3.9.12.3.49 {0x50FC} MATHFUNC_PARAM_C3_0_1_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-157

Local Address: 0x50FC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type		Reset Value				Description																			
31..0		C3				RW		0x00000000				Coefficient setting for IIR0 REG: C3 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																			

3.9.12.3.50 {0x5100} MATHFUNC_PARAM_C3_0_1_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-158

Local Address: 0x5100																		Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0															
C3		Reserved																																					
Bits				Name								Type		Reset Value								Description																	
31..30				C3								RW		0x0								Coefficient setting for IIR0 REG: C3 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																	
29..0				Reserved								RO		0x00000000								Reserved																	

3.9.12.3.51 {0x5104} MATHFUNC_PARAM_C4_0_1_MSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-159

Local Address: 0x5104																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4																															
Bits		Name						Type	Reset Value						Description																
31..0		C4						RW	0x00000000						Coefficient setting for IIR0 REG: C4 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																

3.9.12.3.52 {0x5108} MATHFUNC_PARAM_C4_0_1_LSB Details

The IIR Parameter for Math Function 0

Table SCU (Sensor Control Unit)-160

Local Address: 0x5108																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4		Reserved																													
Bits		Name						Type	Reset Value						Description																
31..30		C4						RW	0x0						Coefficient setting for IIR0 REG: C4 Coefficient value format: (s2.31) Changing the setting value is prohibited during operation.																
29..0		Reserved						RO	0x00000000						Reserved																

3.9.12.3.53 {0x510C} MATHFUNC_PARAM_1_0 Details

The IIR Parameter for Math Function 1

Refer to {0x50A0} MATHFUNC_PARAM_0_0 Details

Table SCU (Sensor Control Unit)-161

Local Address: 0x510C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																S2		Reserved				S1									
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0																								
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0																								

3.9.12.3.54 {0x5110} MATHFUNC_PARAM_C0_1_0_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50A4} MATHFUNC_PARAM_C0_0_0_MSB Details

Table SCU (Sensor Control Unit)-162

Local Address: 0x5110																Register Type: RW (read/write) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C0																																
Bits		Name						Type	Reset Value						Description																	
31..0		C0						RW	0x00000000																							

3.9.12.3.55 {0x5114} MATHFUNC_PARAM_C0_1_0_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50A8} MATHFUNC_PARAM_C0_0_0_LSB Details

Table SCU (Sensor Control Unit)-163

Local Address: 0x5114																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C0		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C0				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.56 {0x5118} MATHFUNC_PARAM_C1_1_0_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50B0} MATHFUNC_PARAM_C1_0_0_MSB Details

Table SCU (Sensor Control Unit)-164

Local Address: 0x5118																Register Type: RW (read/write) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C1																																
Bits		Name						Type	Reset Value						Description																	
31..0		C1						RW	0x00000000																							

3.9.12.3.57 {0x511C} MATHFUNC_PARAM_C1_1_0_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50B4} MATHFUNC_PARAM_C1_0_0_LSB Details

Table SCU (Sensor Control Unit)-165

Local Address: 0x511C																Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
C1		Reserved																															
Bits				Name				Type		Reset Value				Description																			
31..30				C1				RW		0x0																							
29..0				Reserved				RO		0x00000000				Reserved																			

3.9.12.3.58 {0x5120} MATHFUNC_PARAM_C2_1_0_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50B8} MATHFUNC_PARAM_C2_0_0_MSB Details

Table SCU (Sensor Control Unit)-166

Local Address: 0x5120																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000																								

3.9.12.3.59 {0x5124} MATHFUNC_PARAM_C2_1_0_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50BC} MATHFUNC_PARAM_C2_0_0_LSB Details

Table SCU (Sensor Control Unit)-167

Local Address: 0x5124																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C2				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.60 {0x5128} MATHFUNC_PARAM_C3_1_0_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50D0} MATHFUNC_PARAM_C3_0_0_MSB Details

Table SCU (Sensor Control Unit)-168

Local Address: 0x5128																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type	Reset Value				Description																				
31..0		C3				RW	0x00000000																								

3.9.12.3.61 {0x512C} MATHFUNC_PARAM_C3_1_0_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50D4} MATHFUNC_PARAM_C3_0_0_LSB Details

Table SCU (Sensor Control Unit)-169

Local Address: 0x512C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C3				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

The IIR Parameter for Math Function 1

MATHFUNC PARAM C4 0 0 MSB Details

Table SCU (Sensor Control Unit)-170

Local Address: 0x5130																Register Type: RW (read/write) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C4																																
Bits		Name						Type	Reset Value						Description																	
31..0		C4						RW	0x00000000																							

3.9.12.3.63 {0x5134} MATHFUNC PARAM C4 1 0 LSB Details

The IIR Parameter for Math Function 1

Refer	to	{0x50DC}	MATHFUNC_PARAM_C4_0_0_LSB
Details	{0x50DC} MATHFUNC_PARAM_C4_0_0_LSB		

Table SCU (Sensor Control Unit)-171

Local Address: 0x5134																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C4				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.64 {0x5138} MATHFUNC_PARAM_1_1 Details

The IIR Parameter for Math Function 1

Refer to {0x50E0} MATHFUNC_PARAM_0_1 Details

Table SCU (Sensor Control Unit)-172

Local Address: 0x5138																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																S2		Reserved				S1									
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0																								
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0																								

3.9.12.3.65 {0x513C} MATHFUNC_PARAM_C0_1_1_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50E4} MATHFUNC_PARAM_C0_0_1_MSB Details

Table SCU (Sensor Control Unit)-173

Local Address: 0x513C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0																															
Bits		Name				Type	Reset Value				Description																				
31..0		C0				RW	0x00000000																								

3.9.12.3.66 {0x5140} MATHFUNC_PARAM_C0_1_1_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50E8} MATHFUNC_PARAM_C0_0_1_LSB Details

Table SCU (Sensor Control Unit)-174

Local Address: 0x5140																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C0		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C0				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.67 {0x5144} MATHFUNC_PARAM_C1_1_1_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50EC} MATHFUNC_PARAM_C1_0_1_MSB Details

Table SCU (Sensor Control Unit)-175

Local Address: 0x5144																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1																															
Bits		Name				Type		Reset Value				Description																			
31..0		C1				RW		0x00000000																							

3.9.12.3.68 {0x5148} MATHFUNC_PARAM_C1_1_1_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50F0} MATHFUNC_PARAM_C1_0_1_LSB Details

Table SCU (Sensor Control Unit)-176

Local Address: 0x5148																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C1				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.69 {0x514C} MATHFUNC_PARAM_C2_1_1_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50F4} MATHFUNC_PARAM_C2_0_1_MSB Details

Table SCU (Sensor Control Unit)-177

Local Address: 0x514C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000																								

3.9.12.3.70 {0x5150} MATHFUNC_PARAM_C2_1_1_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x50F8} MATHFUNC_PARAM_C2_0_1_LSB Details

Table SCU (Sensor Control Unit)-178

Local Address: 0x5150																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C2		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C2				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.71 {0x5154} MATHFUNC_PARAM_C3_1_1_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50FC} MATHFUNC_PARAM_C3_0_1_MSB
Details [{0x50FC} MATHFUNC_PARAM_C3_0_1_MSB](#)

Table SCU (Sensor Control Unit)-179

Local Address: 0x5154																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type	Reset Value				Description																				
31..0		C3				RW	0x00000000																								

3.9.12.3.72 {0x5158} MATHFUNC_PARAM_C3_1_1_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x5100} MATHFUNC_PARAM_C3_0_1_LSB Details

Table SCU (Sensor Control Unit)-180

Local Address: 0x5158																		Register Type: RW (read/write)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C3				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.73 {0x515C} MATHFUNC_PARAM_C4_1_1_MSB Details

The IIR Parameter for Math Function 1

Refer to {0x50FC} MATHFUNC_PARAM_C3_0_1_MSB Details

Table SCU (Sensor Control Unit)-181

Local Address: 0x515C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4																															
Bits		Name				Type	Reset Value				Description																				
31..0		C4				RW	0x00000000																								

3.9.12.3.74 {0x5160} MATHFUNC_PARAM_C4_1_1_LSB Details

The IIR Parameter for Math Function 1

Refer to {0x5100} MATHFUNC_PARAM_C3_0_1_LSB Details

Table SCU (Sensor Control Unit)-182

Local Address: 0x5160																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C4		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C4				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.75 {0x5164} MATHFUNC_PARAM_2_0 Details

The IIR Parameter for Math Function 2

Refer to {0x50A0} MATHFUNC_PARAM_0_0 Details

Table SCU (Sensor Control Unit)-183

Local Address: 0x5164																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																S2		Reserved				S1									
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0																								
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0																								

3.9.12.3.76 {0x5168} MATHFUNC_PARAM_C0_2_0_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50A4} MATHFUNC_PARAM_C0_0_0_MSB Details

Table SCU (Sensor Control Unit)-184

Local Address: 0x5168																Register Type: RW (read/write) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C0																																
Bits		Name						Type	Reset Value						Description																	
31..0		C0						RW	0x00000000																							

3.9.12.3.77 {0x516C} MATHFUNC_PARAM_C0_2_0_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50A8} MATHFUNC_PARAM_C0_0_0_LSB
Details [{0x50A8} MATHFUNC_PARAM_C0_0_0_LSB](#)

Table SCU (Sensor Control Unit)-185

Local Address: 0x516C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C0		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C0				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.78 {0x5170} MATHFUNC_PARAM_C1_2_0_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50B0} MATHFUNC_PARAM_C1_0_0_MSB
Details [{0x50B0} MATHFUNC_PARAM_C1_0_0_MSB](#)

Table SCU (Sensor Control Unit)-186

Local Address: 0x5170																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1																															
Bits		Name				Type	Reset Value				Description																				
31..0		C1				RW	0x00000000																								

3.9.12.3.79 {0x5174} MATHFUNC_PARAM_C1_2_0_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50B4} MATHFUNC_PARAM_C1_0_0_LSB Details

Table SCU (Sensor Control Unit)-187

Local Address: 0x5174																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C1		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C1				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.80 {0x5178} MATHFUNC_PARAM_C2_2_0_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50B8} MATHFUNC_PARAM_C2_0_0_MSB Details

Table SCU (Sensor Control Unit)-188

Local Address: 0x5178																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000																								

3.9.12.3.81 {0x517C} MATHFUNC_PARAM_C2_2_0_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50BC} MATHFUNC_PARAM_C2_0_0_LSB Details

Table SCU (Sensor Control Unit)-189

Local Address: 0x517C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C2		Reserved																													
Bits		Name						Type	Reset Value						Description																
31..30		C2						RW	0x0																						
29..0		Reserved						RO	0x00000000						Reserved																

3.9.12.3.82 {0x5180} MATHFUNC_PARAM_C3_2_0_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50D0} MATHFUNC_PARAM_C3_0_0_MSB Details

Table SCU (Sensor Control Unit)-190

Local Address: 0x5180																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type	Reset Value				Description																				
31..0		C3				RW	0x00000000																								

3.9.12.3.83 {0x5184} MATHFUNC_PARAM_C3_2_0_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50D4} MATHFUNC_PARAM_C3_0_0_LSB Details

Table SCU (Sensor Control Unit)-191

Local Address: 0x5184																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C3		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C3				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.84 {0x5188} MATHFUNC_PARAM_C4_2_0_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50D8} MATHFUNC_PARAM_C4_0_0_MSB Details

Table SCU (Sensor Control Unit)-192

Local Address: 0x5188																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4																															
Bits		Name				Type	Reset Value				Description																				
31..0		C4				RW	0x00000000																								

3.9.12.3.85 {0x518C} MATHFUNC_PARAM_C4_2_0_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50DC} MATHFUNC_PARAM_C4_0_0_LSB Details

Table SCU (Sensor Control Unit)-193

Local Address: 0x518C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C4				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.86 {0x5190} MATHFUNC_PARAM_2_1 Details

The IIR Parameter for Math Function 2

Table SCU (Sensor Control Unit)-194

Local Address: 0x5190																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																S2		Reserved				S1									
Bits		Name				Type	Reset Value				Description																				
31..11		Reserved				RO	0x000000				Reserved																				
10..8		S2				RW	0x0																								
7..3		Reserved				RO	0x00				Reserved																				
2..0		S1				RW	0x0																								

3.9.12.3.87 {0x5194} MATHFUNC_PARAM_C0_2_1_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50E4} MATHFUNC_PARAM_C0_0_1_MSB Details

Table SCU (Sensor Control Unit)-195

Local Address: 0x5194																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0																															
Bits		Name				Type	Reset Value				Description																				
31..0		C0				RW	0x00000000																								

3.9.12.3.88 {0x5198} MATHFUNC_PARAM_C0_2_1_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50E8} MATHFUNC_PARAM_C0_0_1_LSB
Details [{0x50E8} MATHFUNC_PARAM_C0_0_1_LSB](#)

Table SCU (Sensor Control Unit)-196

Local Address: 0x5198																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C0				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.89 {0x519C} MATHFUNC_PARAM_C1_2_1_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50EC} MATHFUNC_PARAM_C1_0_1_MSB
 Details [{0x50EC} MATHFUNC_PARAM_C1_0_1_MSB](#)

Table SCU (Sensor Control Unit)-197

Local Address: 0x519C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1																															
Bits		Name				Type		Reset Value				Description																			
31..0		C1				RW		0x00000000																							

3.9.12.3.90 {0x51A0} MATHFUNC_PARAM_C1_2_1_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50F0} MATHFUNC_PARAM_C1_0_1_LSB
 Details [{0x50F0} MATHFUNC_PARAM_C1_0_1_LSB](#)

Table SCU (Sensor Control Unit)-198

Local Address: 0x51A0																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C1		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C1				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.91 {0x51A4} MATHFUNC_PARAM_C2_2_1_MSB Details

The IIR Parameter for Math Function 2

Refer {0x50F4} MATHFUNC_PARAM_C2_0_1_MSB
 Details [{0x50F4} MATHFUNC_PARAM_C2_0_1_MSB](#)

Table SCU (Sensor Control Unit)-199

Local Address: 0x51A4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2																															
Bits		Name				Type	Reset Value				Description																				
31..0		C2				RW	0x00000000																								

3.9.12.3.92 {0x51A8} MATHFUNC_PARAM_C2_2_1_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x50F8} MATHFUNC_PARAM_C2_0_1_LSB Details

Table SCU (Sensor Control Unit)-200

Local Address: 0x51A8																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
C2		Reserved																													
Bits				Name				Type		Reset Value				Description																	
31..30				C2				RW		0x0																					
29..0				Reserved				RO		0x00000000				Reserved																	

3.9.12.3.93 {0x51AC} MATHFUNC_PARAM_C3_2_1_MSB Details

The IIR Parameter for Math Function 2

Refer {0x50FC} MATHFUNC_PARAM_C3_0_1_MSB
 Details [{0x50FC} MATHFUNC_PARAM_C3_0_1_MSB](#)

Table SCU (Sensor Control Unit)-201

Local Address: 0x51AC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3																															
Bits		Name				Type	Reset Value				Description																				
31..0		C3				RW	0x00000000																								

3.9.12.3.94 {0x51B0} MATHFUNC_PARAM_C3_2_1_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x5100} MATHFUNC_PARAM_C3_0_1_LSB
 Details [{0x5100} MATHFUNC_PARAM_C3_0_1_LSB](#)

Table SCU (Sensor Control Unit)-202

Local Address: 0x51B0																		Register Type: RW (read/write)													
Reset Value: 0x00000000																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3		Reserved																													
Bits		Name				Type	Reset Value				Description																				
31..30		C3				RW	0x0																								
29..0		Reserved				RO	0x00000000				Reserved																				

3.9.12.3.95 {0x51B4} MATHFUNC_PARAM_C4_2_1_MSB Details

The IIR Parameter for Math Function 2

Refer to {0x50FC} MATHFUNC_PARAM_C3_0_1_MSB
Details [{0x50FC} MATHFUNC_PARAM_C3_0_1_MSB](#)

Table SCU (Sensor Control Unit)-203

Local Address: 0x51B4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4																															
Bits		Name				Type	Reset Value				Description																				
31..0		C4				RW	0x00000000																								

3.9.12.3.96 {0x51B8} MATHFUNC_PARAM_C4_2_1_LSB Details

The IIR Parameter for Math Function 2

Refer to {0x5108} MATHFUNC_PARAM_C4_0_1_LSB Details

Table SCU (Sensor Control Unit)-204

Local Address: 0x51B8																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
C4		Reserved																																			
Bits				Name								Type		Reset Value								Description															
31..30				C4								RW		0x0																							
29..0				Reserved								RO		0x00000000								Reserved															

3.9.12.3.97 {0x51BC} EVENT_PARAM0_THRESH Details

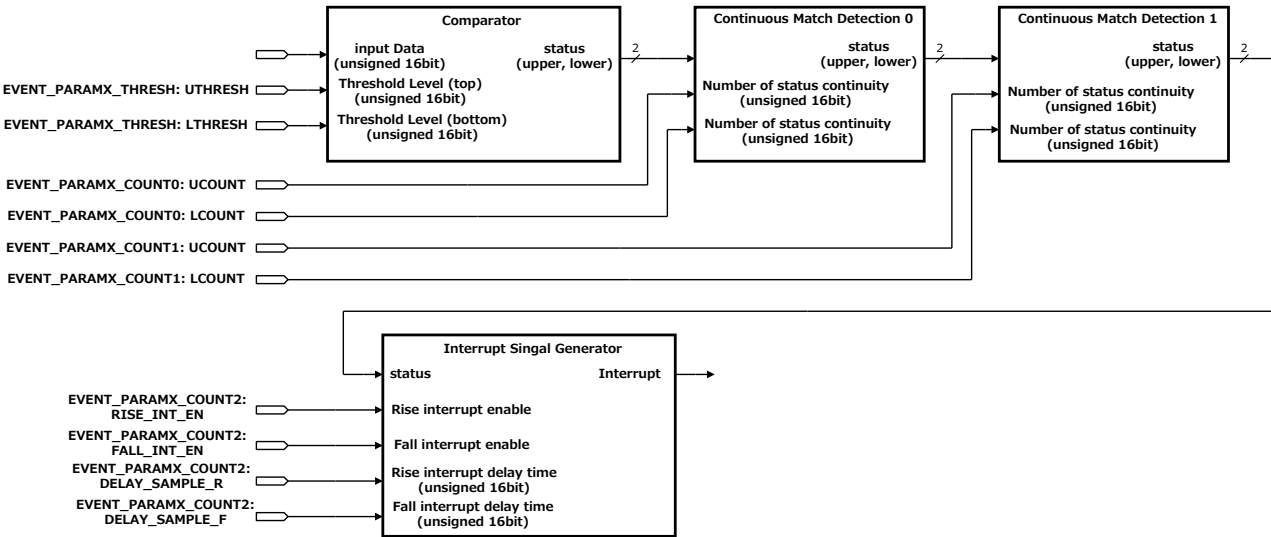


Figure SCU (Sensor Control Unit)-88 Excess Detection Overview

Excess detection for Math Function 0

Table SCU (Sensor Control Unit)-205

Local Address: 0x51BC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHRESH																UTHRESH															
Bits		Name				Type	Reset Value				Description																				
31..16		LTHRESH				RW	0x0000				Reference value for excess detection (bottom)																				
15..0		UTHRESH				RW	0x0000				Reference value for excess detection (top)																				

3.9.12.3.98 {0x51C0} EVENT_PARAM0_COUNT0 Details

Excess detection for Math Function 0

Table SCU (Sensor Control Unit)-206

Local Address: 0x51C0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name			Type	Reset Value		Description																								
31..16	LCOUNT			RW	0x0000		Designates how many times the input value exceeds the top threshold before the event ignition																								
15..0	UCOUNT			RW	0x0000		Designates how many times the input value exceeds the bottom threshold before the event ignition																								

3.9.12.3.99 {0x51C4} EVENT_PARAM0_COUNT1 Details

Excess detection for Math Function 0

Table SCU (Sensor Control Unit)-207

Local Address: 0x51C4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name			Type	Reset Value		Description																								
31..16	LCOUNT			RW	0x0000		Designates how many times the input value exceeds the top threshold before the event ignition																								
15..0	UCOUNT			RW	0x0000		Designates how many times the input value exceeds the bottom threshold before the event ignition																								

3.9.12.3.100 {0x51C8} EVENT_PARAM0_COUNT2 Details

Excess detection for Math Function 0

Table SCU (Sensor Control Unit)-208

Local Address: 0x51C8																Register Type: RW (read/write) Reset Value: 0x00000000																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																								FALL_INT_EN	Reserved												RISE_INT_EN
Bits	Name			Type	Reset Value			Description																													
31..9	Reserved			RO	0x000000			Reserved																													
8	FALL_INT_EN			RW	0x0			Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are bigger than the top threshold” to “determined serially that the input values are smaller than the bottom threshold”.																													
7..1	Reserved			RO	0x00			Reserved																													
0	RISE_INT_EN			RW	0x0			Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are smaller than the bottom threshold” to “determined serially that the input values are bigger than the top threshold”.																													

3.9.12.3.101 {0x51CC} EVENT_PARAM1_THRESH Details

Excess detection for Math Function 1

Table SCU (Sensor Control Unit)-209

Local Address: 0x51CC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHRESH																UTHRESH															
Bits		Name				Type	Reset Value				Description																				
31..16		LTHRESH				RW	0x0000				Reference value for excess detection (bottom)																				
15..0		UTHRESH				RW	0x0000				Reference value for excess detection (top)																				

3.9.12.3.102 {0x51D0} EVENT_PARAM1_COUNT0 Details

Excess detection for Math Function 1

Table SCU (Sensor Control Unit)-210

Local Address: 0x51D0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name		Type	Reset Value	Description																										
31..16	LCOUNT		RW	0x0000	Designates how many times the input value exceeds the top threshold before the event ignition																										
15..0	UCOUNT		RW	0x0000	Designates how many times the input value exceeds the bottom threshold before the event ignition																										

3.9.12.3.103 {0x51D4} EVENT_PARAM1_COUNT1 Details

Excess detection for Math Function 1

Table SCU (Sensor Control Unit)-211

Local Address: 0x51D4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name			Type	Reset Value	Description																									
31..16	LCOUNT			RW	0x0000	Designates how many times the input value exceeds the top threshold before the event ignition																									
15..0	UCOUNT			RW	0x0000	Designates how many times the input value exceeds the bottom threshold before the event ignition																									

3.9.12.3.104 {0x51D8} EVENT_PARAM1_COUNT2 Details

Excess detection for Math Function 1

Table SCU (Sensor Control Unit)-212

Local Address: 0x51D8																Register Type: RW (read/write) Reset Value: 0x00000000																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																								FALL_INT_EN	Reserved												RISE_INT_EN
Bits	Name			Type	Reset Value	Description																															
31..9	Reserved			RO	0x000000	Reserved																															
8	FALL_INT_EN			RW	0x0	Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are bigger than the top threshold” to “determined serially that the input values are smaller than the bottom threshold”.																															
7..1	Reserved			RO	0x00	Reserved																															
0	RISE_INT_EN			RW	0x0	Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are smaller than the bottom threshold” to “determined serially that the input values are bigger than the top threshold”.																															

3.9.12.3.105 {0x51DC} EVENT_PARAM2_THRESH Details

Excess detection for Math Function 2

Table SCU (Sensor Control Unit)-213

Local Address: 0x51DC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTHRESH																UTHRESH															
Bits		Name				Type	Reset Value				Description																				
31..16		LTHRESH				RW	0x0000				Bottom threshold																				
15..0		UTHRESH				RW	0x0000				Top threshold																				

3.9.12.3.106 {0x51E0} EVENT_PARAM2_COUNT0 Details

Excess detection for Math Function 2

Table SCU (Sensor Control Unit)-214

Local Address: 0x51E0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name		Type	Reset Value	Description																										
31..16	LCOUNT		RW	0x0000	Designates how many times the input value exceeds the top threshold before the event ignition																										
15..0	UCOUNT		RW	0x0000	Designates how many times the input value exceeds the bottom threshold before the event ignition																										

3.9.12.3.107 {0x51E4} EVENT_PARAM2_COUNT1 Details

Excess detection for Math Function 2

Table SCU (Sensor Control Unit)-215

Local Address: 0x51E4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCOUNT																UCOUNT															
Bits	Name		Type	Reset Value	Description																										
31..16	LCOUNT		RW	0x0000	Designates how many times the input value exceeds the top threshold before the event ignition																										
15..0	UCOUNT		RW	0x0000	Designates how many times the input value exceeds the bottom threshold before the event ignition																										

3.9.12.3.108 {0x51E8} EVENT_PARAM2_COUNT2 Details

Excess detection for Math Function 2

Table SCU (Sensor Control Unit)-216

Local Address: 0x51E8																						Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																						FALL_INT_EN	Reserved												RISE_INT_EN		
Bits	Name							Type	Reset Value	Description																											
31..9	Reserved							RO	0x000000	Reserved																											
8	FALL_INT_EN							RW	0x0	Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are bigger than the top threshold” to “determined serially that the input values are smaller than the bottom threshold”.																											
7..1	Reserved							RO	0x00	Reserved																											
0	RISE_INT_EN							RW	0x0	Interrupt occurrence permission in the case that the status has changed from “determined serially that the input values are smaller than the bottom threshold” to “determined serially that the input values are bigger than the top threshold”.																											

3.9.12.3.109 {0x51EC} EVENT_PARAM0_DELAY_SAMPLE Details

Table SCU (Sensor Control Unit)-217

Local Address: 0x51EC																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
DELAY_SAMPLE_F																DELAY_SAMPLE_R															
Bits		Name						Type		Reset Value				Description																	
31..16		DELAY_SAMPLE_F						RW		0x0000				After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																	
15..0		DELAY_SAMPLE_R						RW		0x0000				After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																	

3.9.12.3.110 {0x51F0} EVENT_PARAM1_DELAY_SAMPLE Details

Table SCU (Sensor Control Unit)-218

Local Address: 0x51F0																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
DELAY_SAMPLE_F																DELAY_SAMPLE_R															
Bits		Name						Type	Reset Value						Description																
31..16		DELAY_SAMPLE_F						RW	0x0000						After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																
15..0		DELAY_SAMPLE_R						RW	0x0000						After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																

3.9.12.3.111 {0x51F4} EVENT_PARAM2_DELAY_SAMPLE Details

Table SCU (Sensor Control Unit)-219

Local Address: 0x51F4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAY_SAMPLE_F																DELAY_SAMPLE_R															
Bits		Name				Type		Reset Value				Description																			
31..16		DELAY_SAMPLE_F				RW		0x0000				After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																			
15..0		DELAY_SAMPLE_R				RW		0x0000				After the conditions of the event ignition is fulfilled, this register designates how many samples must be taken before the event ignition.																			

3.9.12.3.112 {0x5200} EVENT_TIMESTAMP0_R_MSB Details

Table SCU (Sensor Control Unit)-220

Local Address: 0x5200																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP																															
Bits		Name				Type	Reset Value				Description																				
31..0		TIMESTAMP				RO	0x00000000				Time stamp value (integer part of second) at the EVENT0 occurrence																				

3.9.12.3.113 {0x5204} EVENT_TIMESTAMP0_R_LSB Details

Table SCU (Sensor Control Unit)-221

Local Address: 0x5204																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TIMESTAMP																
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		TIMESTAMP				RO	0x0000				Time stamp value (second after the decimal point) at the EVENT0 occurrence																				

3.9.12.3.114 {0x5208} EVENT_TIMESTAMP1_R_MSB Details

Table SCU (Sensor Control Unit)-222

Local Address: 0x5208																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TIMESTAMP																																
Bits		Name						Type	Reset Value						Description																	
31..0		TIMESTAMP						RO	0x00000000						Time stamp value (integer part of second) at the EVENT1 occurrence																	

3.9.12.3.115 {0x520C} EVENT_TIMESTAMP1_R_LSB Details

Table SCU (Sensor Control Unit)-223

Local Address: 0x520C																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TIMESTAMP															
Bits		Name				Type		Reset Value				Description																			
31..15		Reserved				RO		0x00000				Reserved																			
14..0		TIMESTAMP				RO		0x0000				Time stamp value (second after the decimal point at the EVENT1 occurrence																			

3.9.12.3.116 {0x5210} EVENT_TIMESTAMP2_R_MSB Details

Table SCU (Sensor Control Unit)-224

Local Address: 0x5210																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TIMESTAMP																																
Bits		Name						Type	Reset Value						Description																	
31..0		TIMESTAMP						RO	0x00000000						Time stamp value (integer part of second) at the EVENT2 occurrence																	

3.9.12.3.117 {0x5214} EVENT_TIMESTAMP2_R_LSB Details

Table SCU (Sensor Control Unit)-225

Local Address: 0x5214																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TIMESTAMP															
Bits		Name				Type		Reset Value				Description																			
31..15		Reserved				RO		0x00000				Reserved																			
14..0		TIMESTAMP				RO		0x0000				Time stamp value (second after the decimal point) at the EVENT2 occurrence																			

3.9.12.3.118 {0x5218} EVENT_TIMESTAMP0_F_MSB Details

Table SCU (Sensor Control Unit)-226

Local Address: 0x5218																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TIMESTAMP																																
Bits		Name						Type	Reset Value						Description																	
31..0		TIMESTAMP						RO	0x00000000						Time stamp value (integer part of second) at the EVENT0 occurrence																	

3.9.12.3.119 {0x521C} EVENT_TIMESTAMP0_F_LSB Details

Table SCU (Sensor Control Unit)-227

Local Address: 0x521C																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TIMESTAMP															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		TIMESTAMP						RO	0x0000						Time stamp value (second after the decimal point) at the EVENT0 occurrence																

3.9.12.3.120 {0x5220} EVENT_TIMESTAMP1_F_MSB Details

Table SCU (Sensor Control Unit)-228

Local Address: 0x5220																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TIMESTAMP																																
Bits		Name						Type	Reset Value						Description																	
31..0		TIMESTAMP						RO	0x00000000						Time stamp value (integer part of second) at the EVENT1 occurrence																	

3.9.12.3.121 {0x5224} EVENT_TIMESTAMP1_F_LSB Details

Table SCU (Sensor Control Unit)-229

Local Address: 0x5224																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TIMESTAMP															
Bits		Name				Type		Reset Value				Description																			
31..15		Reserved				RO		0x00000				Reserved																			
14..0		TIMESTAMP				RO		0x0000				Time stamp value (second after the decimal point) at the EVENT1 occurrence																			

3.9.12.3.122 {0x5228} EVENT_TIMESTAMP2_F_MSB Details

Table SCU (Sensor Control Unit)-230

Local Address: 0x5228																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP																															
Bits		Name				Type	Reset Value				Description																				
31..0		TIMESTAMP				RO	0x00000000				Time stamp value (integer part of second) at the EVENT2 occurrence																				

3.9.12.3.123 {0x522C} EVENT_TIMESTAMP2_F_LSB Details

Table SCU (Sensor Control Unit)-231

Local Address: 0x522C																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TIMESTAMP															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		TIMESTAMP				RO	0x0000				Time stamp value (second after the decimal point) at the EVENT2 occurrence																				

3.9.12.3.124 {0x5230} FIFO_WRITE_CTRL Details

Table SCU (Sensor Control Unit)-232

Local Address: 0x5230																						Register Type: RW (read/write) Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																						EVENT2_F	EVENT1_F	EVENT0_F	EVENT2_R	EVENT1_R	EVENT0_R								
Bits	Name		Type	Reset Value	Description																														
31..6	Reserved		RO	0x00000000	Reserved																														
5	EVENT2_F		RW	0x0																															
4	EVENT1_F		RW	0x0																															
3	EVENT0_F		RW	0x0																															
2	EVENT2_R		RW	0x0																															
1	EVENT1_R		RW	0x0																															
0	EVENT0_R		RW	0x0	The status of MATH_EVENT. It is referred when writing data to the FIFO. It can be cleared by writing “1”.																														

3.9.12.3.125 {0x5400} INT_ENABLE_MAIN Details

Table SCU (Sensor Control Unit)-233

Local Address: 0x5400																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								D1_R3_CH_ALMOST_FULL								N2_R1_C_ALMOST_FULL								MATH_EVENT2_R							
MATH_EVENT2_F								D0_R3_CH_ALMOST_FULL								N1_R1_C_ALMOST_FULL								MATH_EVENT1_R							
MATH_EVENT1_F								N7_R1_C_ALMOST_FULL								N0_R1_C_ALMOST_FULL								MATH_EVENT0_R							
MATH_EVENT0_F								N6_R1_C_ALMOST_FULL								D1_R2_C_ALMOST_FULL								HPADC1_ALMOST_FULL							
ISOP3								N5_R1_C_ALMOST_FULL								D1_R1_C_ALMOST_FULL								HPADC0_ALMOST_FULL							
ISOP2								N4_R1_C_ALMOST_FULL								D0_R2_C_ALMOST_FULL								LPADC_ALMOST_FULL							
ISOP1								N3_R1_C_ALMOST_FULL								D0_R1_C_ALMOST_FULL								I2C1							
ISOP0																								I2C0							
Reserved																								SPI							
Bits	Name							Type	Reset Value	Description																					
31	Reserved							RO	0x0	Reserved																					
30	MATH_EVENT2_F							RW	0x0																						
29	MATH_EVENT1_F							RW	0x0																						
28	MATH_EVENT0_F							RW	0x0																						
27	ISOP3							RW	0x0																						
26	ISOP2							RW	0x0																						
25	ISOP1							RW	0x0																						
24	ISOP0							RW	0x0																						
23	Reserved							RO	0x0	Reserved																					
22	D1_R3_CH_ALMOST_FULL							RW	0x0																						
21	D0_R3_CH_ALMOST_FULL							RW	0x0																						
20	N7_R1_C_ALMOST_FULL							RW	0x0																						
19	N6_R1_C_ALMOST_FULL							RW	0x0																						
18	N5_R1_C_ALMOST_FULL							RW	0x0																						
17	N4_R1_C_ALMOST_FULL							RW	0x0																						
16	N3_R1_C_ALMOST_FULL							RW	0x0																						
15	N2_R1_C_ALMOST_FULL							RW	0x0																						
14	N1_R1_C_ALMOST_FULL							RW	0x0																						
13	N0_R1_C_ALMOST_FULL							RW	0x0																						
12	D1_R2_C_ALMOST_FULL							RW	0x0																						

11	D1_R1_C_ALMOST_FULL	RW	0x0	
10	D0_R2_C_ALMOST_FULL	RW	0x0	
9	D0_R1_C_ALMOST_FULL	RW	0x0	
8	MATH_EVENT2_R	RW	0x0	
7	MATH_EVENT1_R	RW	0x0	
6	MATH_EVENT0_R	RW	0x0	
5	HPADC1_ALMOST_FULL	RW	0x0	
4	HPADC0_ALMOST_FULL	RW	0x0	
3	LPADC_ALMOST_FULL	RW	0x0	
2	I2C1	RW	0x0	
1	I2C0	RW	0x0	
0	SPI	RW	0x0	Interrupt permission for the SPI or Math Function Event 0. The interrupt is permitted by writing “1”. Writing “0” cannot prohibit the interrupt.

3.9.12.3.126 {0x5404} INT_DISABLE_MAIN Details

Table SCU (Sensor Control Unit)-234

Local Address: 0x5404																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								D1_R3_CH_ALMOST_FULL								N2_R1_C_ALMOST_FULL								MATH_EVENT2_R							
MATH_EVENT2_F								D0_R3_CH_ALMOST_FULL								N1_R1_C_ALMOST_FULL								MATH_EVENT1_R							
MATH_EVENT1_F								N7_R1_C_ALMOST_FULL								N0_R1_C_ALMOST_FULL								MATH_EVENT0_R							
MATH_EVENT0_F								N6_R1_C_ALMOST_FULL								D1_R2_C_ALMOST_FULL								HPADC1_ALMOST_FULL							
ISOP3								N5_R1_C_ALMOST_FULL								D0_R2_C_ALMOST_FULL								HPADC0_ALMOST_FULL							
ISOP2								N4_R1_C_ALMOST_FULL								D0_R1_C_ALMOST_FULL								LPADC_ALMOST_FULL							
ISOP1								N3_R1_C_ALMOST_FULL																							
ISOP0																															
Reserved																															
								</																							

11	D1_R1_C_ALMOST_FULL	RW	0x0	
10	D0_R2_C_ALMOST_FULL	RW	0x0	
9	D0_R1_C_ALMOST_FULL	RW	0x0	
8	MATH_EVENT2_R	RW	0x0	
7	MATH_EVENT1_R	RW	0x0	
6	MATH_EVENT0_R	RW	0x0	
5	HPADC1_ALMOST_FULL	RW	0x0	
4	HPADC0_ALMOST_FULL	RW	0x0	
3	LPADC_ALMOST_FULL	RW	0x0	
2	I2C1	RW	0x0	
1	I2C0	RW	0x0	
0	SPI	RW	0x0	Interrupt prohibition for the SPI. The interrupt is prohibited by writing “1”. Writing “0” cannot permit the interrupt.

3.9.12.3.127 {0x5408} INT_CLEAR_MAIN Details

Table SCU (Sensor Control Unit)-235

Local Address: 0x5408																Register Type: WO (write only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved MATH_EVENT2_F MATH_EVENT1_F MATH_EVENT0_F ISOP3 ISOP2 ISOP1 ISOP0								Reserved D1_R3_CH_ALMOST_FULL D0_R3_CH_ALMOST_FULL N7_R1_C_ALMOST_FULL N6_R1_C_ALMOST_FULL N5_R1_C_ALMOST_FULL N4_R1_C_ALMOST_FULL N3_R1_C_ALMOST_FULL N2_R1_C_ALMOST_FULL N1_R1_C_ALMOST_FULL N0_R1_C_ALMOST_FULL D1_R2_C_ALMOST_FULL D1_R1_C_ALMOST_FULL D0_R2_C_ALMOST_FULL D0_R1_C_ALMOST_FULL MATH_EVENT2_R MATH_EVENT1_R MATH_EVENT0_R HPADC1_ALMOST_FULL HPADC0_ALMOST_FULL LPADC_ALMOST_FULL								Reserved															
Bits	Name							Type	Reset Value	Description																					
31	Reserved							WO	0x0	Reserved																					
30	MATH_EVENT2_F							WO	0x0																						
29	MATH_EVENT1_F							WO	0x0																						
28	MATH_EVENT0_F							WO	0x0																						
27	ISOP3							WO	0x0																						
26	ISOP2							WO	0x0																						
25	ISOP1							WO	0x0																						
24	ISOP0							WO	0x0																						
23	Reserved							WO	0x0	Reserved																					
22	D1_R3_CH_ALMOST_FULL							WO	0x0																						
21	D0_R3_CH_ALMOST_FULL							WO	0x0																						
20	N7_R1_C_ALMOST_FULL							WO	0x0																						
19	N6_R1_C_ALMOST_FULL							WO	0x0																						
18	N5_R1_C_ALMOST_FULL							WO	0x0																						
17	N4_R1_C_ALMOST_FULL							WO	0x0																						
16	N3_R1_C_ALMOST_FULL							WO	0x0																						
15	N2_R1_C_ALMOST_FULL							WO	0x0																						
14	N1_R1_C_ALMOST_FULL							WO	0x0																						
13	N0_R1_C_ALMOST_FULL							WO	0x0																						
12	D1_R2_C_ALMOST_FULL							WO	0x0																						
11	D1_R1_C_ALMOST_FULL							WO	0x0																						

10	D0_R2_C_ALMOST_FULL	WO	0x0	
9	D0_R1_C_ALMOST_FULL	WO	0x0	
8	MATH_EVENT2_R	WO	0x0	
7	MATH_EVENT1_R	WO	0x0	
6	MATH_EVENT0_R	WO	0x0	
5	HPADC1_ALMOST_FULL	WO	0x0	
4	HPADC0_ALMOST_FULL	WO	0x0	
3	LPADC_ALMOST_FULL	WO	0x0	
2..0	Reserved	WO	0x0	Reserved

3.9.12.3.128 {0x540C} LEVEL_SEL_MAIN Details

Table SCU (Sensor Control Unit)-236

Local Address: 0x540C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								ISOP3 ISOP2 ISOP1 ISOP0 Reserved D1_R3_CH_ALMOST_FULL D0_R3_CH_ALMOST_FULL N7_R1_C_ALMOST_FULL N6_R1_C_ALMOST_FULL N5_R1_C_ALMOST_FULL N4_R1_C_ALMOST_FULL N3_R1_C_ALMOST_FULL N2_R1_C_ALMOST_FULL N1_R1_C_ALMOST_FULL N0_R1_C_ALMOST_FULL D1_R2_C_ALMOST_FULL D1_R1_C_ALMOST_FULL D0_R2_C_ALMOST_FULL D0_R1_C_ALMOST_FULL								Reserved HPADC1_ALMOST_FULL HPADC0_ALMOST_FULL LPADC_ALMOST_FULL Reserved															
Bits	Name							Type	Reset Value	Description																					
31..28	Reserved							RO	0x0	Reserved																					
27	ISOP3							RW	0x0																						
26	ISOP2							RW	0x0																						
25	ISOP1							RW	0x0																						
24	ISOP0							RW	0x0																						
23	Reserved							RO	0x0	Reserved																					
22	D1_R3_CH_ALMOST_FULL							RW	0x0																						
21	D0_R3_CH_ALMOST_FULL							RW	0x0																						
20	N7_R1_C_ALMOST_FULL							RW	0x0																						
19	N6_R1_C_ALMOST_FULL							RW	0x0																						
18	N5_R1_C_ALMOST_FULL							RW	0x0																						
17	N4_R1_C_ALMOST_FULL							RW	0x0																						
16	N3_R1_C_ALMOST_FULL							RW	0x0																						
15	N2_R1_C_ALMOST_FULL							RW	0x0																						
14	N1_R1_C_ALMOST_FULL							RW	0x0																						
13	N0_R1_C_ALMOST_FULL							RW	0x0																						
12	D1_R2_C_ALMOST_FULL							RW	0x0																						
11	D1_R1_C_ALMOST_FULL							RW	0x0																						
10	D0_R2_C_ALMOST_FULL							RW	0x0																						
9	D0_R1_C_ALMOST_FULL							RW	0x0																						

8..6	Reserved	RO	0x0	Reserved
5	HPADC1_ALMOST_FULL	RW	0x0	
4	HPADC0_ALMOST_FULL	RW	0x0	
3	LPADC_ALMOST_FULL	RW	0x0	Set “1” when you want to use interrupt LPADC_ALMOST_FULL as a level interrupt. Set “0” when you use the interrupt as an edge detection.
2..0	Reserved	RO	0x0	Reserved

3.9.12.3.129 {0x5410} INT_RAW_STT_MAIN Details

Table SCU (Sensor Control Unit)-237

Local Address: 0x5410																Register Type: RO (read only) Reset Value: 0x00000000																		
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0										
Reserved	MATH_EVENT2_F	MATH_EVENT1_F	MATH_EVENT0_F	ISOP3	ISOP2	ISOP1	ISOP0	Reserved	D1_R3_CH_ALMOST_FULL	D0_R3_CH_ALMOST_FULL	N7_R1_C_ALMOST_FULL	N6_R1_C_ALMOST_FULL	N5_R1_C_ALMOST_FULL	N4_R1_C_ALMOST_FULL	N3_R1_C_ALMOST_FULL	N2_R1_C_ALMOST_FULL	N1_R1_C_ALMOST_FULL	N0_R1_C_ALMOST_FULL	D1_R2_C_ALMOST_FULL	D1_R1_C_ALMOST_FULL	D0_R2_C_ALMOST_FULL	D0_R1_C_ALMOST_FULL	MATH_EVENT2_R	MATH_EVENT1_R	MATH_EVENT0_R	HPADC1_ALMOST_FULL	HPADC0_ALMOST_FULL	LPADC_ALMOST_FULL	I2C1	I2C0	SPI			
	Bits	Name							Type	Reset Value	Description																							
	31	Reserved							RO	0x0	Reserved																							
	30	MATH_EVENT2_F							RO	0x0																								
	29	MATH_EVENT1_F							RO	0x0																								
	28	MATH_EVENT0_F							RO	0x0																								
	27	ISOP3							RO	0x0																								
	26	ISOP2							RO	0x0																								
	25	ISOP1							RO	0x0																								
	24	ISOP0							RO	0x0																								
	23	Reserved							RO	0x0	Reserved																							
	22	D1_R3_CH_ALMOST_FULL							RO	0x0																								
	21	D0_R3_CH_ALMOST_FULL							RO	0x0																								
20	N7_R1_C_ALMOST_FULL							RO	0x0																									
19	N6_R1_C_ALMOST_FULL							RO	0x0																									
18	N5_R1_C_ALMOST_FULL							RO	0x0																									
17	N4_R1_C_ALMOST_FULL							RO	0x0																									
16	N3_R1_C_ALMOST_FULL							RO	0x0																									
15	N2_R1_C_ALMOST_FULL							RO	0x0																									
14	N1_R1_C_ALMOST_FULL							RO	0x0																									
13	N0_R1_C_ALMOST_FULL							RO	0x0																									
12	D1_R2_C_ALMOST_FULL							RO	0x0																									
11	D1_R1_C_ALMOST_FULL							RO	0x0																									

10	D0_R2_C_ALMOST_FULL	RO	0x0	
9	D0_R1_C_ALMOST_FULL	RO	0x0	
8	MATH_EVENT2_R	RO	0x0	
7	MATH_EVENT1_R	RO	0x0	
6	MATH_EVENT0_R	RO	0x0	
5	HPADC1_ALMOST_FULL	RO	0x0	
4	HPADC0_ALMOST_FULL	RO	0x0	
3	LPADC_ALMOST_FULL	RO	0x0	
2	I2C1	RO	0x0	
1	I2C0	RO	0x0	
0	SPI	RO	0x0	The interrupt status of the SPI or Math Function Event 0 before masking

3.9.12.3.130 {0x5414} INT_MASKED_STT_MAIN Details

Table SCU (Sensor Control Unit)-238

Local Address: 0x5414																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALL_ORED_ERR	MATH_EVENT2_F	MATH_EVENT1_F	MATH_EVENT0_F	ISOP3	ISOP2	ISOP1	ISOP0	Reserved	D1_R3_CH_ALMOST_FULL	D0_R3_CH_ALMOST_FULL	N7_R1_C_ALMOST_FULL	N6_R1_C_ALMOST_FULL	N5_R1_C_ALMOST_FULL	N4_R1_C_ALMOST_FULL	N3_R1_C_ALMOST_FULL	N2_R1_C_ALMOST_FULL	N1_R1_C_ALMOST_FULL	N0_R1_C_ALMOST_FULL	D1_R2_C_ALMOST_FULL	D1_R1_C_ALMOST_FULL	D0_R2_C_ALMOST_FULL	D0_R1_C_ALMOST_FULL	MATH_EVENT2_R	MATH_EVENT1_R	MATH_EVENT0_R	HPADC1_ALMOST_FULL	HPADC0_ALMOST_FULL	LPADC_ALMOST_FULL	I2C1	I2C0	SPI
Bits	Name										Type	Reset Value	Description																		
31	ALL_ORED_ERR										RO	0x0																			
30	MATH_EVENT2_F										RO	0x0																			
29	MATH_EVENT1_F										RO	0x0																			
28	MATH_EVENT0_F										RO	0x0																			
27	ISOP3										RO	0x0																			
26	ISOP2										RO	0x0																			
25	ISOP1										RO	0x0																			
24	ISOP0										RO	0x0																			
23	Reserved										RO	0x0	Reserved																		
22	D1_R3_CH_ALMOST_FULL										RO	0x0																			
21	D0_R3_CH_ALMOST_FULL										RO	0x0																			
20	N7_R1_C_ALMOST_FULL										RO	0x0																			
19	N6_R1_C_ALMOST_FULL										RO	0x0																			
18	N5_R1_C_ALMOST_FULL										RO	0x0																			
17	N4_R1_C_ALMOST_FULL										RO	0x0																			
16	N3_R1_C_ALMOST_FULL										RO	0x0																			
15	N2_R1_C_ALMOST_FULL										RO	0x0																			
14	N1_R1_C_ALMOST_FULL										RO	0x0																			
13	N0_R1_C_ALMOST_FULL										RO	0x0																			
12	D1_R2_C_ALMOST_FULL										RO	0x0																			
11	D1_R1_C_ALMOST_FULL										RO	0x0																			

10	D0_R2_C_ALMOST_FULL	RO	0x0	
9	D0_R1_C_ALMOST_FULL	RO	0x0	
8	MATH_EVENT2_R	RO	0x0	
7	MATH_EVENT1_R	RO	0x0	
6	MATH_EVENT0_R	RO	0x0	
5	HPADC1_ALMOST_FULL	RO	0x0	
4	HPADC0_ALMOST_FULL	RO	0x0	
3	LPADC_ALMOST_FULL	RO	0x0	
2	I2C1	RO	0x0	
1	I2C0	RO	0x0	
0	SPI	RO	0x0	The interrupt status of the SPI or Math Function Event 0 after masking

3.9.12.3.131 {0x5420} INT_ENABLE_ERR_0 Details

Table SCU (Sensor Control Unit)-239

Local Address: 0x5420																Register Type: RW (read/write) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved	PWM7_INVALID_VALUE	PWM6_INVALID_VALUE	PWM5_INVALID_VALUE	PWM4_INVALID_VALUE	PWM3_INVALID_VALUE	PWM2_INVALID_VALUE	PWM1_INVALID_VALUE	PWM0_INVALID_VALUE	D1_R3_CH_OVER_RUN	D0_R3_CH_OVER_RUN	N7_R1_C_OVER_RUN	N6_R1_C_OVER_RUN	N5_R1_C_OVER_RUN	N4_R1_C_OVER_RUN	N3_R1_C_OVER_RUN	N2_R1_C_OVER_RUN	N1_R1_C_OVER_RUN	N0_R1_C_OVER_RUN	D1_R2_C_OVER_RUN	D1_R1_C_OVER_RUN	D0_R2_C_OVER_RUN	D0_R1_C_OVER_RUN	Reserved	ADCIF_READ_ERR	HPADC1_OVER_RUN	HPADC0_OVER_RUN	LPADC_OVER_RUN	LPADC_OVER_RUN3	LPADC_OVER_RUN2	LPADC_OVER_RUN1					
	Bits	Name								Type	Reset Value								Description																
	31	Reserved								RO	0x0								Reserved																
	30	PWM7_INVALID_VALUE								RW	0x0																								
	29	PWM6_INVALID_VALUE								RW	0x0																								
	28	PWM5_INVALID_VALUE								RW	0x0																								
	27	PWM4_INVALID_VALUE								RW	0x0																								
	26	PWM3_INVALID_VALUE								RW	0x0																								
	25	PWM2_INVALID_VALUE								RW	0x0																								
	24	PWM1_INVALID_VALUE								RW	0x0								Interrupt permission to detect outlier setting (CYCLE < THRESH) to PWM1																
	23	PWM0_INVALID_VALUE								RW	0x0								Interrupt permission to detect outlier setting (CYCLE < THRESH) to PWM0																
	22	D1_R3_CH_OVER_RUN								RW	0x0																								
	21	D0_R3_CH_OVER_RUN								RW	0x0																								
	20	N7_R1_C_OVER_RUN								RW	0x0																								
	19	N6_R1_C_OVER_RUN								RW	0x0																								
	18	N5_R1_C_OVER_RUN								RW	0x0																								
17	N4_R1_C_OVER_RUN								RW	0x0																									
16	N3_R1_C_OVER_RUN								RW	0x0																									
15	N2_R1_C_OVER_RUN								RW	0x0																									
14	N1_R1_C_OVER_RUN								RW	0x0																									
13	N0_R1_C_OVER_RUN								RW	0x0																									
12	D1_R2_C_OVER_RUN								RW	0x0																									

11	D1_R1_C_OVER_RUN	RW	0x0	
10	D0_R2_C_OVER_RUN	RW	0x0	
9	D0_R1_C_OVER_RUN	RW	0x0	
8..7	Reserved	RO	0x0	Reserved
6	ADCIF_READ_ERR	RW	0x0	
5	HPADC1_OVER_RUN	RW	0x0	
4	HPADC0_OVER_RUN	RW	0x0	
3	LPADC_OVER_RUN	RW	0x0	
2	LPADC_OVER_RUN3	RW	0x0	
1	LPADC_OVER_RUN2	RW	0x0	
0	LPADC_OVER_RUN1	RW	0x0	

3.9.12.3.132 {0x5424} INT_DISABLE_ERR_0 Details

Table SCU (Sensor Control Unit)-240

Local Address: 0x5424																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	PWM7_INVALID_VALUE	PWM6_INVALID_VALUE	PWM5_INVALID_VALUE	PWM4_INVALID_VALUE	PWM3_INVALID_VALUE	PWM2_INVALID_VALUE	PWM1_INVALID_VALUE	PWM0_INVALID_VALUE	D1_R3_CH_OVER_RUN	D0_R3_CH_OVER_RUN	N7_R1_C_OVER_RUN	N6_R1_C_OVER_RUN	N5_R1_C_OVER_RUN	N4_R1_C_OVER_RUN	N3_R1_C_OVER_RUN	N2_R1_C_OVER_RUN	N1_R1_C_OVER_RUN	N0_R1_C_OVER_RUN	D1_R2_C_OVER_RUN	D1_R1_C_OVER_RUN	D0_R2_C_OVER_RUN	D0_R1_C_OVER_RUN	Reserved	ADCIF_READ_ERR	HPADC1_OVER_RUN	HPADC0_OVER_RUN	LPADC_OVER_RUN	LPADC_OVER_RUN3	LPADC_OVER_RUN2	LPADC_OVER_RUN1	
	Bits	Name								Type	Reset Value				Description																
	31	Reserved								RO	0x0				Reserved																
	30	PWM7_INVALID_VALUE								RW	0x0																				
	29	PWM6_INVALID_VALUE								RW	0x0																				
	28	PWM5_INVALID_VALUE								RW	0x0																				
	27	PWM4_INVALID_VALUE								RW	0x0																				
	26	PWM3_INVALID_VALUE								RW	0x0																				
	25	PWM2_INVALID_VALUE								RW	0x0																				
	24	PWM1_INVALID_VALUE								RW	0x0				Interrupt permission to detect outlier setting (CYCLE < THRESH) to PWM1																
	23	PWM0_INVALID_VALUE								RW	0x0				Interrupt permission to detect outlier setting (CYCLE < THRESH) to PWM0																
	22	D1_R3_CH_OVER_RUN								RW	0x0																				
	21	D0_R3_CH_OVER_RUN								RW	0x0																				
	20	N7_R1_C_OVER_RUN								RW	0x0																				
	19	N6_R1_C_OVER_RUN								RW	0x0																				
	18	N5_R1_C_OVER_RUN								RW	0x0																				
17	N4_R1_C_OVER_RUN								RW	0x0																					
16	N3_R1_C_OVER_RUN								RW	0x0																					
15	N2_R1_C_OVER_RUN								RW	0x0																					
14	N1_R1_C_OVER_RUN								RW	0x0																					
13	N0_R1_C_OVER_RUN								RW	0x0																					
12	D1_R2_C_OVER_RUN								RW	0x0																					

11	D1_R1_C_OVER_RUN	RW	0x0	
10	D0_R2_C_OVER_RUN	RW	0x0	
9	D0_R1_C_OVER_RUN	RW	0x0	
8..7	Reserved	RO	0x0	Reserved
6	ADCIF_READ_ERR	RW	0x0	
5	HPADC1_OVER_RUN	RW	0x0	
4	HPADC0_OVER_RUN	RW	0x0	
3	LPADC_OVER_RUN	RW	0x0	
2	LPADC_OVER_RUN3	RW	0x0	
1	LPADC_OVER_RUN2	RW	0x0	
0	LPADC_OVER_RUN1	RW	0x0	Interrupt permission of overrun error (write occurrence at FIFO Full) for LPADC

3.9.12.3.133 {0x5428} INT_CLEAR_ERR_0 Details

Table SCU (Sensor Control Unit)-241

Local Address: 0x5428																				Register Type: WO (write only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								Reserved								Reserved								Reserved											
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3.9.12.3.134 {0x542C} INT_RAW_STT_ERR_0 Details

Table SCU (Sensor Control Unit)-242

Local Address: 0x542C																Register Type: RO (read only)															
																Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	PWM7_INVALID_VALUE	PWM6_INVALID_VALUE	PWM5_INVALID_VALUE	PWM4_INVALID_VALUE	PWM3_INVALID_VALUE	PWM2_INVALID_VALUE	PWM1_INVALID_VALUE	PWM0_INVALID_VALUE	D1_R3_CH_OVER_RUN	D0_R3_CH_OVER_RUN	N7_R1_C_OVER_RUN	N6_R1_C_OVER_RUN	N5_R1_C_OVER_RUN	N4_R1_C_OVER_RUN	N3_R1_C_OVER_RUN	N2_R1_C_OVER_RUN	N1_R1_C_OVER_RUN	N0_R1_C_OVER_RUN	D1_R2_C_OVER_RUN	D1_R1_C_OVER_RUN	D0_R2_C_OVER_RUN	D0_R1_C_OVER_RUN	Reserved	ADCIF_READ_ERR	HPADC1_OVER_RUN	HPADC0_OVER_RUN	LPADC_OVER_RUN	LPADC_OVER_RUN3	LPADC_OVER_RUN2	LPADC_OVER_RUN1	
	Bits	Name							Type	Reset Value		Description																			
31	Reserved							RO	0x0		Reserved																				
30	PWM7_INVALID_VALUE							RO	0x0																						
29	PWM6_INVALID_VALUE							RO	0x0																						
28	PWM5_INVALID_VALUE							RO	0x0																						
27	PWM4_INVALID_VALUE							RO	0x0																						
26	PWM3_INVALID_VALUE							RO	0x0																						
25	PWM2_INVALID_VALUE							RO	0x0																						
24	PWM1_INVALID_VALUE							RO	0x0																						
23	PWM0_INVALID_VALUE							RO	0x0																						
22	D1_R3_CH_OVER_RUN							RO	0x0																						
21	D0_R3_CH_OVER_RUN							RO	0x0																						
20	N7_R1_C_OVER_RUN							RO	0x0																						
19	N6_R1_C_OVER_RUN							RO	0x0																						
18	N5_R1_C_OVER_RUN							RO	0x0																						
17	N4_R1_C_OVER_RUN							RO	0x0																						
16	N3_R1_C_OVER_RUN							RO	0x0																						
15	N2_R1_C_OVER_RUN							RO	0x0																						
14	N1_R1_C_OVER_RUN							RO	0x0																						
13	N0_R1_C_OVER_RUN							RO	0x0																						
12	D1_R2_C_OVER_RUN							RO	0x0																						
11	D1_R1_C_OVER_RUN							RO	0x0																						
10	D0_R2_C_OVER_RUN							RO	0x0																						

9	D0_R1_C_OVER_RUN	RO	0x0	
8..7	Reserved	RO	0x0	Reserved
6	ADCIF_READ_ERR	RO	0x0	
5	HPADC1_OVER_RUN	RO	0x0	
4	HPADC0_OVER_RUN	RO	0x0	
3	LPADC_OVER_RUN	RO	0x0	
2	LPADC_OVER_RUN3	RO	0x0	
1	LPADC_OVER_RUN2	RO	0x0	
0	LPADC_OVER_RUN1	RO	0x0	

3.9.12.3.135 {0x5430} INT_MASKED_STT_ERR_0 Details

Table SCU (Sensor Control Unit)-243

Local Address: 0x5430																Register Type: RO (read only)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PWM7_INVALID_VALUE	PWM6_INVALID_VALUE	PWM5_INVALID_VALUE	PWM4_INVALID_VALUE	PWM3_INVALID_VALUE	PWM2_INVALID_VALUE	PWM1_INVALID_VALUE	PWM0_INVALID_VALUE	D1_R3_CH_OVER_RUN	D0_R3_CH_OVER_RUN	N7_R1_C_OVER_RUN	N6_R1_C_OVER_RUN	N5_R1_C_OVER_RUN	N4_R1_C_OVER_RUN	N3_R1_C_OVER_RUN	N2_R1_C_OVER_RUN	N1_R1_C_OVER_RUN	N0_R1_C_OVER_RUN	D1_R2_C_OVER_RUN	D1_R1_C_OVER_RUN	D0_R2_C_OVER_RUN	D0_R1_C_OVER_RUN	Reserved	ADCIF_READ_ERR	HPADC1_OVER_RUN	HPADC0_OVER_RUN	LPADC_OVER_RUN	LPADC_OVER_RUN3	LPADC_OVER_RUN2	LPADC_OVER_RUN1	
Bits	Name								Type	Reset Value		Description																			
31	Reserved								RO	0x0		Reserved																			
30	PWM7_INVALID_VALUE								RO	0x0																					
29	PWM6_INVALID_VALUE								RO	0x0																					
28	PWM5_INVALID_VALUE								RO	0x0																					
27	PWM4_INVALID_VALUE								RO	0x0																					
26	PWM3_INVALID_VALUE								RO	0x0																					
25	PWM2_INVALID_VALUE								RO	0x0																					
24	PWM1_INVALID_VALUE								RO	0x0																					
23	PWM0_INVALID_VALUE								RO	0x0																					
22	D1_R3_CH_OVER_RUN								RO	0x0																					
21	D0_R3_CH_OVER_RUN								RO	0x0																					
20	N7_R1_C_OVER_RUN								RO	0x0																					
19	N6_R1_C_OVER_RUN								RO	0x0																					
18	N5_R1_C_OVER_RUN								RO	0x0																					
17	N4_R1_C_OVER_RUN								RO	0x0																					
16	N3_R1_C_OVER_RUN								RO	0x0																					
15	N2_R1_C_OVER_RUN								RO	0x0																					
14	N1_R1_C_OVER_RUN								RO	0x0																					
13	N0_R1_C_OVER_RUN								RO	0x0																					
12	D1_R2_C_OVER_RUN								RO	0x0																					
11	D1_R1_C_OVER_RUN								RO	0x0																					
10	D0_R2_C_OVER_RUN								RO	0x0																					

9	D0_R1_C_OVER_RUN	RO	0x0	
8..7	Reserved	RO	0x0	Reserved
6	ADCIF_READ_ERR	RO	0x0	
5	HPADC1_OVER_RUN	RO	0x0	
4	HPADC0_OVER_RUN	RO	0x0	
3	LPADC_OVER_RUN	RO	0x0	
2	LPADC_OVER_RUN3	RO	0x0	
1	LPADC_OVER_RUN2	RO	0x0	
0	LPADC_OVER_RUN1	RO	0x0	

3.9.12.3.136 {0x5440} INT_ENABLE_ERR_1 Details

Table SCU (Sensor Control Unit)-244

Local Address: 0x5440																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								D1_R3_CH_UNDER_RUN	D0_R3_CH_UNDER_RUN	N7_R1_C_UNDER_RUN	N6_R1_C_UNDER_RUN	N5_R1_C_UNDER_RUN	N4_R1_C_UNDER_RUN	N3_R1_C_UNDER_RUN	N2_R1_C_UNDER_RUN	N1_R1_C_UNDER_RUN	N0_R1_C_UNDER_RUN	D1_R2_C_UNDER_RUN	D1_R1_C_UNDER_RUN	D0_R2_C_UNDER_RUN	D0_R1_C_UNDER_RUN	Reserved				HPADC1_UNDER_RUN	HPADC0_UNDER_RUN	LPADC_UNDER_RUN	LPADC_UNDER_RUN3	LPADC_UNDER_RUN2	LPADC_UNDER_RUN1
Bits	Name							Type	Reset Value		Description																				
31..23	Reserved							RO	0x000		Reserved																				
22	D1_R3_CH_UNDER_RUN							RW	0x0																						
21	D0_R3_CH_UNDER_RUN							RW	0x0																						
20	N7_R1_C_UNDER_RUN							RW	0x0																						
19	N6_R1_C_UNDER_RUN							RW	0x0																						
18	N5_R1_C_UNDER_RUN							RW	0x0																						
17	N4_R1_C_UNDER_RUN							RW	0x0																						
16	N3_R1_C_UNDER_RUN							RW	0x0																						
15	N2_R1_C_UNDER_RUN							RW	0x0																						
14	N1_R1_C_UNDER_RUN							RW	0x0																						
13	N0_R1_C_UNDER_RUN							RW	0x0																						
12	D1_R2_C_UNDER_RUN							RW	0x0																						
11	D1_R1_C_UNDER_RUN							RW	0x0																						
10	D0_R2_C_UNDER_RUN							RW	0x0																						
9	D0_R1_C_UNDER_RUN							RW	0x0																						
8..6	Reserved							RO	0x0		Reserved																				
5	HPADC1_UNDER_RUN							RW	0x0																						
4	HPADC0_UNDER_RUN							RW	0x0																						
3	LPADC_UNDER_RUN							RW	0x0																						
2	LPADC_UNDER_RUN3							RW	0x0																						
1	LPADC_UNDER_RUN2							RW	0x0																						
0	LPADC_UNDER_RUN1							RW	0x0																						

3.9.12.3.137 {0x5444} INT_DISABLE_ERR_1 Details

Table SCU (Sensor Control Unit)-245

Local Address: 0x5444																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								D1_R3_CH_UNDER_RUN	D0_R3_CH_UNDER_RUN	N7_R1_C_UNDER_RUN	N6_R1_C_UNDER_RUN	N5_R1_C_UNDER_RUN	N4_R1_C_UNDER_RUN	N3_R1_C_UNDER_RUN	N2_R1_C_UNDER_RUN	N1_R1_C_UNDER_RUN	N0_R1_C_UNDER_RUN	D1_R2_C_UNDER_RUN	D1_R1_C_UNDER_RUN	D0_R2_C_UNDER_RUN	D0_R1_C_UNDER_RUN	Reserved				HPADC1_UNDER_RUN	HPADC0_UNDER_RUN	LPADC_UNDER_RUN	LPADC_UNDER_RUN3	LPADC_UNDER_RUN2	LPADC_UNDER_RUN1
Bits	Name							Type	Reset Value		Description																				
31..23	Reserved							RO	0x000		Reserved																				
22	D1_R3_CH_UNDER_RUN							RW	0x0																						
21	D0_R3_CH_UNDER_RUN							RW	0x0																						
20	N7_R1_C_UNDER_RUN							RW	0x0																						
19	N6_R1_C_UNDER_RUN							RW	0x0																						
18	N5_R1_C_UNDER_RUN							RW	0x0																						
17	N4_R1_C_UNDER_RUN							RW	0x0																						
16	N3_R1_C_UNDER_RUN							RW	0x0																						
15	N2_R1_C_UNDER_RUN							RW	0x0																						
14	N1_R1_C_UNDER_RUN							RW	0x0																						
13	N0_R1_C_UNDER_RUN							RW	0x0																						
12	D1_R2_C_UNDER_RUN							RW	0x0																						
11	D1_R1_C_UNDER_RUN							RW	0x0																						
10	D0_R2_C_UNDER_RUN							RW	0x0																						
9	D0_R1_C_UNDER_RUN							RW	0x0																						
8..6	Reserved							RO	0x0		Reserved																				
5	HPADC1_UNDER_RUN							RW	0x0																						
4	HPADC0_UNDER_RUN							RW	0x0																						
3	LPADC_UNDER_RUN							RW	0x0																						
2	LPADC_UNDER_RUN3							RW	0x0																						
1	LPADC_UNDER_RUN2							RW	0x0																						
0	LPADC_UNDER_RUN1							RW	0x0																						

3.9.12.3.138 {0x5448} INT_CLEAR_ERR_1 Details

Table SCU (Sensor Control Unit)-246

Local Address: 0x5448																							Register Type: WO (write only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Reserved																											HPADC1_UNDER_RUN	HPADC0_UNDER_RUN	LPADC_UNDER_RUN	LPADC_UNDER_RUN3	LPADC_UNDER_RUN2	LPADC_UNDER_RUN1				
Bits	Name							Type	Reset Value							Description																				
31..6	Reserved							WO	0x00000000							Reserved																				
5	HPADC1_UNDER_RUN							WO	0x0																											
4	HPADC0_UNDER_RUN							WO	0x0																											
3	LPADC_UNDER_RUN							WO	0x0																											
2	LPADC_UNDER_RUN3							WO	0x0																											
1	LPADC_UNDER_RUN2							WO	0x0																											
0	LPADC_UNDER_RUN1							WO	0x0																											

3.9.12.3.139 {0x544C} INT_RAW_STT_ERR_1 Details

Table SCU (Sensor Control Unit)-247

Local Address: 0x544C																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								D1_R3_CH_UNDER_RUN	D0_R3_CH_UNDER_RUN	N7_R1_C_UNDER_RUN	N6_R1_C_UNDER_RUN	N5_R1_C_UNDER_RUN	N4_R1_C_UNDER_RUN	N3_R1_C_UNDER_RUN	N2_R1_C_UNDER_RUN	N1_R1_C_UNDER_RUN	N0_R1_C_UNDER_RUN	D1_R2_C_UNDER_RUN	D1_R1_C_UNDER_RUN	D0_R2_C_UNDER_RUN	D0_R1_C_UNDER_RUN	Reserved				HPADC1_UNDER_RUN	HPADC0_UNDER_RUN	LPADC_UNDER_RUN	LPADC_UNDER_RUN3	LPADC_UNDER_RUN2	LPADC_UNDER_RUN1
Bits	Name							Type	Reset Value				Description																		
31..23	Reserved							RO	0x000				Reserved																		
22	D1_R3_CH_UNDER_RUN							RO	0x0																						
21	D0_R3_CH_UNDER_RUN							RO	0x0																						
20	N7_R1_C_UNDER_RUN							RO	0x0																						
19	N6_R1_C_UNDER_RUN							RO	0x0																						
18	N5_R1_C_UNDER_RUN							RO	0x0																						
17	N4_R1_C_UNDER_RUN							RO	0x0																						
16	N3_R1_C_UNDER_RUN							RO	0x0																						
15	N2_R1_C_UNDER_RUN							RO	0x0																						
14	N1_R1_C_UNDER_RUN							RO	0x0																						
13	N0_R1_C_UNDER_RUN							RO	0x0																						
12	D1_R2_C_UNDER_RUN							RO	0x0																						
11	D1_R1_C_UNDER_RUN							RO	0x0																						
10	D0_R2_C_UNDER_RUN							RO	0x0																						
9	D0_R1_C_UNDER_RUN							RO	0x0																						
8..6	Reserved							RO	0x0				Reserved																		
5	HPADC1_UNDER_RUN							RO	0x0																						
4	HPADC0_UNDER_RUN							RO	0x0																						
3	LPADC_UNDER_RUN							RO	0x0																						
2	LPADC_UNDER_RUN3							RO	0x0																						
1	LPADC_UNDER_RUN2							RO	0x0																						
0	LPADC_UNDER_RUN1							RO	0x0																						

3.9.12.3.140 {0x5450} INT_MASKED_STT_ERR_1 Details

Table SCU (Sensor Control Unit)-248

Local Address: 0x5450																Register Type: RO (read only) Reset Value: 0x00000000																										
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																		
Reserved								D1_R3_CH_UNDER_RUN	D0_R3_CH_UNDER_RUN	N7_R1_C_UNDER_RUN	N6_R1_C_UNDER_RUN	N5_R1_C_UNDER_RUN	N4_R1_C_UNDER_RUN	N3_R1_C_UNDER_RUN	N2_R1_C_UNDER_RUN	N1_R1_C_UNDER_RUN	N0_R1_C_UNDER_RUN	D1_R2_C_UNDER_RUN	D1_R1_C_UNDER_RUN	D0_R2_C_UNDER_RUN	D0_R1_C_UNDER_RUN	Reserved				HPADC1_UNDER_RUN	HPADC0_UNDER_RUN	LPADC_UNDER_RUN	LPADC_UNDER_RUN3	LPADC_UNDER_RUN2	LPADC_UNDER_RUN1											
								Bits	Name							Type	Reset Value									Description																
								31..23	Reserved							RO	0x000									Reserved																
								22	D1_R3_CH_UNDER_RUN							RO	0x0																									
								21	D0_R3_CH_UNDER_RUN							RO	0x0																									
								20	N7_R1_C_UNDER_RUN							RO	0x0																									
								19	N6_R1_C_UNDER_RUN							RO	0x0																									
								18	N5_R1_C_UNDER_RUN							RO	0x0																									
								17	N4_R1_C_UNDER_RUN							RO	0x0																									
								16	N3_R1_C_UNDER_RUN							RO	0x0																									
								15	N2_R1_C_UNDER_RUN							RO	0x0																									
								14	N1_R1_C_UNDER_RUN							RO	0x0																									
								13	N0_R1_C_UNDER_RUN							RO	0x0																									
								12	D1_R2_C_UNDER_RUN							RO	0x0																									
								11	D1_R1_C_UNDER_RUN							RO	0x0																									
								10	D0_R2_C_UNDER_RUN							RO	0x0																									
9	D0_R1_C_UNDER_RUN							RO	0x0																																	
8..6	Reserved							RO	0x0							Reserved																										
5	HPADC1_UNDER_RUN							RO	0x0																																	
4	HPADC0_UNDER_RUN							RO	0x0																																	
3	LPADC_UNDER_RUN							RO	0x0																																	
2	LPADC_UNDER_RUN3							RO	0x0																																	
1	LPADC_UNDER_RUN2							RO	0x0																																	
0	LPADC_UNDER_RUN1							RO	0x0																																	

3.9.12.3.141 {0x5460} INT_ENABLE_ERR_2 Details

Table SCU (Sensor Control Unit)-249

Local Address: 0x5460																Register Type: RW (read/write) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								EXE_ERR9	EXE_ERR8	EXE_ERR7	EXE_ERR6	EXE_ERR5	EXE_ERR4	EXE_ERR3	EXE_ERR2	EXE_ERR1	EXE_ERR0	Reserved								REQ_BEFORE_FINISH9	REQ_BEFORE_FINISH8	REQ_BEFORE_FINISH7	REQ_BEFORE_FINISH6	REQ_BEFORE_FINISH5	REQ_BEFORE_FINISH4	REQ_BEFORE_FINISH3	REQ_BEFORE_FINISH2	REQ_BEFORE_FINISH1	REQ_BEFORE_FINISH0
Bits	Name							Type		Reset Value		Description																							
31..26	Reserved							RO		0x00		Reserved																							
25	EXE_ERR9							RW		0x0																									
24	EXE_ERR8							RW		0x0																									
23	EXE_ERR7							RW		0x0																									
22	EXE_ERR6							RW		0x0																									
21	EXE_ERR5							RW		0x0																									
20	EXE_ERR4							RW		0x0																									
19	EXE_ERR3							RW		0x0																									
18	EXE_ERR2							RW		0x0																									
17	EXE_ERR1							RW		0x0																									
16	EXE_ERR0							RW		0x0		Permission of interrupt for not completing the sequencer’s process successfully when executing Sequencer 0																							
15..10	Reserved							RO		0x00		Reserved																							
9	REQ_BEFORE_FINISH9							RW		0x0																									
8	REQ_BEFORE_FINISH8							RW		0x0																									
7	REQ_BEFORE_FINISH7							RW		0x0																									
6	REQ_BEFORE_FINISH6							RW		0x0																									
5	REQ_BEFORE_FINISH5							RW		0x0																									
4	REQ_BEFORE_FINISH4							RW		0x0																									
3	REQ_BEFORE_FINISH3							RW		0x0																									
2	REQ_BEFORE_FINISH2							RW		0x0																									

1	REQ_BEFORE_FINISH1	RW	0x0	
0	REQ_BEFORE_FINISH0	RW	0x0	Permission of interrupt for requesting the next operation before completion (Sequencer 0)

3.9.12.3.142 {0x5464} INT_DISABLE_ERR_2 Details

Table SCU (Sensor Control Unit)-250

Local Address: 0x5464																Register Type: RW (read/write) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								EXE_ERR9	EXE_ERR8	EXE_ERR7	EXE_ERR6	EXE_ERR5	EXE_ERR4	EXE_ERR3	EXE_ERR2	EXE_ERR1	EXE_ERR0	Reserved								REQ_BEFORE_FINISH9	REQ_BEFORE_FINISH8	REQ_BEFORE_FINISH7	REQ_BEFORE_FINISH6	REQ_BEFORE_FINISH5	REQ_BEFORE_FINISH4	REQ_BEFORE_FINISH3	REQ_BEFORE_FINISH2	REQ_BEFORE_FINISH1	REQ_BEFORE_FINISH0
Bits	Name							Type	Reset Value		Description																								
31..26	Reserved							RO	0x00		Reserved																								
25	EXE_ERR9							RW	0x0																										
24	EXE_ERR8							RW	0x0																										
23	EXE_ERR7							RW	0x0																										
22	EXE_ERR6							RW	0x0																										
21	EXE_ERR5							RW	0x0																										
20	EXE_ERR4							RW	0x0																										
19	EXE_ERR3							RW	0x0																										
18	EXE_ERR2							RW	0x0																										
17	EXE_ERR1							RW	0x0																										
16	EXE_ERR0							RW	0x0		Permission of interrupt for not completing the sequencer’s process successfully when executing Sequencer 0																								
15..10	Reserved							RO	0x00		Reserved																								
9	REQ_BEFORE_FINISH9							RW	0x0																										
8	REQ_BEFORE_FINISH8							RW	0x0																										
7	REQ_BEFORE_FINISH7							RW	0x0																										
6	REQ_BEFORE_FINISH6							RW	0x0																										
5	REQ_BEFORE_FINISH5							RW	0x0																										
4	REQ_BEFORE_FINISH4							RW	0x0																										
3	REQ_BEFORE_FINISH3							RW	0x0																										
2	REQ_BEFORE_FINISH2							RW	0x0																										

1	REQ_BEFORE_FINISH1	RW	0x0	
0	REQ_BEFORE_FINISH0	RW	0x0	Permission of interrupt for requesting the next operation before completion (Sequencer 0)

3.9.12.3.143 {0x5468} INT_CLEAR_ERR_2 Details

Table SCU (Sensor Control Unit)-251

Local Address: 0x5468																Register Type: WO (write only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								EXE_ERR9	EXE_ERR8	EXE_ERR7	EXE_ERR6	EXE_ERR5	EXE_ERR4	EXE_ERR3	EXE_ERR2	EXE_ERR1	EXE_ERR0	Reserved								REQ_BEFORE_FINISH9	REQ_BEFORE_FINISH8	REQ_BEFORE_FINISH7	REQ_BEFORE_FINISH6	REQ_BEFORE_FINISH5	REQ_BEFORE_FINISH4	REQ_BEFORE_FINISH3	REQ_BEFORE_FINISH2	REQ_BEFORE_FINISH1	REQ_BEFORE_FINISH0
Bits	Name							Type	Reset Value							Description																			
31..26	Reserved							WO	0x00							Reserved																			
25	EXE_ERR9							WO	0x0																										
24	EXE_ERR8							WO	0x0																										
23	EXE_ERR7							WO	0x0																										
22	EXE_ERR6							WO	0x0																										
21	EXE_ERR5							WO	0x0																										
20	EXE_ERR4							WO	0x0																										
19	EXE_ERR3							WO	0x0																										
18	EXE_ERR2							WO	0x0																										
17	EXE_ERR1							WO	0x0																										
16	EXE_ERR0							WO	0x0							Clear of interrupt for not completing the sequencer’s process successfully when executing Sequencer 0																			
15..10	Reserved							WO	0x00							Reserved																			
9	REQ_BEFORE_FINISH9							WO	0x0																										
8	REQ_BEFORE_FINISH8							WO	0x0																										
7	REQ_BEFORE_FINISH7							WO	0x0																										
6	REQ_BEFORE_FINISH6							WO	0x0																										
5	REQ_BEFORE_FINISH5							WO	0x0																										
4	REQ_BEFORE_FINISH4							WO	0x0																										
3	REQ_BEFORE_FINISH3							WO	0x0																										
2	REQ_BEFORE_FINISH2							WO	0x0																										

1	REQ_BEFORE_FINISH1	WO	0x0	
0	REQ_BEFORE_FINISH0	WO	0x0	Clear of interrupt for requesting the next operation before completion (Sequencer 0)

3.9.12.3.144 {0x546C} INT_RAW_STT_ERR_2 Details

Table SCU (Sensor Control Unit)-252

Local Address: 0x546C																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								EXE_ERR9	EXE_ERR8	EXE_ERR7	EXE_ERR6	EXE_ERR5	EXE_ERR4	EXE_ERR3	EXE_ERR2	EXE_ERR1	EXE_ERR0	Reserved								REQ_BEFORE_FINISH9	REQ_BEFORE_FINISH8	REQ_BEFORE_FINISH7	REQ_BEFORE_FINISH6	REQ_BEFORE_FINISH5	REQ_BEFORE_FINISH4	REQ_BEFORE_FINISH3	REQ_BEFORE_FINISH2	REQ_BEFORE_FINISH1	REQ_BEFORE_FINISH0
Bits	Name							Type	Reset Value							Description																			
31..26	Reserved							RO	0x00							Reserved																			
25	EXE_ERR9							RO	0x0																										
24	EXE_ERR8							RO	0x0																										
23	EXE_ERR7							RO	0x0																										
22	EXE_ERR6							RO	0x0																										
21	EXE_ERR5							RO	0x0																										
20	EXE_ERR4							RO	0x0																										
19	EXE_ERR3							RO	0x0																										
18	EXE_ERR2							RO	0x0																										
17	EXE_ERR1							RO	0x0																										
16	EXE_ERR0							RO	0x0							Status of interrupt for not completing the sequencer’s process successfully when executing Sequencer 0 (before masking)																			
15..10	Reserved							RO	0x00							Reserved																			
9	REQ_BEFORE_FINISH9							RO	0x0																										
8	REQ_BEFORE_FINISH8							RO	0x0																										
7	REQ_BEFORE_FINISH7							RO	0x0																										
6	REQ_BEFORE_FINISH6							RO	0x0																										
5	REQ_BEFORE_FINISH5							RO	0x0																										
4	REQ_BEFORE_FINISH4							RO	0x0																										
3	REQ_BEFORE_FINISH3							RO	0x0																										
2	REQ_BEFORE_FINISH2							RO	0x0																										

1	REQ_BEFORE_FINISH1	RO	0x0	
0	REQ_BEFORE_FINISH0	RO	0x0	Interrupt status for requesting the next operation before completion (Sequencer 0, before masking)

3.9.12.3.145 {0x5470} INT_MASKED_STT_ERR_2 Details

Table SCU (Sensor Control Unit)-253

Local Address: 0x5470																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved								EXE_ERR9	EXE_ERR8	EXE_ERR7	EXE_ERR6	EXE_ERR5	EXE_ERR4	EXE_ERR3	EXE_ERR2	EXE_ERR1	EXE_ERR0	Reserved								REQ_BEFORE_FINISH9	REQ_BEFORE_FINISH8	REQ_BEFORE_FINISH7	REQ_BEFORE_FINISH6	REQ_BEFORE_FINISH5	REQ_BEFORE_FINISH4	REQ_BEFORE_FINISH3	REQ_BEFORE_FINISH2	REQ_BEFORE_FINISH1	REQ_BEFORE_FINISH0
Bits	Name							Type	Reset Value							Description																			
31..26	Reserved							RO	0x00							Reserved																			
25	EXE_ERR9							RO	0x0																										
24	EXE_ERR8							RO	0x0																										
23	EXE_ERR7							RO	0x0																										
22	EXE_ERR6							RO	0x0																										
21	EXE_ERR5							RO	0x0																										
20	EXE_ERR4							RO	0x0																										
19	EXE_ERR3							RO	0x0																										
18	EXE_ERR2							RO	0x0																										
17	EXE_ERR1							RO	0x0																										
16	EXE_ERR0							RO	0x0							Status of interrupt for not completing the sequencer’s process successfully when executing Sequencer 0 (after masking)																			
15..10	Reserved							RO	0x00							Reserved																			
9	REQ_BEFORE_FINISH9							RO	0x0																										
8	REQ_BEFORE_FINISH8							RO	0x0																										
7	REQ_BEFORE_FINISH7							RO	0x0																										
6	REQ_BEFORE_FINISH6							RO	0x0																										
5	REQ_BEFORE_FINISH5							RO	0x0																										
4	REQ_BEFORE_FINISH4							RO	0x0																										
3	REQ_BEFORE_FINISH3							RO	0x0																										
2	REQ_BEFORE_FINISH2							RO	0x0																										

1	REQ_BEFORE_FINISH1	RO	0x0	
0	REQ_BEFORE_FINISH0	RO	0x0	Interrupt status for requesting the next operation before completion (Sequencer 0, after masking)

3.9.12.3.146 {0x5500} RAM_TEST Details

Table SCU (Sensor Control Unit)-254

Local Address: 0x5500																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						ICGOVERRIDE	WM	RM	EN_STANDBY	EN_IG					
Bits	Name				Type	Reset Value				Description																					
31..9	Reserved				RO	0x000000				Reserved																					
8..7	ICGOVERRIDE				RW	0x0																									
6..5	WM				RW	0x0				write timing margin common to all RAMs in the SCU																					
4..2	RM				RW	0x0				read timing margin common to all RAMs in the SCU																					
1	EN_STANDBY				RW	0x0				standby enable common to all RAMs in the SCU																					
0	EN_IG				RW	0x0				InputGate enable common to all RAMs in the SCU																					

3.9.12.3.147 {0x5510} SCU_POWER Details

Clock Control under Internal Sequencer's control

0: CK_SCU 1: CK_SCU_SPI 2: CK_SCU_I2C0 3: CK_SCU_I2C1

Table SCU (Sensor Control Unit)-255

Local Address: 0x5510																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										CLK_EN					
Bits		Name				Type	Reset Value				Description																				
31..4		Reserved				RO	0x00000000				Reserved																				
3..0		CLK_EN				RO	0x0																								

3.9.12.3.148 {0x5520} INT_ENABLE_MAIN_AD Details

Table SCU (Sensor Control Unit)-256

Local Address: 0x5520																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												LPADC_ALMOST_FULL3	LPADC_ALMOST_FULL2	LPADC_ALMOST_FULL1	
Bits	Name							Type	Reset Value							Description															
31..3	Reserved							RO	0x00000000							Reserved															
2	LPADC_ALMOST_FULL3							RW	0x0																						
1	LPADC_ALMOST_FULL2							RW	0x0																						
0	LPADC_ALMOST_FULL1							RW	0x0							Interrupt permission for the SPI or Math Function Event 0. The interrupt is permitted by writing “1”. Writing “0” cannot prohibit the interrupt.															

3.9.12.3.149 {0x5524} INT_DISABLE_MAIN_AD Details

Table SCU (Sensor Control Unit)-257

Local Address: 0x5524																								Register Type: RW (read/write)											
																								Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																												LPADC_ALMOST_FULL3	LPADC_ALMOST_FULL2	LPADC_ALMOST_FULL1					
Bits	Name							Type	Reset Value							Description																			
31..3	Reserved							RO	0x00000000							Reserved																			
2	LPADC_ALMOST_FULL3							RW	0x0																										
1	LPADC_ALMOST_FULL2							RW	0x0																										
0	LPADC_ALMOST_FULL1							RW	0x0							Interrupt prohibition for the SPI. The interrupt is prohibited by writing “1”. Writing “0” cannot permit the interrupt.																			

3.9.12.3.150 {0x5528} INT_CLEAR_MAIN_AD Details

Table SCU (Sensor Control Unit)-258

Local Address: 0x5528																						Register Type: WO (write only)									
																						Reset Value: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												LPADC_ALMOST_FULL3			
																												LPADC_ALMOST_FULL2			
																												LPADC_ALMOST_FULL1			
Bits	Name							Type	Reset Value							Description															
31..3	Reserved							WO	0x00000000							Reserved															
2	LPADC_ALMOST_FULL3							WO	0x0																						
1	LPADC_ALMOST_FULL2							WO	0x0																						
0	LPADC_ALMOST_FULL1							WO	0x0							Interrupt clear of Math Function Event 0. When the SPI is selected, the interrupt is cleared by the register of the SPI Slave.															

3.9.12.3.151 {0x552C} LEVEL_SEL_MAIN_AD Details

Table SCU (Sensor Control Unit)-259

Local Address: 0x552C																						Register Type: RW (read/write)									
																						Reset Value: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												LPADC_ALMOST_FULL3	LPADC_ALMOST_FULL2	LPADC_ALMOST_FULL1	
Bits	Name							Type	Reset Value							Description															
31..3	Reserved							RO	0x00000000							Reserved															
2	LPADC_ALMOST_FULL3							RW	0x0																						
1	LPADC_ALMOST_FULL2							RW	0x0																						
0	LPADC_ALMOST_FULL1							RW	0x0																						

3.9.12.3.152 {0x5530} INT_RAW_STT_MAIN_AD Details

Table SCU (Sensor Control Unit)-260

Local Address: 0x5530																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												LPADC_ALMOST_FULL3	LPADC_ALMOST_FULL2	LPADC_ALMOST_FULL1	
Bits	Name							Type	Reset Value							Description															
31..3	Reserved							RO	0x00000000							Reserved															
2	LPADC_ALMOST_FULL3							RO	0x0																						
1	LPADC_ALMOST_FULL2							RO	0x0																						
0	LPADC_ALMOST_FULL1							RO	0x0							Interrupt status of the SPI or Math Function Event 0 before masking															

3.9.12.3.153 {0x5534} INT_MASKED_STT_MAIN_AD Details

Table SCU (Sensor Control Unit)-261

Local Address: 0x5534																						Register Type: RO (read only) Reset Value: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												LPADC_ALMOST_FULL3	LPADC_ALMOST_FULL2	LPADC_ALMOST_FULL1	
Bits	Name							Type	Reset Value							Description															
31..3	Reserved							RO	0x00000000							Reserved															
2	LPADC_ALMOST_FULL3							RO	0x0																						
1	LPADC_ALMOST_FULL2							RO	0x0																						
0	LPADC_ALMOST_FULL1							RO	0x0							Interrupt status of the SPI or Math Function Event 0 after masking															

3.9.12.3.154 {0x5600} PWM0_PARAM Details

Table SCU (Sensor Control Unit)-262

Local Address: 0x5600																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM0_THRESH																PWM0_CYCLE															
Bits		Name				Type		Reset Value				Description																			
31..16		PWM0_THRESH				RW		0x0000				Sets the duty of PWM0 output																			
15..0		PWM0_CYCLE				RW		0x0000				Sets the cycle of PWM0 output																			

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.155 {0x5604} PWM0_EN Details

100: LPADC0 101: LPADC1 110: LPADC2 111: LPADC3

Table SCU (Sensor Control Unit)-263

Local Address: 0x5604																		Register Type: RW (read/write) Reset Value: 0x00000000														
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0								
Reserved																		PWM_SELL0								PWM0_EN						
Bits		Name						Type	Reset Value						Description																	
31..8		Reserved						RO	0x000000						Reserved																	
7..1		PWM_SELL0						RW	0x00						[3:1]: Selects a target AD which the PWM0 is synchronized with 0x0: is not synchronized with ADs 0x1: is synchronized with HPADC0 0x2: is synchronized with HPADC1 0x3: is synchronized with LPADC in operation 0x4: is synchronized with LPADC0 0x5: is synchronized with LPADC1 0x6: is synchronized with LPADC2 0x7: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM0 is synchronized with																	
0		PWM0_EN						RW	0x0						Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”.																	

3.9.12.3.156 {0x5608} PWM0_UPDATE Details

Table SCU (Sensor Control Unit)-264

Local Address: 0x5608																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM0_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM0_UPDATE				WO	0x0				Reflects a set value in PWM0’s operation by writing “1” on this register.																				

3.9.12.3.157 {0x560C} PWM1_PARAM Details

Table SCU (Sensor Control Unit)-265

Local Address: 0x560C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM1_THRESH																PWM1_CYCLE															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM1_THRESH				RW	0x0000				Sets the duty of PWM1 output																				
15..0		PWM1_CYCLE				RW	0x0000				Sets the output cycle of PWM1																				

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.158 {0x5610} PWM1_EN Details

Table SCU (Sensor Control Unit)-266

Local Address: 0x5610																						Register Type: RW (read/write)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved																						PWM_SELL1										PWM1_EN
Bits		Name				Type	Reset Value				Description																					
31..8		Reserved				RO	0x000000				Reserved																					
7..1		PWM_SELL1				RW	0x00				[3:1]: Selects a target AD which the PWM1 is synchronized with 0x0: is not synchronized with ADs 0x1: is synchronized with HPADC0 0x2: is synchronized with HPADC1 0x3: is synchronized with LPADC in operation 0x4: is synchronized with LPADC0 0x5: is synchronized with LPADC1 0x6: is synchronized with LPADC2 0x7: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM1 is synchronized with																					
0		PWM1_EN				RW	0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”.																					

3.9.12.3.159 {0x5614} PWM1_UPDATE Details

Table SCU (Sensor Control Unit)-267

Local Address: 0x5614																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM1_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM1_UPDATE				WO	0x0				Reflects a set value in PWM1’s operation by writing “1” on this register.																				

3.9.12.3.160 {0x5618} PWM2_PARAM Details

Table SCU (Sensor Control Unit)-268

Local Address: 0x5618																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM2_THRESH																PWM2_CYCLE															
Bits				Name				Type		Reset Value				Description																	
31..16				PWM2_THRESH				RW		0x0000				Sets the duty of PWM2 output																	
15..0				PWM2_CYCLE				RW		0x0000				Sets the output cycle of PWM2																	

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.161 {0x561C} PWM2_EN Details

Table SCU (Sensor Control Unit)-269

Local Address: 0x561C																				Register Type: RW (read/write)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																							PWM_SELL2						PWM2_EN		
Bits		Name					Type	Reset Value					Description																		
31..8		Reserved					RO	0x000000					Reserved																		
7..1		PWM_SELL2					RW	0x00					[3:1]: Selects a target AD which the PWM2 is synchronized with 0x0: is not synchronized with ADs 0x1: is synchronized with HPADC0 0x2: is synchronized with HPADC1 0x3: is synchronized with LPADC in operation 0x4: is synchronized with LPADC0 0x5: is synchronized with LPADC1 0x6: is synchronized with LPADC2 0x7: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM2 is synchronized with																		
0		PWM2_EN					RW	0x0					Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Written values can always be read out. Changed contents are reflected to the HW by writing “1” in PWM2_UPDATE.																		

3.9.12.3.162 {0x5620} PWM2_UPDATE Details

Table SCU (Sensor Control Unit)-270

Local Address: 0x5620																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM2_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM2_UPDATE				WO	0x0				Reflects a set value in PWM2’s operation by writing “1” on this register.																				

3.9.12.3.163 {0x5624} PWM3_PARAM Details

Table SCU (Sensor Control Unit)-271

Local Address: 0x5624																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM3_THRESH																PWM3_CYCLE															
Bits				Name				Type		Reset Value				Description																	
31..16				PWM3_THRESH				RW		0x0000				Sets the duty of PWM3 output																	
15..0				PWM3_CYCLE				RW		0x0000				Sets the output cycle of PWM3																	

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.164 {0x5628} PWM3_EN Details

Table SCU (Sensor Control Unit)-272

Local Address: 0x5628																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																PWM_SELL3								PWM3_EN							
Bits				Name				Type		Reset Value				Description																	
31..8				Reserved				RO		0x000000				Reserved																	
7..1				PWM_SELL3				RW		0x00				[3:1]: Selects a target AD which the PWM3 is synchronized with 0x0: is not synchronized with ADs 0x1: is synchronized with HPADC0 0x2: is synchronized with HPADC1 0x3: is synchronized with LPADC in operation 0x4: is synchronized with LPADC0 0x5: is synchronized with LPADC1 0x6: is synchronized with LPADC2 0x7: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM3 is synchronized with																	
0				PWM3_EN				RW		0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Written values can always be read out. Changed contents are reflected to the HW by writing “1” in PWM3_UPDATE.																	

3.9.12.3.165 {0x562C} PWM3_UPDATE Details

Table SCU (Sensor Control Unit)-273

Local Address: 0x562C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM3_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM3_UPDATE				WO	0x0				Reflects a set value in PWM3’s operation by writing “1” on this register.																				

3.9.12.3.166 {0x5630} PWM_PASE0 Details

Table SCU (Sensor Control Unit)-274

Local Address: 0x5630																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM_CNTEN0																PWM_DELAY0															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN0				RW	0x0000				[19:16]: Sets the PWM prescale 0x0: 1/1 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128 0x8: 1/256 [23:20]: The number of AD capturing based on the PWM (from 1 to 15 available) [31:24]: Positioning for capturing AD based on the PWM (step is SCU_CK unit) (from 3 to 255 available)																				
15..0		PWM_DELAY0				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.167 {0x5634} PWM_PASE1 Details

Table SCU (Sensor Control Unit)-275

Local Address: 0x5634																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN1																PWM_DELAY1															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN1				RW	0x0000				PWM1 setting for the control specification, refer to PWM_CNTEN0																				
15..0		PWM_DELAY1				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.168 {0x5638} PWM_PASE2 Details

Table SCU (Sensor Control Unit)-276

Local Address: 0x5638																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN2																PWM_DELAY2															
Bits		Name				Type		Reset Value				Description																			
31..16		PWM_CNTEN2				RW		0x0000				PWM2 setting for the control specification, refer to PWM_CNTEN0																			
15..0		PWM_DELAY2				RW		0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																			

3.9.12.3.169 {0x563C} PWM_PASE3 Details

Table SCU (Sensor Control Unit)-277

Local Address: 0x563C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN3																PWM_DELAY3															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN3				RW	0x0000				PWM3 setting for the control specification, refer to PWM_CNTEN0																				
15..0		PWM_DELAY3				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.170 {0x5640} PWM4_PARM Details

Table SCU (Sensor Control Unit)-278

Local Address: 0x5640																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM4_THRESH																PWM4_CYCLE															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM4_THRESH				RW	0x0000				Sets the duty of PWM4 output																				
15..0		PWM4_CYCLE				RW	0x0000				Sets the output cycle of PWM4																				

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.171 {0x5644} PWM4_EN Details

100 : LPADC0 101:LPADC1 110:LPADC2 111:LPADC3

Table SCU (Sensor Control Unit)-279

Local Address: 0x5644																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PWM_SELL4				PWM4_EN			
Bits		Name				Type	Reset Value				Description																				
31..8		Reserved				RO	0x000000				Reserved																				
7..1		PWM_SELL4				RW	0x00				[3:1]: Selects a target AD which the PWM4 is synchronized with 0x0: is not synchronized with ADs 0x1: is synchronized with HPADC0 0x2: is synchronized with HPADC1 0x3: is synchronized with LPADC in operation 0x4: is synchronized with LPADC0 0x5: is synchronized with LPADC1 0x6: is synchronized with LPADC2 0x7: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM4 is synchronized with																				
0		PWM4_EN				RW	0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Changed contents are reflected to the HW by writing “1” in PWM4_UPDATE.																				

3.9.12.3.172 {0x5648} PWM4_UPDATE Details

Table SCU (Sensor Control Unit)-280

Local Address: 0x5648																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM4_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM4_UPDATE				WO	0x0				Reflects a set value in PWM4’s operation by writing “1” on this register.																				

3.9.12.3.173 {0x564C} PWM5_PARAM Details

Table SCU (Sensor Control Unit)-281

Local Address: 0x564C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM5_THRESH																PWM5_CYCLE															
Bits		Name				Type		Reset Value				Description																			
31..16		PWM5_THRESH				RW		0x0000				Sets the duty of PWM5 output																			
15..0		PWM5_CYCLE				RW		0x0000				Sets the output cycle of PWM5																			

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.174 {0x5650} PWM5_EN Details

Table SCU (Sensor Control Unit)-282

Local Address: 0x5650																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																PWM_SELL5								PWM5_EN							
Bits		Name				Type	Reset Value				Description																				
31..8		Reserved				RO	0x000000				Reserved																				
7..1		PWM_SELL5				RW	0x00				[3:1]: Selects a target AD which the PWM5 is synchronized with 000: is not synchronized with ADs 001: is synchronized with HPADC0 002: is synchronized with HPADC1 003: is synchronized with LPADC in operation 004: is synchronized with LPADC0 005: is synchronized with LPADC1 006: is synchronized with LPADC2 007: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM5 is synchronized with																				
0		PWM5_EN				RW	0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Written values can always be read out. Changed contents are reflected to the HW by writing “1” in PWM5_UPDATE.																				

3.9.12.3.175 {0x5654} PWM5_UPDATE Details

Table SCU (Sensor Control Unit)-283

Local Address: 0x5654																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														PWM5_UPDATE	
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM5_UPDATE				WO	0x0				Reflects a set value in PWM5’s operation by writing “1” on this register.																				

3.9.12.3.176 {0x5658} PWM6_PARAM Details

Table SCU (Sensor Control Unit)-284

Local Address: 0x5658																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM6_THRESH																PWM6_CYCLE															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM6_THRESH				RW	0x0000				Sets the duty of PWM6 output																				
15..0		PWM6_CYCLE				RW	0x0000				Sets the output cycle of PWM6																				

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.177 {0x565C} PWM6_EN Details

Table SCU (Sensor Control Unit)-285

Local Address: 0x565C																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PWM_SELL6				PWM6_EN			
Bits		Name				Type	Reset Value				Description																				
31..8		Reserved				RO	0x000000				Reserved																				
7..1		PWM_SELL6				RW	0x00				[3:1]: Selects a target AD which the PWM6 is synchronized with 000: is not synchronized with ADs 001: is synchronized with HPADC0 002: is synchronized with HPADC1 003: is synchronized with LPADC in operation 004: is synchronized with LPADC0 005: is synchronized with LPADC1 006: is synchronized with LPADC2 007: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM6 is synchronized with																				
0		PWM6_EN				RW	0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Written values can always be read out. Changed contents are reflected to the HW by writing “1” in PWM6_UPDATE.																				

3.9.12.3.178 {0x5660} PWM6_UPDATE Details

Table SCU (Sensor Control Unit)-286

Local Address: 0x5660																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM6_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM6_UPDATE				WO	0x0				Reflects a set value in PWM6’s operation by writing “1” on this register.																				

3.9.12.3.179 {0x5664} PWM7_PARAM Details

Table SCU (Sensor Control Unit)-287

Local Address: 0x5664																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM7_THRESH																PWM7_CYCLE															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM7_THRESH				RW	0x0000				Sets the duty of PWM7 output																				
15..0		PWM7_CYCLE				RW	0x0000				Sets the output cycle of PWM7																				

For formulas of the cycle and the DUTY, refer to the below.

As for the formula of the PWM cycle, refer to Section 3.9.11.2.1, and as for the formula of the DUTY (period of HIGH/cycle) of the PWM output, refer to Section 3.9.11.2.2.

3.9.12.3.180 {0x5668} PWM7_EN Details

Table SCU (Sensor Control Unit)-288

Local Address: 0x5668																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																PWM_SELL7								PWM7_EN							
Bits				Name				Type		Reset Value				Description																	
31..8				Reserved				RO		0x000000				Reserved																	
7..1				PWM_SELL7				RW		0x00				[3:1]: Selects a target AD which the PWM7 is synchronized with 000: is not synchronized with ADs 001: is synchronized with HPADC0 002: is synchronized with HPADC1 003: is synchronized with LPADC in operation 004: is synchronized with LPADC0 005: is synchronized with LPADC1 006: is synchronized with LPADC2 007: is synchronized with LPADC3 [6:4]: Selects a target PWM which the PWM7 is synchronized with																	
0				PWM7_EN				RW		0x0				Controls the permission/stop of the PWM's operation. The operation is permitted by writing “1”. The operation is suspended by writing “0”. Written values can always be read out. Changed contents are reflected to the HW by writing “1” in PWM7_UPDATE.																	

3.9.12.3.181 {0x566C} PWM7_UPDATE Details

Table SCU (Sensor Control Unit)-289

Local Address: 0x566C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PWM7_UPDATE
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		PWM7_UPDATE				WO	0x0				Reflects a set value in PWM7’s operation by writing “1” on this register.																				

3.9.12.3.182 {0x5670} PWM_PASE4 Details

Table SCU (Sensor Control Unit)-290

Local Address: 0x5670																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN4																PWM_DELAY4															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN4				RW	0x0000				PWM4 setting for the control specification, refer to PWM_CNTEN0																				
15..0		PWM_DELAY4				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.183 {0x5674} PWM_PASE5 Details

Table SCU (Sensor Control Unit)-291

Local Address: 0x5674																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN5																PWM_DELAY5															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN5				RW	0x0000				PWM5 setting for the control specification, refer to PWM_CNTEN0																				
15..0		PWM_DELAY5				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.184 {0x5678} PWM_PASE6 Details

Table SCU (Sensor Control Unit)-292

Local Address: 0x5678																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM_CNTEN6																PWM_DELAY6															
Bits		Name				Type		Reset Value				Description																			
31..16		PWM_CNTEN6				RW		0x0000				PWM6 setting for the control specification, refer to PWM_CNTEN0																			
15..0		PWM_DELAY6				RW		0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																			

3.9.12.3.185 {0x567C} PWM_PASE7 Details

Table SCU (Sensor Control Unit)-293

Local Address: 0x567C																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CNTEN7																PWM_DELAY7															
Bits		Name				Type	Reset Value				Description																				
31..16		PWM_CNTEN7				RW	0x0000				PWM7 setting for the control specification, refer to PWM_CNTEN0																				
15..0		PWM_DELAY7				RW	0x0000				Adjusts phases for the timing of AD data capturing (to SCU unit 0-65535 clock)																				

3.9.12.3.186 {0x5680} PWM_TIMER01 details

When the PWM is not used, PWM generator can be used as a timer. In this case, counter values within the timer can be read.

Table SCU (Sensor Control Unit)-294

Local Address: 0x5680																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER1																TIMER0															
Bits		Name				Type	Reset Value				Description																				
31..16		TIMER1				RO	0x0000				Counter value of PWM1																				
15..0		TIMER0				RO	0x0000				Counter value of PWM0																				

3.9.12.3.187 {0x5684} PWM_TIMER23 Details

When the PWM is not used, PWM generator can be used as a timer. In this case, counter values within the timer can be read.

Table SCU (Sensor Control Unit)-295

Local Address: 0x5684																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER3																TIMER2															
Bits		Name				Type	Reset Value				Description																				
31..16		TIMER3				RO	0x0000				Counter value of PWM3																				
15..0		TIMER2				RO	0x0000				Counter value of PWM2																				

3.9.12.3.188 {0x5688} PWM_TIMER45 Details

When the PWM is not used, PWM generator can be used as a timer. In this case, counter values within the timer can be read.

Table SCU (Sensor Control Unit)-296

Local Address: 0x5688																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER5																TIMER4															
Bits		Name				Type	Reset Value				Description																				
31..16		TIMER5				RO	0x0000				Counter value of PWM5																				
15..0		TIMER4				RO	0x0000				Counter value of PWM4																				

3.9.12.3.189 {0x568C} PWM_TIMER67 Details

When the PWM is not used, PWM generator can be used as a timer. In this case, counter values within the timer can be read.

Table SCU (Sensor Control Unit)-297

Local Address: 0x568C																Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
TIMER7																TIMER6															
Bits				Name				Type		Reset Value				Description																	
31..16				TIMER7				RO		0x0000				Counter value of PWM7																	
15..0				TIMER6				RO		0x0000				Counter value of PWM6																	

3.9.12.3.190 {0x5690} PWM_FUNCSEL0 Details

When synthesizing the PWM, you can designate the polarity of the source PWM (for PWM0-3).

Table SCU (Sensor Control Unit)-298

Local Address: 0x5690																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_SEL_INV3								PWM_SEL_INV2								PWM_SEL_INV1								PWM_SEL_INV0							
Bits		Name						Type	Reset Value				Description																		
31..24		PWM_SEL_INV3						RW	0x00																						
23..16		PWM_SEL_INV2						RW	0x00																						
15..8		PWM_SEL_INV1						RW	0x00																						
7..0		PWM_SEL_INV0						RW	0x00																						

3.9.12.3.191 {0x5694} PWM_FUNC1 Details

When synthesizing the PWM, you can designate the polarity of the source PWM (for PWM4-7).

Table SCU (Sensor Control Unit)-299

Local Address: 0x5694																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_SEL_INV7								PWM_SEL_INV6								PWM_SEL_INV5								PWM_SEL_INV4							
Bits		Name						Type	Reset Value				Description																		
31..24		PWM_SEL_INV7						RW	0x00																						
23..16		PWM_SEL_INV6						RW	0x00																						
15..8		PWM_SEL_INV5						RW	0x00																						
7..0		PWM_SEL_INV4						RW	0x00																						

3.9.12.3.192 {0x5698} PWM_FUCN2 Details

When synthesizing the PWM, you can designate whether to use the PWM or not (for PWM0-3).

Table SCU (Sensor Control Unit)-300

Local Address: 0x5698																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM_SEL_DIS3								PWM_SEL_DIS2								PWM_SEL_DIS1								PWM_SEL_DIS0							
Bits		Name						Type		Reset Value				Description																	
31..24		PWM_SEL_DIS3						RW		0x00																					
23..16		PWM_SEL_DIS2						RW		0x00																					
15..8		PWM_SEL_DIS1						RW		0x00																					
7..0		PWM_SEL_DIS0						RW		0x00																					

3.9.12.3.193 {0x569C} PWM_FUNC3 Details

When synthesizing the PWM, you can designate whether to use the PWM or not (for PWM4-7).

Table SCU (Sensor Control Unit)-301

Local Address: 0x569C																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
PWM_SEL_DIS7								PWM_SEL_DIS6								PWM_SEL_DIS5								PWM_SEL_DIS4							
Bits		Name						Type		Reset Value						Description															
31..24		PWM_SEL_DIS7						RW		0x00						Invalid because the HWdoes not exist															
23..16		PWM_SEL_DIS6						RW		0x00						Invalid because the HWdoes not exist															
15..8		PWM_SEL_DIS5						RW		0x00						Invalid because the HWdoes not exist															
7..0		PWM_SEL_DIS4						RW		0x00						Invalid because the HWdoes not exist															

3.9.12.3.194 {0x56A0} PWM_FUNC4 Details

You can select synthesis by ANDing or ORing PWMs (0: AND, 1: OR)

Table SCU (Sensor Control Unit)-302

Local Address: 0x56A0																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_SEL7				PWM_SEL6				PWM_SEL5				PWM_SEL4				PWM_SEL3				PWM_SEL2				PWM_SEL1				PWM_SEL0			
Bits		Name						Type	Reset Value						Description																
31..28		PWM_SEL7						RW	0x0						Invalid setting																
27..24		PWM_SEL6						RW	0x0						Invalid setting																
23..20		PWM_SEL5						RW	0x0						Invalid setting																
19..16		PWM_SEL4						RW	0x0						Invalid setting																
15..12		PWM_SEL3						RW	0x0						For PWM3 unit																
11..8		PWM_SEL2						RW	0x0						For PWM2 unit																
7..4		PWM_SEL1						RW	0x0						For PWM1 unit																
3..0		PWM_SEL0						RW	0x0						For PWM0 unit																

3.9.12.3.195 {0x56A4} POWER_EN Details

Prohibited setting

Table SCU (Sensor Control Unit)-303

Local Address: 0x56A4																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																POWER_EN															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		POWER_EN				RW	0xFFFF				Prohibited setting																				

3.9.12.3.196 {0x0 .. 0x3FFC} SEQ_IRAM Details

Instruction RAM array for internal sequencer

Refer to Section 3.9.12.11.

Table SCU (Sensor Control Unit)-304

Local Address: 0x0				Memory Type: RW (read/write) Reset Value: 0xxxxxxxxx
Bits	Name	Type	Reset Value	Description
31..0	SEQ_IRAM	RW	0xxxxxxxxx	Instruction RAM array for internal sequencer

3.9.12.3.197 {0x4000 .. 0x4FFC} SEQ_DRAM Details

Data Ram array for internal sequencer

Table SCU (Sensor Control Unit)-305

Local Address: 0x4000				Memory Type: RW (read/write) Reset Value: 0xxxxxxxxx
Bits	Name	Type	Reset Value	Description
31..0	SEQ_DRAM	RW	0xxxxxxxxx	Data Ram array for internal sequencer

3.9.12.4 SCU_ADCIF_REG Register List

The following describes 32 bit address offset from the CPU. For calculating the address from the CPU, add this address to each offset in the table.

Offset:0x0018dc00 (Mirror:0x0418dc00)

For the offset Address from 0x0200 to 0x03D4 of the ADCIF control registers, refer to Chapter of ADC (3.21).

3.9.12.5 SCU_MATH_PROC_REG Overview

Only sequencers in the SCU can access this register.

The following describes 32 bit address offsets which can be seen from the sequencers in the SCU. For calculating the address to access from the sequencer in the CPU, add this address to each offset in the table.

Offset:0x0000e000

3.9.12.6 SCU_MATH_PROC_REG Register List

Table SCU (Sensor Control Unit)-306

Offset (Transaction Port)	Address	Name	Type	Size (bits)	Description	Reset Value
0x0		MATH_PROC_EXE	RO	32		0x00000000
0x4		WRITE_DATA_SET0	RW	32		0x00000000
0x8		WRITE_DATA_SET1	RW	32		0x00000000
0xC		WRITE_DATA_SET2	RW	32		0x00000000
0x10		WRITE_DATA_SET3	RW	32		0x00000000
0x14		WRITE_DATA_SET4	RW	32		0x00000000
0x18		WRITE_DATA_SET5	RW	32		0x00000000
0x80		READ_DATA_SET0	RO	32		0x00000000
0x84		READ_DATA_SET1	RO	32		0x00000000
0x88		READ_DATA_SET2	WO	32		0x00000000

3.9.12.6.1 {0x0} MATH_PROC_EXE Details

Table SCU (Sensor Control Unit)-307

Local Address: 0x0																Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																MATH_PROC_EXE															
Bits		Name				Type		Reset Value		Description																					
31..16		Reserved				RO		0x0000		Reserved																					
15..0		MATH_PRO C_EXE				RO		0x0000		This is a flag of determining whether MATH_PROC should be executed or not. 1: Performs MATH_PROC processing 0, 4, 8 to 15 bit only: valid The following describes the conditions that the value of MATH_PROC_EXE becomes “1”. 0, 4 bit: When if any of the following (1), (2), and (3) are true (1) When OFST_GAIN_EN{0x5070} of MATHID which you use is “1” (2) When MATHFUNC_SEL{0x508c} of MATHID which you use is set (3) When the set value for DECIMATION_PARAM0/1 {0x5084/0x5088} of MATHID which you use is 'd9 or less 8 to 15 bit: When if any of the following (1) and (2) are true (1) When OFST_GAIN_EN{0x5070} of MATHID which you use is “1” (2) When MATHFUNC_SEL{0x508c} of MATHID which you use is set Refer to Section 3.9.9.9.																					

3.9.12.6.2 {0x4} WRITE_DATA_SET0 Details

Table SCU (Sensor Control Unit)-308

Local Address: 0x4																Register Type: RW (read/write) Reset Value: 0x00000000																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0															
DATA_X																Reserved								VEC_ELE_NUM				Reserved								FIFO_W_ID			
Bits				Name				Type				Reset Value				Description																							
31..16				DATA_X				RW				0x0000				Vector element X of the target data for processing request																							
15..10				Reserved				RO				0x00				Reserved																							
9..8				VEC_ELE_NUM				RW				0x0				The number of Vector element X of the target data for processing request “0” is equivalent to “1” element. You can select one integer from 1, 2, and 3.																							
7..4				Reserved				RO				0x0				Reserved																							
3..0				FIFO_W_ID				RW				0x0				You can select one integer for MATH ID for processing request from 0, 4, 8 to 15.																							

3.9.12.6.3 {0x8} WRITE_DATA_SET1 Details

Table SCU (Sensor Control Unit)-309

Local Address: 0x8																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_Z																DATA_Y															
Bits		Name				Type		Reset Value				Description																			
31..16		DATA_Z				RW		0x0000																							
15..0		DATA_Y				RW		0x0000																							

3.9.12.6.4 {0xC} WRITE_DATA_SET2 Details

Table SCU (Sensor Control Unit)-310

Local Address: 0xC																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN_X																OFST_X															
Bits		Name				Type		Reset Value				Description																			
31..16		GAIN_X				RW		0x0000																							
15..0		OFST_X				RW		0x0000																							

3.9.12.6.5 {0x10} WRITE_DATA_SET3 Details

Table SCU (Sensor Control Unit)-311

Local Address: 0x10																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN_Y																OFST_Y															
Bits		Name				Type		Reset Value				Description																			
31..16		GAIN_Y				RW		0x0000																							
15..0		OFST_Y				RW		0x0000																							

3.9.12.6.6 {0x14} WRITE_DATA_SET4 Details

Table SCU (Sensor Control Unit)-312

Local Address: 0x14																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN_Z																OFST_Z															
Bits		Name				Type		Reset Value				Description																			
31..16		GAIN_Z				RW		0x0000																							
15..0		OFST_Z				RW		0x0000																							

3.9.12.6.7 {0x18} WRITE_DATA_SET5 Details

Table SCU (Sensor Control Unit)-313

Local Address: 0x18																		Register Type: RW (read/write)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													DATA_UPDATE		
Bits	Name							Type	Reset Value							Description															
31..1	Reserved							RO	0x00000000							Reserved															
0	DATA_UPDATE							RW	0x0							This can be set if some changes need to be made between WRITE_DATA_SET0 and WRITE_DATA_SET5, or if MATH is executed.															

3.9.12.6.8 {0x80} READ_DATA_SET0 Details

Table SCU (Sensor Control Unit)-314

Local Address: 0x80																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_X																Reserved				VEC_ELE_NUM				Reserved				FIFO_W_ID			
Bits	Name			Type	Reset Value			Description																							
31..16	DATA_X			RO	0x0000																										
15..10	Reserved			RO	0x00			Reserved																							
9..8	VEC_ELE_NUM			RO	0x0																										
7..4	Reserved			RO	0x0			Reserved																							
3..0	FIFO_W_ID			RO	0x0			MATH ID (from 0 to 15) which is requested to process is output. The order in which the MATH ID is output is not the same as the order of the input.																							

3.9.12.6.9 {0x84} READ_DATA_SET1 Details

Table SCU (Sensor Control Unit)-315

Local Address: 0x84																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_Z																DATA_Y															
Bits		Name				Type	Reset Value				Description																				
31..16		DATA_Z				RO	0x0000																								
15..0		DATA_Y				RO	0x0000																								

3.9.12.6.10 {0x88} READ_DATA_SET2 Details

Table SCU (Sensor Control Unit)-316

Local Address: 0x88																Register Type: WO (write only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved																																DATA_READ_DONE
Bits		Name						Type	Reset Value						Description																	
31..1		Reserved						WO	0x00000000						Reserved																	
0		DATA_READ_DONE						WO	0x0																							

3.9.12.7 SCU_SEQ_REG Overview

Only sequencers in the SCU can access these registers.

The following describes 32 bit address offset which can be seen from the sequencer in the SCU. For calculating the address to access from the sequencer in the SCU, add this Offset: 0x0000e400 to each Offset Address (Transaction Port) in the table.

Offset: 0x0000e400

3.9.12.8 SCU_SEQ_REG Register List

Table SCU (Sensor Control Unit)-317

Offset (Transaction Port)	Address	Name	Type	Size (bits)	Description	Reset Value
0x0		EXTERNAL_STT0	RO	32		0x00000000
0x4		EXTERNAL_STT1	RO	32		0x00000000
0x8		START_CTRL	WO	32		0x00000000
0x10		ISOPSTT	RW	32		0x00000000
0x14		ISOPINT	RW	32		0x00000000
0x18		POWER_CTRL	RW	32		0x00000000
0x20		TIME_STAMP_MSB	RO	32		0x00000000
0x24		TIME_STAMP_LSB	RO	32		0x00000000
0x40		ISOPMONOUT	RW	32		0x00000000
0x44		SCU_ISOP_POWER	RW	32	0: CK_SCU 1: CK_SPI 2: CK_I2C0 3: CK_I2C1	0x00000000
0x190		TIMER_SEL	RW	32		0x00000000

3.9.12.8.1 {0x0} EXTERNAL_STT0 Details

Table SCU (Sensor Control Unit)-318

Local Address: 0x0																Register Type: RO (read only) Reset Value: 0x00000000																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
TIMER_INT2	TIMER_INT1	TIMER_INT0	FIFO1_ALL_ON_STT	FIFO0_ALL_ON_STT	MATH_PROC_READ_DATA_READY	MATH_PROC_WRITE_DATA_READY	HPADC1_NOT_EMPTY	HPADC0_NOT_EMPTY	LPADC_NOT_EMPTY3	LPADC_NOT_EMPTY2	LPADC_NOT_EMPTY1	LPADC_NOT_EMPTY0	I2C1_ACTIVE	I2C1_MASTER_ON_HOLD	I2C1_RX_ALMOST_FULL	I2C0_ACTIVE	I2C0_MASTER_ON_HOLD	I2C0_RX_ALMOST_FULL	PWD_I2C_ON_STT	PWD_SPI_ON_STT	APB_ACCESS_INHIBIT	EXE_REQ_STT															
Bits	Name											Type	Reset Value	Description																							
31	TIMER_INT2											RO	0x0																								
30	TIMER_INT1											RO	0x0																								
29	TIMER_INT0											RO	0x0																								
28	FIFO1_ALL_ON_STT											RO	0x0	Indicates that the power supply state of FIFO SRAM 32KByte region is All On																							
27	FIFO0_ALL_ON_STT											RO	0x0	Indicates that the power supply state of FIFO SRAM 8KByte region is All On.																							
26	MATH_PROC_READ_DATA_READY											RO	0x0	Indicates the status that the readout from MATH_PROC is possible																							
25	MATH_PROC_WRITE_DATA_READY											RO	0x0	Indicates the status that the write to MATH_PROC is possible																							
24	HPADC1_NOT_EMPTY											RO	0x0	Indicates that one or more data exist in the FIFO for HPADC1																							
23	HPADC0_NOT_EMPTY											RO	0x0	Indicates that one or more data exist in the FIFO for HPADC0																							
22	LPADC_NOT_EMPTY3											RO	0x0	Indicates that one or more data exist in the FIFO for LPADC																							
21	LPADC_NOT_EMPTY2											RO	0x0	Indicates that one or more data exist in the FIFO for LPADC																							

20	LPADC_NOT_EMPTY1	RO	0x0	Indicates that one or more data exist in the FIFO for LPADC
19	LPADC_NOT_EMPTY0	RO	0x0	Indicates that one or more data exist in the FIFO for LPADC
18	I2C1_ACTIVE	RO	0x0	Indicates the operation active status of I2C1
17	I2C1_MASTER_ON_HOLD	RO	0x0	Indicates that the status is I2C1 TX_FIFO Empty, but a STOP command has not been issued
16	I2C1_RX_ALMOST_FULL	RO	0x0	Indicates that more data than designated exist in the RX_FIFO of I2C1
15	I2C0_ACTIVE	RO	0x0	Indicates the operation active status of I2C0
14	I2C0_MASTER_ON_HOLD	RO	0x0	Indicates that the status is I2C0 TX_FIFO Empty, but a STOP command has not been issued
13	I2C0_RX_ALMOST_FULL	RO	0x0	Indicates that more data than designated exist in the RX_FIFO of I2C0
12	PWD_I2C_ON_STT	RO	0x0	Power supply status of PWD_I2C
11	PWD_SPI_ON_STT	RO	0x0	Power supply status of PWD_ SPI
10	APB_ACCESS_INHIBIT	RO	0x0	ORed signal of ACCESS_INHIBIT
9..0	EXE_REQ_STT	RO	0x000	Execution request to each sequencer

3.9.12.8.2 {0x4} EXTERNAL_STT1 Details

Table SCU (Sensor Control Unit)-319

Local Address: 0x4																Register Type: RO (read only) Reset Value: 0x00000000																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0												
LPADC_ACCESS_INHIBIT3		LPADC_ACCESS_INHIBIT2		LPADC_ACCESS_INHIBIT1		I2C1_FSM_STATUS				Reserved				I2C0_FSM_STATUS				MATH_EVENT_F				MATH_EVENT_R				APB_ACCESS_ERR		DRAM_ALL_ON_STT		Reserved		HPADC1_ACCESS_INHIBIT		HPADC0_ACCESS_INHIBIT		LPADC_ACCESS_INHIBIT		I2C1_ACCESS_INHIBIT		I2C0_ACCESS_INHIBIT		SPI_ACCESS_INHIBIT	
Bits		Name						Type	Reset Value	Description																																	
31		LPADC_ACCESS_INHIBIT3						RO	0x0																																		
30		LPADC_ACCESS_INHIBIT2						RO	0x0																																		
29		LPADC_ACCESS_INHIBIT1						RO	0x0																																		
28..24		I2C1_FSM_STATUS						RO	0x00	FSM status of I2C1																																	
23..21		Reserved						RO	0x0	Reserved																																	
20..16		I2C0_FSM_STATUS						RO	0x00	FSM status of I2C0																																	
15..13		MATH_EVENT_F						RO	0x0	The status of Math Function interrupt to the CPU																																	
12..10		MATH_EVENT_R						RO	0x0	The status of Math Function interrupt to the CPU																																	
9		APB_ACCESS_ERR						RO	0x0	Indicates “1” when APB error occurs																																	
8		DRAM_ALL_ON_STT						RO	0x0	Indicates the power supply status of the internal sequencer SEQ_DRAM																																	
7..6		Reserved						RO	0x0	Reserved																																	
5		HPADC1_ACCESS_INHIBIT						RO	0x0	Indicates that the sequencer is inhibited from accessing the target APB Slave																																	
4		HPADC0_ACCESS_INHIBIT						RO	0x0	Refer to HPADC1_ACCESS_INHIBIT																																	
3		LPADC_ACCESS_INHIBIT						RO	0x0	Refer to HPADC1_ACCESS_INHIBIT																																	
2		I2C1_ACCESS_INHIBIT						RO	0x0	Refer to HPADC1_ACCESS_INHIBIT																																	
1		I2C0_ACCESS_INHIBIT						RO	0x0	Refer to HPADC1_ACCESS_INHIBIT																																	
0		SPI_ACCESS_INHIBIT						RO	0x0	Refer to HPADC1_ACCESS_INHIBIT																																	

3.9.12.8.3 {0x8} START_CTRL Details

Table SCU (Sensor Control Unit)-320

Local Address: 0x8																Register Type: WO (write only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						EXE_ERR										Reserved						EXE_DONE									
Bits		Name						Type	Reset Value						Description																
31..26		Reserved						WO	0x00						Reserved																
25..16		EXE_ERR						WO	0x000						Indicates error notification of each sequencer when executed																
15..10		Reserved						WO	0x00						Reserved																
9..0		EXE_DONE						WO	0x000						Indicates execution-completed notification of each sequencer																

3.9.12.8.4 {0x10} ISOPSTT Details

Table SCU (Sensor Control Unit)-321

Local Address: 0x10																Register Type: RW (read/write)																											
																Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
LPADC_ACCESS_INHIBIT_ACK3			LPADC_ACCESS_INHIBIT_ACK2			LPADC_ACCESS_INHIBIT_ACK1			Reserved								ISOP_READY	Reserved								HPADC1_ACCESS_INHIBIT_ACK			HPADC0_ACCESS_INHIBIT_ACK			LPADC_ACCESS_INHIBIT_ACK			I2C1_ACCESS_INHIBIT_ACK			I2C0_ACCESS_INHIBIT_ACK			SPI_ACCESS_INHIBIT_ACK		
Bits		Name								Type		Reset Value		Description																													
31		LPADC_ACCESS_INHIBIT_ACK3								RW		0x0																															
30		LPADC_ACCESS_INHIBIT_ACK2								RW		0x0																															
29		LPADC_ACCESS_INHIBIT_ACK1								RW		0x0																															
28..17		Reserved								RO		0x000		Reserved																													
16		ISOP_READY								RW		0x0		Indicates “1” when the boot of the internal sequencer has been completed																													
15..6		Reserved								RO		0x000		Reserved																													
5		HPADC1_ACCESS_INHIBIT_ACK								RW		0x0		ACK output in response to the INHIBIT request																													
4		HPADC0_ACCESS_INHIBIT_ACK								RW		0x0		Refer HPADC1_ACCESS_INHIBIT_ACK to																													
3		LPADC_ACCESS_INHIBIT_ACK								RW		0x0		Refer HPADC1_ACCESS_INHIBIT_ACK to																													
2		I2C1_ACCESS_INHIBIT_ACK								RW		0x0		Refer HPADC1_ACCESS_INHIBIT_ACK to																													
1		I2C0_ACCESS_INHIBIT_ACK								RW		0x0		Refer HPADC1_ACCESS_INHIBIT_ACK to																													
0		SPI_ACCESS_INHIBIT_ACK								RW		0x0		Refer HPADC1_ACCESS_INHIBIT_ACK to																													

3.9.12.8.5 {0x14} ISOPINT Details

Table SCU (Sensor Control Unit)-322

Local Address: 0x14																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										ISOP_INT					
Bits		Name		Type	Reset Value		Description																								
31..4		Reserved		RO	0x00000000		Reserved																								
3..0		ISOP_INT		RW	0x0		Information interrupt output to the CPU (used for SW definition)																								

3.9.12.8.6 {0x18} POWER_CTRL Details

Table SCU (Sensor Control Unit)-323

Local Address: 0x18																Register Type: RW (read/write) Reset Value: 0x00000000																				
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								APB_ACCESS_ERR_CLR	Reserved								FIFO1_RETENTION_REQ	FIFO0_RETENTION_REQ	Reserved								FIFO1_ALL_ON_REQ	FIFO0_ALL_ON_REQ	Reserved							
Bits	Name							Type	Reset Value		Description																									
31..25	Reserved							RO	0x00		Reserved																									
24	APB_ACCESS_ERR_CLR							WO	0x0		Clear the APB_ACCESS_ERR in EXTERNAL_STT1																									
23..18	Reserved							RO	0x00		Reserved																									
17	FIFO1_RETENTION_REQ							RW	0x0		Requests for the retention of the power supply status of FIFO SRAM 32 KByte region																									
16	FIFO0_RETENTION_REQ							RW	0x0		Requests for the retention of the power supply status of FIFO SRAM 8 KByte region																									
15..10	Reserved							RO	0x00		Reserved																									
9	FIFO1_ALL_ON_REQ							RW	0x0		Requests that the power supply status of FIFO SRAM 34 KByte region turn All On																									
8	FIFO0_ALL_ON_REQ							RW	0x0		Requests that the power supply status of FIFO SRAM 6 KByte region turn All On																									
7..0	Reserved							RO	0x00		Reserved																									

3.9.12.8.7 {0x20} TIME_STAMP_MSB Details

Table SCU (Sensor Control Unit)-324

Local Address: 0x20															Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TIME_STAMP_46_15																																
Bits	Name							Type	Reset Value							Description																
31..0	TIME_STAMP_46_15							RO	0x00000000							Time stamp information with 47 bit data width on the MSB side																

3.9.12.8.8 {0x24} TIME_STAMP_LSB Details

Table SCU (Sensor Control Unit)-325

Local Address: 0x24																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
TIME_STAMP_31_0																																			
Bits		Name						Type	Reset Value						Description																				
31..0		TIME_STAMP_31_0						RO	0x00000000						Time stamp information with 47 bit data width on the LSB side																				

3.9.12.8.9 {0x40} ISOPMONOUT Details

Table SCU (Sensor Control Unit)-326

Local Address: 0x40																		Register Type: RW (read/write) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MON1										Reserved						MON0									
Bits		Name						Type	Reset Value						Description																
31..26		Reserved						RO	0x00						Reserved																
25..16		MON1						RW	0x000						Indicates debug monitor output for the external pin output																
15..10		Reserved						RO	0x00						Reserved																
9..0		MON0						RW	0x000						Indicates debug monitor output for the external pin output																

3.9.12.8.10 {0x44} SCU_ISOP_POWER Details

0: CK_SCU 1: CK_SPI 2: CK_I2C0 3: CK_I2C1

Table SCU (Sensor Control Unit)-327

Local Address: 0x44																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								CLK_EN							
Bits		Name				Type	Reset Value				Description																				
31..5		Reserved				RO	0x00000000				Reserved																				
4..0		CLK_EN				RW	0x00																								

3.9.12.8.11 {0x190} TIMER_SEL Details

Table SCU (Sensor Control Unit)-328

Local Address: 0x190																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TIMWE_SEL2								TIMWE_SEL1								TIMWE_SEL0							
Bits		Name						Type		Reset Value						Description															
31..24		Reserved						RO		0x00						Reserved															
23..16		TIMWE_SEL2						RW		0x00																					
15..8		TIMWE_SEL1						RW		0x00																					
7..0		TIMWE_SEL0						RW		0x00																					

3.9.12.9 SCU_FIFO_REG Overview

Offset:0x00180000 (Mirror:0x04180000)

The following describes 32 bit address offset from the CPU. For calculating the address from the CPU, add this Offset: 0x0000e400 to each Offset Address (Transaction Port) in the table.

Offset: 0x0000e400

3.9.12.10 SCU_FIFO_REG Register List

Table SCU (Sensor Control Unit)-329 SCU_FIFO_REG Register List

Offset Address (Transaction Port)	Name	Type	Size (bits)	Description	Reset Value
0x0	D0_W0_S_CTRL0	RW	32		0xA0000000
0x4	D0_W0_S_CTRL1	RW	32		0x00000000
0x8	D0_W0_S_STATUS	RO	32		0x00000000
0xC	D0_W0_S_TIMESTAMP0	RO	32		0x00000000
0x10	D0_W0_S_TIMESTAMP1	RO	32		0x00000000
0x20	D0_W1_S_CTRL0	RW	32		0xA0000000
0x24	D0_W1_S_CTRL1	RW	32		0x00000000
0x28	D0_W1_S_STATUS	RO	32		0x00000000
0x2C	D0_W1_S_TIMESTAMP0	RO	32		0x00000000
0x30	D0_W1_S_TIMESTAMP1	RO	32		0x00000000
0x40	D0_W2_S_CTRL0	RW	32		0xA0000000
0x44	D0_W2_S_CTRL1	RW	32		0x00000000
0x48	D0_W2_S_STATUS	RO	32		0x00000000
0x4C	D0_W2_S_TIMESTAMP0	RO	32		0x00000000
0x50	D0_W2_S_TIMESTAMP1	RO	32		0x00000000
0x60	D0_W3_S_CTRL0	RW	32		0xA0000000
0x64	D0_W3_S_CTRL1	RW	32		0x00000000
0x68	D0_W3_S_STATUS	RO	32		0x00000000
0x6C	D0_W3_S_TIMESTAMP0	RO	32		0x00000000
0x70	D0_W3_S_TIMESTAMP1	RO	32		0x00000000
0x80	D1_W0_S_CTRL0	RW	32		0xA0000000
0x84	D1_W0_S_CTRL1	RW	32		0x00000000
0x88	D1_W0_S_STATUS	RO	32		0x00000000
0x8C	D1_W0_S_TIMESTAMP0	RO	32		0x00000000

0x90	D1_W0_S_TIMSTAMP1	RO	32		0x00000000
0xA0	D1_W1_S_CTRL0	RW	32		0xA0000000
0xA4	D1_W1_S_CTRL1	RW	32		0x00000000
0xA8	D1_W1_S_STATUS	RO	32		0x00000000
0xAC	D1_W1_S_TIMSTAMP0	RO	32		0x00000000
0xB0	D1_W1_S_TIMSTAMP1	RO	32		0x00000000
0xC0	D1_W2_S_CTRL0	RW	32		0xA0000000
0xC4	D1_W2_S_CTRL1	RW	32		0x00000000
0xC8	D1_W2_S_STATUS	RO	32		0x00000000
0xCC	D1_W2_S_TIMSTAMP0	RO	32		0x00000000
0xD0	D1_W2_S_TIMSTAMP1	RO	32		0x00000000
0xE0	D1_W3_S_CTRL0	RW	32		0xA0000000
0xE4	D1_W3_S_CTRL1	RW	32		0x00000000
0xE8	D1_W3_S_STATUS	RO	32		0x00000000
0xEC	D1_W3_S_TIMSTAMP0	RO	32		0x00000000
0xF0	D1_W3_S_TIMSTAMP1	RO	32		0x00000000
0x100	N0_W_S_CTRL0	RW	32		0xA0000000
0x104	N0_W_S_CTRL1	RW	32		0x00000000
0x108	N0_W_S_STATUS	RO	32		0x00000000
0x10C	N0_W_S_TIMSTAMP0	RO	32		0x00000000
0x110	N0_W_S_TIMSTAMP1	RO	32		0x00000000
0x120	N1_W_S_CTRL0	RW	32		0xA0000000
0x124	N1_W_S_CTRL1	RW	32		0x00000000
0x128	N1_W_S_STATUS	RO	32		0x00000000
0x12C	N1_W_S_TIMSTAMP0	RO	32		0x00000000
0x130	N1_W_S_TIMSTAMP1	RO	32		0x00000000
0x140	N2_W_S_CTRL0	RW	32		0xA0000000
0x144	N2_W_S_CTRL1	RW	32		0x00000000
0x148	N2_W_S_STATUS	RO	32		0x00000000
0x14C	N2_W_S_TIMSTAMP0	RO	32		0x00000000
0x150	N2_W_S_TIMSTAMP1	RO	32		0x00000000
0x160	N3_W_S_CTRL0	RW	32		0xA0000000
0x164	N3_W_S_CTRL1	RW	32		0x00000000
0x168	N3_W_S_STATUS	RO	32		0x00000000
0x16C	N3_W_S_TIMSTAMP0	RO	32		0x00000000
0x170	N3_W_S_TIMSTAMP1	RO	32		0x00000000
0x180	N4_W_S_CTRL0	RW	32		0xA0000000
0x184	N4_W_S_CTRL1	RW	32		0x00000000

0x188	N4_W_S_STATUS	RO	32		0x00000000
0x18C	N4_W_S_TIMSTAMP0	RO	32		0x00000000
0x190	N4_W_S_TIMSTAMP1	RO	32		0x00000000
0x1A0	N5_W_S_CTRL0	RW	32		0xA0000000
0x1A4	N5_W_S_CTRL1	RW	32		0x00000000
0x1A8	N5_W_S_STATUS	RO	32		0x00000000
0x1AC	N5_W_S_TIMSTAMP0	RO	32		0x00000000
0x1B0	N5_W_S_TIMSTAMP1	RO	32		0x00000000
0x1C0	N6_W_S_CTRL0	RW	32		0xA0000000
0x1C4	N6_W_S_CTRL1	RW	32		0x00000000
0x1C8	N6_W_S_STATUS	RO	32		0x00000000
0x1CC	N6_W_S_TIMSTAMP0	RO	32		0x00000000
0x1D0	N6_W_S_TIMSTAMP1	RO	32		0x00000000
0x1E0	N7_W_S_CTRL0	RW	32		0xA0000000
0x1E4	N7_W_S_CTRL1	RW	32		0x00000000
0x1E8	N7_W_S_STATUS	RO	32		0x00000000
0x1EC	N7_W_S_TIMSTAMP0	RO	32		0x00000000
0x1F0	N7_W_S_TIMSTAMP1	RO	32		0x00000000
0x200	V0_W_C_CTRL0	RW	32		0xA0000000
0x204	V0_W_C_CTRL1	RW	32		0x00000000
0x208	V0_W_C_STATUS	RO	32		0x00000000
0x20C	V0_W_C_TIMSTAMP0	RO	32		0x00000000
0x210	V0_W_C_TIMSTAMP1	RO	32		0x00000000
0x214	V0_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x218	V0_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x220	V1_W_C_CTRL0	RW	32		0xA0000000
0x224	V1_W_C_CTRL1	RW	32		0x00000000
0x228	V1_W_C_STATUS	RO	32		0x00000000
0x22C	V1_W_C_TIMSTAMP0	RO	32		0x00000000
0x230	V1_W_C_TIMSTAMP1	RO	32		0x00000000
0x234	V1_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x238	V1_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x240	V2_W_C_CTRL0	RW	32		0xA0000000
0x244	V2_W_C_CTRL1	RW	32		0x00000000
0x248	V2_W_C_STATUS	RO	32		0x00000000
0x24C	V2_W_C_TIMSTAMP0	RO	32		0x00000000
0x250	V2_W_C_TIMSTAMP1	RO	32		0x00000000
0x254	V2_W_C_TIMSTAMP_SET0	RW	32		0x00000000

0x258	V2_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x260	V3_W_C_CTRL0	RW	32		0xA0000000
0x264	V3_W_C_CTRL1	RW	32		0x00000000
0x268	V3_W_C_STATUS	RO	32		0x00000000
0x26C	V3_W_C_TIMSTAMP0	RO	32		0x00000000
0x270	V3_W_C_TIMSTAMP1	RO	32		0x00000000
0x274	V3_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x278	V3_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x280	V4_W_C_CTRL0	RW	32		0xA0000000
0x284	V4_W_C_CTRL1	RW	32		0x00000000
0x288	V4_W_C_STATUS	RO	32		0x00000000
0x28C	V4_W_C_TIMSTAMP0	RO	32		0x00000000
0x290	V4_W_C_TIMSTAMP1	RO	32		0x00000000
0x294	V4_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x298	V4_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x2A0	V5_W_C_CTRL0	RW	32		0xA0000000
0x2A4	V5_W_C_CTRL1	RW	32		0x00000000
0x2A8	V5_W_C_STATUS	RO	32		0x00000000
0x2AC	V5_W_C_TIMSTAMP0	RO	32		0x00000000
0x2B0	V5_W_C_TIMSTAMP1	RO	32		0x00000000
0x2B4	V5_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x2B8	V5_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x2C0	V6_W_C_CTRL0	RW	32		0xA0000000
0x2C4	V6_W_C_CTRL1	RW	32		0x00000000
0x2C8	V6_W_C_STATUS	RO	32		0x00000000
0x2CC	V6_W_C_TIMSTAMP0	RO	32		0x00000000
0x2D0	V6_W_C_TIMSTAMP1	RO	32		0x00000000
0x2D4	V6_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x2D8	V6_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x2E0	V7_W_C_CTRL0	RW	32		0xA0000000
0x2E4	V7_W_C_CTRL1	RW	32		0x00000000
0x2E8	V7_W_C_STATUS	RO	32		0x00000000
0x2EC	V7_W_C_TIMSTAMP0	RO	32		0x00000000
0x2F0	V7_W_C_TIMSTAMP1	RO	32		0x00000000
0x2F4	V7_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x2F8	V7_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x300	V8_W_C_CTRL0	RW	32		0xA0000000
0x304	V8_W_C_CTRL1	RW	32		0x00000000

0x308	V8_W_C_STATUS	RO	32		0x00000000
0x30C	V8_W_C_TIMSTAMP0	RO	32		0x00000000
0x310	V8_W_C_TIMSTAMP1	RO	32		0x00000000
0x314	V8_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x318	V8_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x320	V9_W_C_CTRL0	RW	32		0xA0000000
0x324	V9_W_C_CTRL1	RW	32		0x00000000
0x328	V9_W_C_STATUS	RO	32		0x00000000
0x32C	V9_W_C_TIMSTAMP0	RO	32		0x00000000
0x330	V9_W_C_TIMSTAMP1	RO	32		0x00000000
0x334	V9_W_C_TIMSTAMP_SET0	RW	32		0x00000000
0x338	V9_W_C_TIMSTAMP_SET1	RW	32		0x00000000
0x1000	D0_R1_C_CTRL0	RW	32		0x0000FFFF
0x1004	D0_R1_C_CTRL1	RW	32		0x00000000
0x1008	D0_R1_C_STATUS0	RO	32		0x00000000
0x100C	D0_R1_C_STATUS1	RO	32		0x00000000
0x1010	D0_R1_C_TIMSTAMP0	RO	32		0x00000000
0x1014	D0_R1_C_TIMSTAMP1	RO	32		0x00000000
0x1020	D0_R2_C_CTRL0	RW	32		0x0000FFFF
0x1024	D0_R2_C_CTRL1	RW	32		0x00000000
0x1028	D0_R2_C_STATUS0	RO	32		0x00000000
0x102C	D0_R2_C_STATUS1	RO	32		0x00000000
0x1030	D0_R2_C_TIMSTAMP0	RO	32		0x00000000
0x1034	D0_R2_C_TIMSTAMP1	RO	32		0x00000000
0x1040	D1_R1_C_CTRL0	RW	32		0x0000FFFF
0x1044	D1_R1_C_CTRL1	RW	32		0x00000000
0x1048	D1_R1_C_STATUS0	RO	32		0x00000000
0x104C	D1_R1_C_STATUS1	RO	32		0x00000000
0x1050	D1_R1_C_TIMSTAMP0	RO	32		0x00000000
0x1054	D1_R1_C_TIMSTAMP1	RO	32		0x00000000
0x1060	D1_R2_C_CTRL0	RW	32		0x0000FFFF
0x1064	D1_R2_C_CTRL1	RW	32		0x00000000
0x1068	D1_R2_C_STATUS0	RO	32		0x00000000
0x106C	D1_R2_C_STATUS1	RO	32		0x00000000
0x1070	D1_R2_C_TIMSTAMP0	RO	32		0x00000000
0x1074	D1_R2_C_TIMSTAMP1	RO	32		0x00000000
0x1080	N0_R1_C_CTRL0	RW	32		0x0000FFFF
0x1084	N0_R1_C_CTRL1	RW	32		0x00000000

0x1088	N0_R1_C_STATUS0	RO	32		0x00000000
0x108C	N0_R1_C_STATUS1	RO	32		0x00000000
0x1090	N0_R1_C_TIMESTAMP0	RO	32		0x00000000
0x1094	N0_R1_C_TIMESTAMP1	RO	32		0x00000000
0x10A0	N1_R1_C_CTRL0	RW	32		0x0000FFFF
0x10A4	N1_R1_C_CTRL1	RW	32		0x00000000
0x10A8	N1_R1_C_STATUS0	RO	32		0x00000000
0x10AC	N1_R1_C_STATUS1	RO	32		0x00000000
0x10B0	N1_R1_C_TIMESTAMP0	RO	32		0x00000000
0x10B4	N1_R1_C_TIMESTAMP1	RO	32		0x00000000
0x10C0	N2_R1_C_CTRL0	RW	32		0x0000FFFF
0x10C4	N2_R1_C_CTRL1	RW	32		0x00000000
0x10C8	N2_R1_C_STATUS0	RO	32		0x00000000
0x10CC	N2_R1_C_STATUS1	RO	32		0x00000000
0x10D0	N2_R1_C_TIMESTAMP0	RO	32		0x00000000
0x10D4	N2_R1_C_TIMESTAMP1	RO	32		0x00000000
0x10E0	N3_R1_C_CTRL0	RW	32		0x0000FFFF
0x10E4	N3_R1_C_CTRL1	RW	32		0x00000000
0x10E8	N3_R1_C_STATUS0	RO	32		0x00000000
0x10EC	N3_R1_C_STATUS1	RO	32		0x00000000
0x10F0	N3_R1_C_TIMESTAMP0	RO	32		0x00000000
0x10F4	N3_R1_C_TIMESTAMP1	RO	32		0x00000000
0x1100	N4_R1_C_CTRL0	RW	32		0x0000FFFF
0x1104	N4_R1_C_CTRL1	RW	32		0x00000000
0x1108	N4_R1_C_STATUS0	RO	32		0x00000000
0x110C	N4_R1_C_STATUS1	RO	32		0x00000000
0x1110	N4_R1_C_TIMESTAMP0	RO	32		0x00000000
0x1114	N4_R1_C_TIMESTAMP1	RO	32		0x00000000
0x1120	N5_R1_C_CTRL0	RW	32		0x0000FFFF
0x1124	N5_R1_C_CTRL1	RW	32		0x00000000
0x1128	N5_R1_C_STATUS0	RO	32		0x00000000
0x112C	N5_R1_C_STATUS1	RO	32		0x00000000
0x1130	N5_R1_C_TIMESTAMP0	RO	32		0x00000000
0x1134	N5_R1_C_TIMESTAMP1	RO	32		0x00000000
0x1140	N6_R1_C_CTRL0	RW	32		0x0000FFFF
0x1144	N6_R1_C_CTRL1	RW	32		0x00000000
0x1148	N6_R1_C_STATUS0	RO	32		0x00000000
0x114C	N6_R1_C_STATUS1	RO	32		0x00000000

0x1150	N6_R1_C_TIMSTAMP0	RO	32		0x00000000
0x1154	N6_R1_C_TIMSTAMP1	RO	32		0x00000000
0x1160	N7_R1_C_CTRL0	RW	32		0x0000FFFF
0x1164	N7_R1_C_CTRL1	RW	32		0x00000000
0x1168	N7_R1_C_STATUS0	RO	32		0x00000000
0x116C	N7_R1_C_STATUS1	RO	32		0x00000000
0x1170	N7_R1_C_TIMSTAMP0	RO	32		0x00000000
0x1174	N7_R1_C_TIMSTAMP1	RO	32		0x00000000
0x1180	D0_R3_CH_CTRL0	RW	32		0x0000FFFF
0x1184	D0_R3_CH_CTRL1	RW	32		0x00000000
0x1188	D0_R3_CH_STATUS0	RO	32		0x00000000
0x118C	D0_R3_CH_STATUS1	RO	32		0x00000000
0x1190	D0_R3_CH_TIMSTAMP0	RO	32		0x00000000
0x1194	D0_R3_CH_TIMSTAMP1	RO	32		0x00000000
0x11A0	D1_R3_CH_CTRL0	RW	32		0x0000FFFF
0x11A4	D1_R3_CH_CTRL1	RW	32		0x00000000
0x11A8	D1_R3_CH_STATUS0	RO	32		0x00000000
0x11AC	D1_R3_CH_STATUS1	RO	32		0x00000000
0x11B0	D1_R3_CH_TIMSTAMP0	RO	32		0x00000000
0x11B4	D1_R3_CH_TIMSTAMP1	RO	32		0x00000000
0x11C0	D0_R0_H_CTRL0	RW	32		0x0000FFFF
0x11C4	D0_R0_H_CTRL1	RW	32		0x00000000
0x11C8	D0_R0_H_STATUS0	RO	32		0x00000000
0x11CC	D0_R0_H_STATUS1	RO	32		0x00000000
0x11D0	D0_R0_H_TIMSTAMP0	RO	32		0x00000000
0x11D4	D0_R0_H_TIMSTAMP1	RO	32		0x00000000
0x11E0	D1_R0_H_CTRL0	RW	32		0x0000FFFF
0x11E4	D1_R0_H_CTRL1	RW	32		0x00000000
0x11E8	D1_R0_H_STATUS0	RO	32		0x00000000
0x11EC	D1_R0_H_STATUS1	RO	32		0x00000000
0x11F0	D1_R0_H_TIMSTAMP0	RO	32		0x00000000
0x11F4	D1_R0_H_TIMSTAMP1	RO	32		0x00000000
0x1200	N0_R0_H_CTRL0	RW	32		0x0000FFFF
0x1204	N0_R0_H_CTRL1	RW	32		0x00000000
0x1208	N0_R0_H_STATUS0	RO	32		0x00000000
0x120C	N0_R0_H_STATUS1	RO	32		0x00000000
0x1210	N0_R0_H_TIMSTAMP0	RO	32		0x00000000
0x1214	N0_R0_H_TIMSTAMP1	RO	32		0x00000000

0x1220	N1_R0_H_CTRL0	RW	32		0x0000FFFF
0x1224	N1_R0_H_CTRL1	RW	32		0x00000000
0x1228	N1_R0_H_STATUS0	RO	32		0x00000000
0x122C	N1_R0_H_STATUS1	RO	32		0x00000000
0x1230	N1_R0_H_TIMESTAMP0	RO	32		0x00000000
0x1234	N1_R0_H_TIMESTAMP1	RO	32		0x00000000
0x1240	N2_R0_H_CTRL0	RW	32		0x0000FFFF
0x1244	N2_R0_H_CTRL1	RW	32		0x00000000
0x1248	N2_R0_H_STATUS0	RO	32		0x00000000
0x124C	N2_R0_H_STATUS1	RO	32		0x00000000
0x1250	N2_R0_H_TIMESTAMP0	RO	32		0x00000000
0x1254	N2_R0_H_TIMESTAMP1	RO	32		0x00000000
0x1260	N3_R0_H_CTRL0	RW	32		0x0000FFFF
0x1264	N3_R0_H_CTRL1	RW	32		0x00000000
0x1268	N3_R0_H_STATUS0	RO	32		0x00000000
0x126C	N3_R0_H_STATUS1	RO	32		0x00000000
0x1270	N3_R0_H_TIMESTAMP0	RO	32		0x00000000
0x1274	N3_R0_H_TIMESTAMP1	RO	32		0x00000000
0x1280	N4_R0_H_CTRL0	RW	32		0x0000FFFF
0x1284	N4_R0_H_CTRL1	RW	32		0x00000000
0x1288	N4_R0_H_STATUS0	RO	32		0x00000000
0x128C	N4_R0_H_STATUS1	RO	32		0x00000000
0x1290	N4_R0_H_TIMESTAMP0	RO	32		0x00000000
0x1294	N4_R0_H_TIMESTAMP1	RO	32		0x00000000
0x12A0	N5_R0_H_CTRL0	RW	32		0x0000FFFF
0x12A4	N5_R0_H_CTRL1	RW	32		0x00000000
0x12A8	N5_R0_H_STATUS0	RO	32		0x00000000
0x12AC	N5_R0_H_STATUS1	RO	32		0x00000000
0x12B0	N5_R0_H_TIMESTAMP0	RO	32		0x00000000
0x12B4	N5_R0_H_TIMESTAMP1	RO	32		0x00000000
0x12C0	N6_R0_H_CTRL0	RW	32		0x0000FFFF
0x12C4	N6_R0_H_CTRL1	RW	32		0x00000000
0x12C8	N6_R0_H_STATUS0	RO	32		0x00000000
0x12CC	N6_R0_H_STATUS1	RO	32		0x00000000
0x12D0	N6_R0_H_TIMESTAMP0	RO	32		0x00000000
0x12D4	N6_R0_H_TIMESTAMP1	RO	32		0x00000000
0x12E0	N7_R0_H_CTRL0	RW	32		0x0000FFFF
0x12E4	N7_R0_H_CTRL1	RW	32		0x00000000

0x12E8	N7_R0_H_STATUS0	RO	32		0x00000000
0x12EC	N7_R0_H_STATUS1	RO	32		0x00000000
0x12F0	N7_R0_H_TIMESTAMP0	RO	32		0x00000000
0x12F4	N7_R0_H_TIMESTAMP1	RO	32		0x00000000
0x1300	V0_R_H_CTRL0	RW	32		0x0000FFFF
0x1304	V0_R_H_CTRL1	RW	32		0x00000000
0x1308	V0_R_H_STATUS0	RO	32		0x00000000
0x130C	V0_R_H_STATUS1	RO	32		0x00000000
0x1310	V0_R_H_TIMESTAMP0	RO	32		0x00000000
0x1314	V0_R_H_TIMESTAMP1	RO	32		0x00000000
0x1320	V1_R_H_CTRL0	RW	32		0x0000FFFF
0x1324	V1_R_H_CTRL1	RW	32		0x00000000
0x1328	V1_R_H_STATUS0	RO	32		0x00000000
0x132C	V1_R_H_STATUS1	RO	32		0x00000000
0x1330	V1_R_H_TIMESTAMP0	RO	32		0x00000000
0x1334	V1_R_H_TIMESTAMP1	RO	32		0x00000000
0x1340	V2_R_H_CTRL0	RW	32		0x0000FFFF
0x1344	V2_R_H_CTRL1	RW	32		0x00000000
0x1348	V2_R_H_STATUS0	RO	32		0x00000000
0x134C	V2_R_H_STATUS1	RO	32		0x00000000
0x1350	V2_R_H_TIMESTAMP0	RO	32		0x00000000
0x1354	V2_R_H_TIMESTAMP1	RO	32		0x00000000
0x1360	V3_R_H_CTRL0	RW	32		0x0000FFFF
0x1364	V3_R_H_CTRL1	RW	32		0x00000000
0x1368	V3_R_H_STATUS0	RO	32		0x00000000
0x136C	V3_R_H_STATUS1	RO	32		0x00000000
0x1370	V3_R_H_TIMESTAMP0	RO	32		0x00000000
0x1374	V3_R_H_TIMESTAMP1	RO	32		0x00000000
0x1380	V4_R_H_CTRL0	RW	32		0x0000FFFF
0x1384	V4_R_H_CTRL1	RW	32		0x00000000
0x1388	V4_R_H_STATUS0	RO	32		0x00000000
0x138C	V4_R_H_STATUS1	RO	32		0x00000000
0x1390	V4_R_H_TIMESTAMP0	RO	32		0x00000000
0x1394	V4_R_H_TIMESTAMP1	RO	32		0x00000000
0x13A0	V5_R_H_CTRL0	RW	32		0x0000FFFF
0x13A4	V5_R_H_CTRL1	RW	32		0x00000000
0x13A8	V5_R_H_STATUS0	RO	32		0x00000000
0x13AC	V5_R_H_STATUS1	RO	32		0x00000000

0x13B0	V5_R_H_TIMSTAMP0	RO	32		0x00000000
0x13B4	V5_R_H_TIMSTAMP1	RO	32		0x00000000
0x13C0	V6_R_H_CTRL0	RW	32		0x0000FFFF
0x13C4	V6_R_H_CTRL1	RW	32		0x00000000
0x13C8	V6_R_H_STATUS0	RO	32		0x00000000
0x13CC	V6_R_H_STATUS1	RO	32		0x00000000
0x13D0	V6_R_H_TIMSTAMP0	RO	32		0x00000000
0x13D4	V6_R_H_TIMSTAMP1	RO	32		0x00000000
0x13E0	V7_R_H_CTRL0	RW	32		0x0000FFFF
0x13E4	V7_R_H_CTRL1	RW	32		0x00000000
0x13E8	V7_R_H_STATUS0	RO	32		0x00000000
0x13EC	V7_R_H_STATUS1	RO	32		0x00000000
0x13F0	V7_R_H_TIMSTAMP0	RO	32		0x00000000
0x13F4	V7_R_H_TIMSTAMP1	RO	32		0x00000000
0x1400	V8_R_H_CTRL0	RW	32		0x0000FFFF
0x1404	V8_R_H_CTRL1	RW	32		0x00000000
0x1408	V8_R_H_STATUS0	RO	32		0x00000000
0x140C	V8_R_H_STATUS1	RO	32		0x00000000
0x1410	V8_R_H_TIMSTAMP0	RO	32		0x00000000
0x1414	V8_R_H_TIMSTAMP1	RO	32		0x00000000
0x1420	V9_R_H_CTRL0	RW	32		0x0000FFFF
0x1424	V9_R_H_CTRL1	RW	32		0x00000000
0x1428	V9_R_H_STATUS0	RO	32		0x00000000
0x142C	V9_R_H_STATUS1	RO	32		0x00000000
0x1430	V9_R_H_TIMSTAMP0	RO	32		0x00000000
0x1434	V9_R_H_TIMSTAMP1	RO	32		0x00000000
0x1C00	DECI_PARTITION_SEL	RW	32		0x00000000

3.9.12.10.1 {0x0} D0_W0_S_CTRL0 Details

Table SCU (Sensor Control Unit)-330

Local Address: 0x0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits	Name			Type	Reset Value			Description																							
31..16	FIFO_START_OFST			RW	0xA000			Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																							
15..0	FIFO_PARTITION_SIZE			RW	0x0000			Partition size -1 Sets partition size minus 1. (by Sample unit)																							

3.9.12.10.2 {0x4} D0_W0_S_CTRL1 Details

Table SCU (Sensor Control Unit)-331

Local Address: 0x4																						Register Type: RW (read/write)													
																						Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL				ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE			
Bits	Name			Type	Reset Value	Description																													
31..17	Reserved			RO	0x0000	Reserved																													
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																													
15..13	Reserved			RO	0x0	Reserved																													
12	ENABLE_ADC_INTERVAL			RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																													
11..8	ADC_INTERVAL			RW	0x0	When ENABLE_ADC_INTERVAL is “1”, ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																													
7..5	Reserved			RO	0x0	Reserved																													
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																													
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																													

3.9.12.10.3 {0x8} D0_W0_S_STATUS Details

Table SCU (Sensor Control Unit)-332

Local Address: 0x8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.4 {0xC} D0_W0_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-333

Local Address: 0xC																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_TIMESTAMP_MSB																															
Bits	Name							Type	Reset Value							Description															
31..0	LATEST_TIMESTAMP_MSB							RO	0x00000000							Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO by second unit															

3.9.12.10.5 {0x10} D0_W0_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-334

Local Address: 0x10																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																LATEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.6 {0x20} D0_W1_S_CTRL0 Details

Table SCU (Sensor Control Unit)-335

Local Address: 0x20																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.7 {0x24} D0_W1_S_CTRL1 Details

Table SCU (Sensor Control Unit)-336

Local Address: 0x24																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_RESET	Reserved										OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits		Name				Type	Reset Value				Description																				
31..17		Reserved				RO	0x0000				Reserved																				
16		FIFO_RESET				WO	0x0				Reset of the FIFO Clears the writing pointer to “0”																				
15..5		Reserved				RO	0x000				Reserved																				
4		OVERWRITE_IF_FULL				RW	0x0				OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																				
3..0		FIFO_SAMPLE_SIZE				RW	0x0				Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																				

3.9.12.10.8 {0x28} D0_W1_S_STATUS Details

Table SCU (Sensor Control Unit)-337

Local Address: 0x28																				Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
FIFO_WRITE_PTR																Reserved										FIFO_WRITE_PHASE									
Bits	Name				Type	Reset Value				Description																									
31..16	FIFO_WRITE_PTR				RO	0x0000				Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4	Reserved				RO	0x000				Reserved																									
3..0	FIFO_WRITE_PHASE				RO	0x0				Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.9 {0x2C} D0_W1_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-338

Local Address: 0x2C																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.10 {0x30} D0_W1_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-339

Local Address: 0x30																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name					Type	Reset Value					Description																		
31..15		Reserved					RO	0x00000					Reserved																		
14..0		LATEST_TIMESTAMP_LSB					RO	0x0000					Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.11 {0x40} D0_W2_S_CTRL0 Details

Table SCU (Sensor Control Unit)-340

Local Address: 0x40																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.12 {0x44} D0_W2_S_CTRL1 Details

Table SCU (Sensor Control Unit)-341

Local Address: 0x44														Register Type: RW (read/write)																				
														Reset Value: 0x00000000																				
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0										
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE
Bits		Name				Type		Reset Value				Description																						
31..17		Reserved				RO		0x0000				Reserved																						
16		FIFO_RESET				WO		0x0				Reset of the FIFO Clears the writing pointer to “0”																						
15..5		Reserved				RO		0x000				Reserved																						
4		OVERWRITE_IF_FULL				RW		0x0				OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																						
3..0		FIFO_SAMPLE_SIZE				RW		0x0				Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																						

3.9.12.10.13 {0x48} D0_W2_S_STATUS Details

Table SCU (Sensor Control Unit)-342

Local Address: 0x48																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits				Name				Type				Reset Value				Description																			
31..16				FIFO_WRITE_PTR				RO				0x0000				Writing pointer address of the FIFO The start address where the next data is written by Byte unit																			
15..4				Reserved				RO				0x000				Reserved																			
3..0				FIFO_WRITE_PHASE				RO				0x0				Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																			

3.9.12.10.14 {0x4C} D0_W2_S_TIMESTAMP0 Details

Table SCU (Sensor Control Unit)-343

Local Address: 0x4C																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.15 {0x50} D0_W2_S_TIMESTAMP1 Details

Table SCU (Sensor Control Unit)-344

Local Address: 0x50																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name					Type	Reset Value					Description																		
31..15		Reserved					RO	0x00000					Reserved																		
14..0		LATEST_TIMESTAMP_LSB					RO	0x0000					Latest time stamp (second after the decimal point The start address where the next data is written by Byte unit																		

3.9.12.10.16 {0x60} D0_W3_S_CTRL0 Details

Table SCU (Sensor Control Unit)-345

Local Address: 0x60																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.17 {0x64} D0_W3_S_CTRL1 Details

Table SCU (Sensor Control Unit)-346

Local Address: 0x64																		Register Type: RW (read/write)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_RESET	Reserved											OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE		
Bits		Name				Type		Reset Value				Description																			
31..17		Reserved				RO		0x0000				Reserved																			
16		FIFO_RESET				WO		0x0				Reset of the FIFO Clears the writing pointer to “0”																			
15..5		Reserved				RO		0x000				Reserved																			
4		OVERWRITE_IF_FULL				RW		0x0				OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																			
3..0		FIFO_SAMPLE_SIZE				RW		0x0				Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																			

3.9.12.10.18 {0x68} D0_W3_S_STATUS Details

Table SCU (Sensor Control Unit)-347

Local Address: 0x68																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.19 {0x6C} D0_W3_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-348

Local Address: 0x6C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.20 {0x70} D0_W3_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-349

Local Address: 0x70																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.21 {0x80} D1_W0_S_CTRL0 Details

Table SCU (Sensor Control Unit)-350

Local Address: 0x80																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.22 {0x84} D1_W0_S_CTRL1 Details

Table SCU (Sensor Control Unit)-351

Local Address: 0x84																Register Type: RW (read/write) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																FIFO_RESET	Reserved			ENABLE_ADC_INTERVAL			ADC_INTERVAL					Reserved			OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE		
Bits	Name							Type	Reset Value	Description																									
31..17	Reserved							RO	0x0000	Reserved																									
16	FIFO_RESET							WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																									
15..13	Reserved							RO	0x0	Reserved																									
12	ENABLE_ADC_INTERVAL							RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																									
11..8	ADC_INTERVAL							RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																									
7..5	Reserved							RO	0x0	Reserved																									
4	OVERWRITE_IF_FULL							RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																									
3..0	FIFO_SAMPLE_SIZE							RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																									

3.9.12.10.23 {0x88} D1_W0_S_STATUS Details

Table SCU (Sensor Control Unit)-352

Local Address: 0x88																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.24 {0x8C} D1_W0_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-353

Local Address: 0x8C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.25 {0x90} D1_W0_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-354

Local Address: 0x90																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.26 {0xA0} D1_W1_S_CTRL0 Details

Table SCU (Sensor Control Unit)-355

Local Address: 0xA0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.27 {0xA4} D1_W1_S_CTRL1 Details

Table SCU (Sensor Control Unit)-356

Local Address: 0xA4																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_RESET	Reserved										OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits		Name				Type	Reset Value				Description																				
31..17		Reserved				RO	0x0000				Reserved																				
16		FIFO_RESET				WO	0x0				Reset of the FIFO Clears the writing pointer to “0”																				
15..5		Reserved				RO	0x000				Reserved																				
4		OVERWRITE_IF_FULL				RW	0x0				OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																				
3..0		FIFO_SAMPLE_SIZE				RW	0x0				Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																				

3.9.12.10.28 {0xA8} D1_W1_S_STATUS Details

Table SCU (Sensor Control Unit)-357

Local Address: 0xA8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type	Reset Value	Description																							
31..16		FIFO_WRITE_PTR				RO	0x0000	Writing pointer address of the FIFO The start address where the next data is written by Byte unit																							
15..4		Reserved				RO	0x000	Reserved																							
3..0		FIFO_WRITE_PHASE				RO	0x0	Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																							

3.9.12.10.29 {0xAC} D1_W1_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-358

Local Address: 0xAC																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.30 {0xB0} D1_W1_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-359

Local Address: 0xB0																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.31 {0xC0} D1_W2_S_CTRL0 Details

Table SCU (Sensor Control Unit)-360

Local Address: 0xC0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.32 {0xC4} D1_W2_S_CTRL1 Details

Table SCU (Sensor Control Unit)-361

Local Address: 0xC4														Register Type: RW (read/write) Reset Value: 0x00000000																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits		Name		Type		Reset Value		Description																													
31..17		Reserved		RO		0x0000		Reserved																													
16		FIFO_RESET		WO		0x0		Reset of the FIFO Clears the writing pointer to “0”																													
15..5		Reserved		RO		0x000		Reserved																													
4		OVERWRITE_IF_FULL		RW		0x0		OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																													
3..0		FIFO_SAMPLE_SIZE		RW		0x0		Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																													

3.9.12.10.33 {0xC8} D1_W2_S_STATUS Details

Table SCU (Sensor Control Unit)-362

Local Address: 0xC8																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																									
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4		Reserved				RO		0x000		Reserved																									
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.34 {0xCC} D1_W2_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-363

Local Address: 0xCC																				Register Type: RO (read only) Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.35 {0xD0} D1_W2_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-364

Local Address: 0xD0																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.36 {0xE0} D1_W3_S_CTRL0 Details

Table SCU (Sensor Control Unit)-365

Local Address: 0xE0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.37 {0xE4} D1_W3_S_CTRL1 Details

Table SCU (Sensor Control Unit)-366

Local Address: 0xE4																Register Type: RW (read/write) Reset Value: 0x00000000																		
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0										
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE
Bits	Name		Type	Reset Value	Description																													
31..17	Reserved		RO	0x0000	Reserved																													
16	FIFO_RESET		WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																													
15..5	Reserved		RO	0x000	Reserved																													
4	OVERWRITE_IF_FULL		RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																													
3..0	FIFO_SAMPLE_SIZE		RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																													

3.9.12.10.38 {0xE8} D1_W3_S_STATUS Details

Table SCU (Sensor Control Unit)-367

Local Address: 0xE8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.39 {0xEC} D1_W3_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-368

Local Address: 0xEC																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.40 {0xF0} D1_W3_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-369

Local Address: 0xF0																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.41 {0x100} N0_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-370

Local Address: 0x100																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.42 {0x104} N0_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-371

Local Address: 0x104																				Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL		ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE					
Bits	Name							Type	Reset Value	Description																									
31..17	Reserved							RO	0x0000	Reserved																									
16	FIFO_RESET							WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																									
15..13	Reserved							RO	0x0	Reserved																									
12	ENABLE_ADC_INTERVAL							RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																									
11..8	ADC_INTERVAL							RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																									
7..5	Reserved							RO	0x0	Reserved																									
4	OVERWRITE_IF_FULL							RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																									
3..0	FIFO_SAMPLE_SIZE							RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																									

3.9.12.10.43 {0x108} N0_W_S_STATUS Details

Table SCU (Sensor Control Unit)-372

Local Address: 0x108																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.44 {0x10C} N0_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-373

Local Address: 0x10C																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.45 {0x110} N0_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-374

Local Address: 0x110																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		LATEST_TIMESTAMP_LSB				RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.46 {0x120} N1_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-375

Local Address: 0x120																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.47 {0x124} N1_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-376

Local Address: 0x124																Register Type: RW (read/write) Reset Value: 0x00000000																								
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																
Reserved																FIFO_RESET	Reserved				ENABLE_ADC_INTERVAL				ADC_INTERVAL				Reserved				OVERWRITE_IF_FULL				FIFO_SAMPLE_SIZE			
Bits	Name				Type	Reset Value		Description																																
31..17		Reserved				RO	0x0000		Reserved																															
16		FIFO_RESET				WO	0x0		Reset of the FIFO Clears the writing pointer to “0”																															
15..13		Reserved				RO	0x0		Reserved																															
12		ENABLE_ADC_INTERVAL				RW	0x0		Uses ADC_INTERVAL instead of PRE_DIVIDER																															
11..8		ADC_INTERVAL				RW	0x0		ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																															
7..5		Reserved				RO	0x0		Reserved																															
4		OVERWRITE_IF_FULL				RW	0x0		OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																															
3..0		FIFO_SAMPLE_SIZE				RW	0x0		Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																															

3.9.12.10.48 {0x128} N1_W_S_STATUS Details

Table SCU (Sensor Control Unit)-377

Local Address: 0x128																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved										FIFO_WRITE_PHASE					
Bits		Name						Type	Reset Value						Description																
31..16		FIFO_WRITE_PTR						RO	0x0000						Writing pointer address of the FIFO The start address where the next data is written by Byte unit																
15..4		Reserved						RO	0x000						Reserved																
3..0		FIFO_WRITE_PHASE						RO	0x0						Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																

3.9.12.10.49 {0x12C} N1_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-378

Local Address: 0x12C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.50 {0x130} N1_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-379

Local Address: 0x130																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name					Type	Reset Value					Description																		
31..15		Reserved					RO	0x00000					Reserved																		
14..0		LATEST_TIMESTAMP_LSB					RO	0x0000					Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.51 {0x140} N2_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-380

Local Address: 0x140																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.52 {0x144} N2_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-381

Local Address: 0x144																Register Type: RW (read/write) Reset Value: 0x00000000																								
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																
Reserved																FIFO_RESET	Reserved				ENABLE_ADC_INTERVAL				ADC_INTERVAL				Reserved				OVERWRITE_IF_FULL				FIFO_SAMPLE_SIZE			
Bits	Name			Type	Reset Value	Description																																		
31..17	Reserved			RO	0x0000	Reserved																																		
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																		
15..13	Reserved			RO	0x0	Reserved																																		
12	ENABLE_ADC_INTERVAL			RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																																		
11..8	ADC_INTERVAL			RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																																		
7..5	Reserved			RO	0x0	Reserved																																		
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																																		
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																		

3.9.12.10.53 {0x148} N2_W_S_STATUS Details

Table SCU (Sensor Control Unit)-382

Local Address: 0x148																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.54 {0x14C} N2_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-383

Local Address: 0x14C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.55 {0x150} N2_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-384

Local Address: 0x150																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																LATEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.56 {0x160} N3_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-385

Local Address: 0x160																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.57 {0x164} N3_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-386

Local Address: 0x164																				Register Type: RW (read/write)													
																				Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL		ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE			
Bits	Name							Type	Reset Value	Description																							
31..17	Reserved							RO	0x0000	Reserved																							
16	FIFO_RESET							WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																							
15..13	Reserved							RO	0x0	Reserved																							
12	ENABLE_ADC_INTERVAL							RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																							
11..8	ADC_INTERVAL							RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																							
7..5	Reserved							RO	0x0	Reserved																							
4	OVERWRITE_IF_FULL							RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																							
3..0	FIFO_SAMPLE_SIZE							RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																							

3.9.12.10.58 {0x168} N3_W_S_STATUS Details

Table SCU (Sensor Control Unit)-387

Local Address: 0x168																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.59 {0x16C} N3_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-388

Local Address: 0x16C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.60 {0x170} N3_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-389

Local Address: 0x170																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.61 {0x180} N4_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-390

Local Address: 0x180																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.62 {0x184} N4_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-391

Local Address: 0x184																				Register Type: RW (read/write)													
																				Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL		ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE			
Bits	Name							Type	Reset Value	Description																							
31..17	Reserved							RO	0x0000	Reserved																							
16	FIFO_RESET							WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																							
15..13	Reserved							RO	0x0	Reserved																							
12	ENABLE_ADC_INTERVAL							RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																							
11..8	ADC_INTERVAL							RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																							
7..5	Reserved							RO	0x0	Reserved																							
4	OVERWRITE_IF_FULL							RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																							
3..0	FIFO_SAMPLE_SIZE							RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																							

3.9.12.10.63 {0x188} N4_W_S_STATUS Details

Table SCU (Sensor Control Unit)-392

Local Address: 0x188																Register Type: RO (read only) Reset Value: 0x00000000																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																									
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4		Reserved				RO		0x000		Reserved																									
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.64 {0x18C} N4_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-393

Local Address: 0x18C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.65 {0x190} N4_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-394

Local Address: 0x190																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved															LATEST_TIMESTAMP_LSB																				
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.66 {0x1A0} N5_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-395

Local Address: 0x1A0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.67 {0x1A4} N5_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-396

Local Address: 0x1A4																				Register Type: RW (read/write)													
																				Reset Value: 0x00000000													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL		ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE			
Bits	Name			Type	Reset Value	Description																											
31..17	Reserved			RO	0x0000	Reserved																											
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																											
15..13	Reserved			RO	0x0	Reserved																											
12	ENABLE_ADC_INTERVAL			RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																											
11..8	ADC_INTERVAL			RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																											
7..5	Reserved			RO	0x0	Reserved																											
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																											
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																											

3.9.12.10.68 {0x1A8} N5_W_S_STATUS Details

Table SCU (Sensor Control Unit)-397

Local Address: 0x1A8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.69 {0x1AC} N5_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-398

Local Address: 0x1AC																				Register Type: RO (read only) Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.70 {0x1B0} N5_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-399

Local Address: 0x1B0																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name				Type	Reset Value				Description																								
31..15		Reserved				RO	0x00000				Reserved																								
14..0		LATEST_TIMESTAMP_LSB				RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																								

3.9.12.10.71 {0x1C0} N6_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-400

Local Address: 0x1C0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.72 {0x1C4} N6_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-401

Local Address: 0x1C4																				Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL				ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE			
Bits	Name							Type	Reset Value	Description																									
31..17		Reserved							RO	0x0000	Reserved																								
16		FIFO_RESET							WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																								
15..13		Reserved							RO	0x0	Reserved																								
12		ENABLE_ADC_INTERVAL							RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																								
11..8		ADC_INTERVAL							RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																								
7..5		Reserved							RO	0x0	Reserved																								
4		OVERWRITE_IF_FULL							RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																								
3..0		FIFO_SAMPLE_SIZE							RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																								

3.9.12.10.73 {0x1C8} N6_W_S_STATUS Details

Table SCU (Sensor Control Unit)-402

Local Address: 0x1C8																				Register Type: RO (read only) Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved										FIFO_WRITE_PHASE					
Bits	Name				Type	Reset Value				Description																					
31..16	FIFO_WRITE_PTR				RO	0x0000				Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4	Reserved				RO	0x000				Reserved																					
3..0	FIFO_WRITE_PHASE				RO	0x0				Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.74 {0x1CC} N6_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-403

Local Address: 0x1CC																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.75 {0x1D0} N6_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-404

Local Address: 0x1D0																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		LATEST_TIMESTAMP_LSB				RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.76 {0x1E0} N7_W_S_CTRL0 Details

Table SCU (Sensor Control Unit)-405

Local Address: 0x1E0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.77 {0x1E4} N7_W_S_CTRL1 Details

Table SCU (Sensor Control Unit)-406

Local Address: 0x1E4																				Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved																FIFO_RESET		Reserved		ENABLE_ADC_INTERVAL		ADC_INTERVAL				Reserved		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE					
Bits	Name			Type	Reset Value	Description																													
31..17	Reserved			RO	0x0000	Reserved																													
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																													
15..13	Reserved			RO	0x0	Reserved																													
12	ENABLE_ADC_INTERVAL			RW	0x0	Uses ADC_INTERVAL instead of PRE_DIVIDER																													
11..8	ADC_INTERVAL			RW	0x0	ADC_INTERVAL is used as a sampling interval instead of PRE_DIVIDER. Note: ADC_INTERVAL must be bigger than 1.																													
7..5	Reserved			RO	0x0	Reserved																													
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																													
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																													

3.9.12.10.78 {0x1E8} N7_W_S_STATUS Details

Table SCU (Sensor Control Unit)-407

Local Address: 0x1E8																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																									
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4		Reserved				RO		0x000		Reserved																									
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.79 {0x1EC} N7_W_S_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-408

Local Address: 0x1EC																						Register Type: RO (read only) Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.80 {0x1F0} N7_W_S_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-409

Local Address: 0x1F0																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																LATEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.81 {0x200} V0_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-410

Local Address: 0x200																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.82 {0x204} V0_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-411

Local Address: 0x204																Register Type: RW (read/write)																		
																Reset Value: 0x00000000																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE
Bits	Name				Type	Reset Value	Description																											
31..17	Reserved				RO	0x0000	Reserved																											
16	FIFO_RESET				WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																											
15..5	Reserved				RO	0x000	Reserved																											
4	OVERWRITE_IF_FULL				RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																											
3..0	FIFO_SAMPLE_SIZE				RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																											

3.9.12.10.83 {0x208} V0_W_C_STATUS Details

Table SCU (Sensor Control Unit)-412

Local Address: 0x208																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits	Name							Type	Reset Value	Description																					
31..16	FIFO_WRITE_PTR							RO	0x0000	Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4	Reserved							RO	0x000	Reserved																					
3..0	FIFO_WRITE_PHASE							RO	0x0	Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.84 {0x20C} V0_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-413

Local Address: 0x20C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.85 {0x210} V0_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-414

Local Address: 0x210																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.86 {0x214} V0_W_C_TIMSTAMP_SET0 Details

Table SCU (Sensor Control Unit)-415

Local Address: 0x214																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.87 {0x218} V0_W_C_TIMSTAMP_SET1 Details

Table SCU (Sensor Control Unit)-416

Local Address: 0x218																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.88 {0x220} V1_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-417

Local Address: 0x220																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.89 {0x224} V1_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-418

Local Address: 0x224														Register Type: RW (read/write) Reset Value: 0x00000000																																									
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8														7 6 5 4 3 2 1 0													
Reserved																		FIFO_RESET	Reserved																		OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE																	
Bits	Name			Type	Reset Value	Description																																																	
31..17	Reserved			RO	0x0000	Reserved																																																	
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																																	
15..5	Reserved			RO	0x000	Reserved																																																	
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO full 0: does not overwrite 1: overwrites																																																	
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																																	

3.9.12.10.90 {0x228} V1_W_C_STATUS Details

Table SCU (Sensor Control Unit)-419

Local Address: 0x228																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.91 {0x22C} V1_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-420

Local Address: 0x22C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.92 {0x230} V1_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-421

Local Address: 0x230																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.93 {0x234} V1_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-422

Local Address: 0x234																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.94 {0x238} V1_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-423

Local Address: 0x238																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.95 {0x240} V2_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-424

Local Address: 0x240																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name		Type	Reset Value		Description																								
31..16		FIFO_START_OFST		RW	0xA000		Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																								
15..0		FIFO_PARTITION_SIZE		RW	0x0000		Partition size -1 Sets partition size minus 1. (by Sample unit)																								

3.9.12.10.96 {0x244} V2_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-425

Local Address: 0x244																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														FIFO_RESET	Reserved										OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE					
Bits		Name		Type	Reset Value		Description																								
31..17		Reserved		RO	0x0000		Reserved																								
16		FIFO_RESET		WO	0x0		Reset of the FIFO Clears the writing pointer to “0”																								
15..5		Reserved		RO	0x000		Reserved																								
4		OVERWRITE_IF_FULL		RW	0x0		OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																								
3..0		FIFO_SAMPLE_SIZE		RW	0x0		Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																								

3.9.12.10.97 {0x248} V2_W_C_STATUS Details

Table SCU (Sensor Control Unit)-426

Local Address: 0x248																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.98 {0x24C} V2_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-427

Local Address: 0x24C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.99 {0x250} V2_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-428

Local Address: 0x250																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.100 {0x254} V2_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-429

Local Address: 0x254																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.101 {0x258} V2_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-430

Local Address: 0x258																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.102 {0x260} V3_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-431

Local Address: 0x260																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.103 {0x264} V3_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-432

Local Address: 0x264																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits	Name		Type	Reset Value	Description																																
31..17	Reserved		RO	0x0000	Reserved																																
16	FIFO_RESET		WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																
15..5	Reserved		RO	0x000	Reserved																																
4	OVERWRITE_IF_FULL		RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																																
3..0	FIFO_SAMPLE_SIZE		RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																

3.9.12.10.104 {0x268} V3_W_C_STATUS Details

Table SCU (Sensor Control Unit)-433

Local Address: 0x268																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.105 {0x26C} V3_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-434

Local Address: 0x26C																				Register Type: RO (read only) Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.106 {0x270} V3_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-435

Local Address: 0x270																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved															LATEST_TIMESTAMP_LSB																				
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.107 {0x274} V3_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-436

Local Address: 0x274																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.108 {0x278} V3_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-437

Local Address: 0x278																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																Reserved															
	TIME_STAMP_INTERVAL																LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.109 {0x280} V4_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-438

Local Address: 0x280																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_START_OFST				RW		0xA000		Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																					
15..0		FIFO_PARTITION_SIZE				RW		0x0000		Partition size -1 Sets partition size minus 1. (by Sample unit)																					

3.9.12.10.110 {0x284} V4_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-439

Local Address: 0x284																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits	Name		Type	Reset Value	Description																																
31..17	Reserved		RO	0x0000	Reserved																																
16	FIFO_RESET		WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																
15..5	Reserved		RO	0x000	Reserved																																
4	OVERWRITE_IF_FULL		RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																																
3..0	FIFO_SAMPLE_SIZE		RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																

3.9.12.10.111 {0x288} V4_W_C_STATUS Details

Table SCU (Sensor Control Unit)-440

Local Address: 0x288																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE				
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.112 {0x28C} V4_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-441

Local Address: 0x28C																		Register Type: RO (read only) Reset Value: 0x00000000														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.113 {0x290} V4_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-442

Local Address: 0x290																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.114 {0x294} V4_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-443

Local Address: 0x294																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.115 {0x298} V4_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-444

Local Address: 0x298																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name				Type		Reset Value		Description																					
31		Reserved				RO		0x0		Reserved																					
30..16		TIME_STAMP_INTERVAL				RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																					
15		Reserved				RO		0x0		Reserved																					
14..0		LATEST_BASE_TIMESTAMP_LSB				RW		0x0000		Reference time stamp value (second after the decimal point)																					

3.9.12.10.116 {0x2A0} V5_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-445

Local Address: 0x2A0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name						Type	Reset Value						Description																
31..16		FIFO_START_OFST						RW	0xA000						Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																
15..0		FIFO_PARTITION_SIZE						RW	0x0000						Partition size -1 Sets partition size minus 1. (by Sample unit)																

3.9.12.10.117 {0x2A4} V5_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-446

Local Address: 0x2A4														Register Type: RW (read/write) Reset Value: 0x00000000																																									
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8														7 6 5 4 3 2 1 0													
Reserved																		FIFO_RESET		Reserved																		OVERWRITE_IF_FULL		FIFO_SAMPLE_SIZE															
Bits	Name			Type	Reset Value	Description																																																	
31..17	Reserved			RO	0x0000	Reserved																																																	
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																																	
15..5	Reserved			RO	0x000	Reserved																																																	
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																																																	
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																																	

3.9.12.10.118 {0x2A8} V5_W_C_STATUS Details

Table SCU (Sensor Control Unit)-447

Local Address: 0x2A8																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																									
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4		Reserved				RO		0x000		Reserved																									
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.119 {0x2AC} V5_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-448

Local Address: 0x2AC																				Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
LATEST_TIMESTAMP_MSB																																			
Bits		Name						Type	Reset Value						Description																				
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																				

3.9.12.10.120 {0x2B0} V5_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-449

Local Address: 0x2B0																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.121 {0x2B4} V5_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-450

Local Address: 0x2B4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.122 {0x2B8} V5_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-451

Local Address: 0x2B8																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.123 {0x2C0} V6_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-452

Local Address: 0x2C0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.124 {0x2C4} V6_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-453

Local Address: 0x2C4														Register Type: RW (read/write) Reset Value: 0x00000000																													
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																		FIFO_RESET	Reserved																		OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE					
Bits	Name			Type	Reset Value	Description																																					
31..17	Reserved			RO	0x0000	Reserved																																					
16	FIFO_RESET			WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																																					
15..5	Reserved			RO	0x000	Reserved																																					
4	OVERWRITE_IF_FULL			RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																																					
3..0	FIFO_SAMPLE_SIZE			RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																					

3.9.12.10.125 {0x2C8} V6_W_C_STATUS Details

Table SCU (Sensor Control Unit)-454

Local Address: 0x2C8																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
FIFO_WRITE_PTR																Reserved											FIFO_WRITE_PHASE					
Bits	Name				Type	Reset Value	Description																									
31..16	FIFO_WRITE_PTR				RO	0x0000	Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4	Reserved				RO	0x000	Reserved																									
3..0	FIFO_WRITE_PHASE				RO	0x0	Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.126 {0x2CC} V6_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-455

Local Address: 0x2CC																				Register Type: RO (read only) Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.127 {0x2D0} V6_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-456

Local Address: 0x2D0																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LATEST_TIMESTAMP_LSB																
Bits		Name					Type	Reset Value					Description																		
31..15		Reserved					RO	0x00000					Reserved																		
14..0		LATEST_TIMESTAMP_LSB					RO	0x0000					Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																		

3.9.12.10.128 {0x2D4} V6_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-457

Local Address: 0x2D4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.129 {0x2D8} V6_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-458

Local Address: 0x2D8																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.130 {0x2E0} V7_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-459

Local Address: 0x2E0																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.131 {0x2E4} V7_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-460

Local Address: 0x2E4														Register Type: RW (read/write) Reset Value: 0x00000000																																									
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8														7 6 5 4 3 2 1 0													
Reserved																		FIFO_RESET	Reserved																		OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE																	
Bits		Name		Type		Reset Value		Description																																															
31..17		Reserved		RO		0x0000		Reserved																																															
16		FIFO_RESET		WO		0x0		Reset of the FIFO Clears the writing pointer to “0”																																															
15..5		Reserved		RO		0x000		Reserved																																															
4		OVERWRITE_IF_FULL		RW		0x0		OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																																															
3..0		FIFO_SAMPLE_SIZE		RW		0x0		Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																																															

3.9.12.10.132 {0x2E8} V7_W_C_STATUS Details

Table SCU (Sensor Control Unit)-461

Local Address: 0x2E8																Register Type: RO (read only) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
FIFO_WRITE_PTR																Reserved																FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																									
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																									
15..4		Reserved				RO		0x000		Reserved																									
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																									

3.9.12.10.133 {0x2EC} V7_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-462

Local Address: 0x2EC																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.134 {0x2F0} V7_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-463

Local Address: 0x2F0																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																LATEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																				

3.9.12.10.135 {0x2F4} V7_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-464

Local Address: 0x2F4																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.136 {0x2F8} V7_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-465

Local Address: 0x2F8																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name				Type		Reset Value		Description																					
31		Reserved				RO		0x0		Reserved																					
30..16		TIME_STAMP_INTERVAL				RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																					
15		Reserved				RO		0x0		Reserved																					
14..0		LATEST_BASE_TIMESTAMP_LSB				RW		0x0000		Reference time stamp value (second after the decimal point)																					

3.9.12.10.137 {0x300} V8_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-466

Local Address: 0x300																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type	Reset Value				Description																				
31..16		FIFO_START_OFST				RW	0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																				
15..0		FIFO_PARTITION_SIZE				RW	0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																				

3.9.12.10.138 {0x304} V8_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-467

Local Address: 0x304																Register Type: RW (read/write) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE			
Bits	Name			Type	Reset Value		Description																														
31..17	Reserved			RO	0x0000		Reserved																														
16	FIFO_RESET			WO	0x0		Reset of the FIFO Clears the writing pointer to “0”																														
15..5	Reserved			RO	0x000		Reserved																														
4	OVERWRITE_IF_FULL			RW	0x0		OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																														
3..0	FIFO_SAMPLE_SIZE			RW	0x0		Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																														

3.9.12.10.139 {0x308} V8_W_C_STATUS Details

Table SCU (Sensor Control Unit)-468

Local Address: 0x308																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.140 {0x30C} V8_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-469

Local Address: 0x30C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.141 {0x310} V8_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-470

Local Address: 0x310																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATEST_TIMESTAMP_LSB																	
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		LATEST_TIMESTAMP_LSB						RO	0x0000						Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																

3.9.12.10.142 {0x314} V8_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-471

Local Address: 0x314																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.143 {0x318} V8_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-472

Local Address: 0x318																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.144 {0x320} V9_W_C_CTRL0 Details

Table SCU (Sensor Control Unit)-473

Local Address: 0x320																Register Type: RW (read/write) Reset Value: 0xA0000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_START_OFST																FIFO_PARTITION_SIZE															
Bits		Name				Type		Reset Value				Description																			
31..16		FIFO_START_OFST				RW		0xA000				Start address offset Means the start address offset of the RAM for the FIFO (by Byte unit)																			
15..0		FIFO_PARTITION_SIZE				RW		0x0000				Partition size -1 Sets partition size minus 1. (by Sample unit)																			

3.9.12.10.145 {0x324} V9_W_C_CTRL1 Details

Table SCU (Sensor Control Unit)-474

Local Address: 0x324																Register Type: RW (read/write)																		
																Reset Value: 0x00000000																		
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0										
Reserved																FIFO_RESET	Reserved																OVERWRITE_IF_FULL	FIFO_SAMPLE_SIZE
Bits	Name		Type	Reset Value	Description																													
31..17	Reserved		RO	0x0000	Reserved																													
16	FIFO_RESET		WO	0x0	Reset of the FIFO Clears the writing pointer to “0”																													
15..5	Reserved		RO	0x000	Reserved																													
4	OVERWRITE_IF_FULL		RW	0x0	OVERWRITE_IF_FULL overview Sets whether to overwrite or not at FIFO Full 0: does not overwrite 1: overwrites																													
3..0	FIFO_SAMPLE_SIZE		RW	0x0	Number of Byte per Sample – 1 Sets data length per Sample in the FIFO by Byte unit																													

3.9.12.10.146 {0x328} V9_W_C_STATUS Details

Table SCU (Sensor Control Unit)-475

Local Address: 0x328																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_WRITE_PTR																Reserved												FIFO_WRITE_PHASE			
Bits		Name				Type		Reset Value		Description																					
31..16		FIFO_WRITE_PTR				RO		0x0000		Writing pointer address of the FIFO The start address where the next data is written by Byte unit																					
15..4		Reserved				RO		0x000		Reserved																					
3..0		FIFO_WRITE_PHASE				RO		0x0		Write phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																					

3.9.12.10.147 {0x32C} V9_W_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-476

Local Address: 0x32C																						Register Type: RO (read only)										
																						Reset Value: 0x00000000										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LATEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		LATEST_TIMESTAMP_MSB						RO	0x00000000						Latest time stamp (integer part of second) Time stamp which supports the newest data in the FIFO Second unit																	

3.9.12.10.148 {0x330} V9_W_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-477

Local Address: 0x330																		Register Type: RO (read only) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
Reserved														LATEST_TIMESTAMP_LSB																					
Bits				Name				Type		Reset Value				Description																					
31..15				Reserved				RO		0x00000				Reserved																					
14..0				LATEST_TIMESTAMP_LSB				RO		0x0000				Latest time stamp (second after the decimal point) The start address where the next data is written by Byte unit																					

3.9.12.10.149 {0x334} V9_W_C_TIMESTAMP_SET0 Details

Table SCU (Sensor Control Unit)-478

Local Address: 0x334																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATEST_BASE_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		LATEST_BASE_TIMESTAMP_MSB				RW	0x00000000				Reference time stamp value (integer part of second)																				

3.9.12.10.150 {0x338} V9_W_C_TIMESTAMP_SET1 Details

Table SCU (Sensor Control Unit)-479

Local Address: 0x338																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved	TIME_STAMP_INTERVAL															Reserved	LATEST_BASE_TIMESTAMP_LSB														
Bits		Name						Type		Reset Value		Description																			
31		Reserved						RO		0x0		Reserved																			
30..16		TIME_STAMP_INTERVAL						RW		0x0000		Time stamp interval (virtual sensor partition only) TIME_STAMP_INTERVAL only exists in the control registers for the virtual sensor partition. Every writing to FIFO_WRITE_REG, the value is accumulated to LATEST_TIME_STAMP.																			
15		Reserved						RO		0x0		Reserved																			
14..0		LATEST_BASE_TIMESTAMP_LSB						RW		0x0000		Reference time stamp value (second after the decimal point)																			

3.9.12.10.151 {0x1000} D0_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-480

Local Address: 0x1000																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																WATER_MARK															
Bits				Name				Type				Reset Value				Description															
31..16				Reserved				RO				0x0000				Reserved															
15..0				WATER_MARK				RW				0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.152 {0x1004} D0_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-481

Local Address: 0x1004																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved		RO	0x00	Reserved																																						
25	FIFO_DMA_ENABLE		RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																						
24	FIFO_ENABLE		RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																						
23..17	Reserved		RO	0x00	Reserved																																						
16	FIFO_RESET		WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																						
15..9	Reserved		RO	0x00	Reserved																																						
8	FIFO_PHASE_RESET		WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																						
7..2	Reserved		RO	0x00	Reserved																																						
1	FIFO_UNDER_RUN_CLR		WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																						

0	FIFO_OVER_ RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.153 {0x1008} D0_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-482

Local Address: 0x1008																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits	Name							Type	Reset Value	Description																					
31..16	Reserved							RO	0x0000	Reserved																					
15..0	FIFO_AVAIABLE_DATA_NUM							RO	0x0000	The number of data stored in the FIFO Number of sample unit																					

3.9.12.10.154 {0x100C} D0_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-483

Local Address: 0x100C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name	Type	Reset Value	Description																																	
31..16	FIFO_READ_PTR	RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																																	
15..12	Reserved	RO	0x0	Reserved																																	
11..8	FIFO_READ_PHASE	RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																	
7..6	Reserved	RO	0x0	Reserved																																	
5	FIFO_EMPTY_BYTE	RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																	
4	FIFO_EMPTY_SAMPLE	RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																	
3	FIFO_FULL	RO	0x0	Indicates “1” when the FIFO is full																																	
2	FIFO_ALMOST_FULL	RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																	
1	FIFO_UNDER_RUN	RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																																	
0	FIFO_OVER_RUN	RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																																	

3.9.12.10.155 {0x1010} D0_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-484

Local Address: 0x1010																		Register Type: RO (read only) Reset Value: 0x00000000														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.156 {0x1014} D0_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-485

Local Address: 0x1014																				Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.157 {0x1020} D0_R2_C_CTRL0 Details

Table SCU (Sensor Control Unit)-486

Local Address: 0x1020																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type		Reset Value				Description																			
31..16		Reserved				RO		0x0000				Reserved																			
15..0		WATER_MARK				RW		0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.																			

3.9.12.10.158 {0x1024} D0_R2_C_CTRL1 Details

Table SCU (Sensor Control Unit)-487

Local Address: 0x1024																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved		RO	0x00	Reserved																																						
25	FIFO_DMA_ENABLE		RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																						
24	FIFO_ENABLE		RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																						
23..17	Reserved		RO	0x00	Reserved																																						
16	FIFO_RESET		WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																						
15..9	Reserved		RO	0x00	Reserved																																						
8	FIFO_PHASE_RESET		WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																						
7..2	Reserved		RO	0x00	Reserved																																						
1	FIFO_UNDER_RUN_CLR		WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																						

0	FIFO_OVER_ RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.159 {0x1028} D0_R2_C_STATUS0 Details

Table SCU (Sensor Control Unit)-488

Local Address: 0x1028																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.160 {0x102C} D0_R2_C_STATUS1 Details

Table SCU (Sensor Control Unit)-489

Local Address: 0x102C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits		Name		Type	Reset Value		Description																														
31..16		FIFO_READ_PTR		RO	0x0000		Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																														
15..12		Reserved		RO	0x0		Reserved																														
11..8		FIFO_READ_PHASE		RO	0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																														
7..6		Reserved		RO	0x0		Reserved																														
5		FIFO_EMPTY_BYTE		RO	0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																														
4		FIFO_EMPTY_SAMPLE		RO	0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																														
3		FIFO_FULL		RO	0x0		Indicates “1” when the FIFO is full																														
2		FIFO_ALMOST_FULL		RO	0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																														
1		FIFO_UNDER_RUN		RO	0x0		Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																														
0		FIFO_OVER_RUN		RO	0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																														

3.9.12.10.161 {0x1030} D0_R2_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-490

Local Address: 0x1030																Register Type: RO (read only)																
																Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.162 {0x1034} D0_R2_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-491

Local Address: 0x1034																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														OLDEST_TIMESTAMP_LSB																	
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.163 {0x1040} D1_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-492

Local Address: 0x1040																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.164 {0x1044} D1_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-493

Local Address: 0x1044																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved		RO	0x00	Reserved																																						
25	FIFO_DMA_ENABLE		RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																						
24	FIFO_ENABLE		RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																						
23..17	Reserved		RO	0x00	Reserved																																						
16	FIFO_RESET		WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																						
15..9	Reserved		RO	0x00	Reserved																																						
8	FIFO_PHASE_RESET		WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																						
7..2	Reserved		RO	0x00	Reserved																																						
1	FIFO_UNDER_RUN_CLR		WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																						

0	FIFO_OVER_ RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.165 {0x1048} D1_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-494

Local Address: 0x1048																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.166 {0x104C} D1_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-495

Local Address: 0x104C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																															

3.9.12.10.167 {0x1050} D1_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-496

Local Address: 0x1050																Register Type: RO (read only)																
																Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.168 {0x1054} D1_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-497

Local Address: 0x1054																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.169 {0x1060} D1_R2_C_CTRL0 Details

Table SCU (Sensor Control Unit)-498

Local Address: 0x1060																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits	Name							Type	Reset Value							Description															
31..16	Reserved							RO	0x0000							Reserved															
15..0	WATER_MARK							RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.170 {0x1064} D1_R2_C_CTRL1 Details

Table SCU (Sensor Control Unit)-499

Local Address: 0x1064																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved		RO	0x00	Reserved																																						
25	FIFO_DMA_ENABLE		RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																						
24	FIFO_ENABLE		RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																						
23..17	Reserved		RO	0x00	Reserved																																						
16	FIFO_RESET		WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																						
15..9	Reserved		RO	0x00	Reserved																																						
8	FIFO_PHASE_RESET		WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																						
7..2	Reserved		RO	0x00	Reserved																																						
1	FIFO_UNDER_RUN_CLR		WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																						

0	FIFO_OVER_ RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.171 {0x1068} D1_R2_C_STATUS0 Details

Table SCU (Sensor Control Unit)-500

Local Address: 0x1068																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.172 {0x106C} D1_R2_C_STATUS1 Details

Table SCU (Sensor Control Unit)-501

Local Address: 0x106C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																															

3.9.12.10.173 {0x1070} D1_R2_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-502

Local Address: 0x1070																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.174 {0x1074} D1_R2_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-503

Local Address: 0x1074																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.175 {0x1080} N0_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-504

Local Address: 0x1080																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		WATER_MARK				RW	0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.																				

3.9.12.10.176 {0x1084} N0_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-505

Local Address: 0x1084																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.177 {0x1088} N0_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-506

Local Address: 0x1088																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type		Reset Value		Description																					
31..16		Reserved				RO		0x0000		Reserved																					
15..0		FIFO_AVAIABLE_DATA_NUM				RO		0x0000		The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																					

3.9.12.10.178 {0x108C} N0_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-507

Local Address: 0x108C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																															

3.9.12.10.179 {0x1090} N0_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-508

Local Address: 0x1090																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.180 {0x1094} N0_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-509

Local Address: 0x1094																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.181 {0x10A0} N1_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-510

Local Address: 0x10A0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.182 {0x10A4} N1_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-511

Local Address: 0x10A4																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.183 {0x10A8} N1_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-512

Local Address: 0x10A8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type		Reset Value				Description																			
31..16		Reserved				RO		0x0000				Reserved																			
15..0		FIFO_AVAIABLE_DATA_NUM				RO		0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																			

3.9.12.10.184 {0x10AC} N1_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-513

Local Address: 0x10AC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																																

3.9.12.10.185 {0x10B0} N1_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-514

Local Address: 0x10B0																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.186 {0x10B4} N1_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-515

Local Address: 0x10B4																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type		Reset Value				Description																			
31..15		Reserved				RO		0x00000				Reserved																			
14..0		OLDEST_TIMESTAMP_LSB				RO		0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																			

3.9.12.10.187 {0x10C0} N2_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-516

Local Address: 0x10C0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.188 {0x10C4} N2_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-517

Local Address: 0x10C4																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.189 {0x10C8} N2_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-518

Local Address: 0x10C8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.190 {0x10CC} N2_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-519

Local Address: 0x10CC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																															

3.9.12.10.191 {0x10D0} N2_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-520

Local Address: 0x10D0																				Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0											
OLDEST_TIMESTAMP_MSB																																			
Bits		Name						Type		Reset Value						Description																			
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																			

3.9.12.10.192 {0x10D4} N2_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-521

Local Address: 0x10D4																				Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.193 {0x10E0} N3_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-522

Local Address: 0x10E0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.194 {0x10E4} N3_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-523

Local Address: 0x10E4																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.195 {0x10E8} N3_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-524

Local Address: 0x10E8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		FIFO_AVAIABLE_DATA_NUM						RO	0x0000						The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																

3.9.12.10.196 {0x10EC} N3_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-525

Local Address: 0x10EC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name				Type	Reset Value				Description																											
31..16	FIFO_READ_PTR				RO	0x0000				Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																											
15..12	Reserved				RO	0x0				Reserved																											
11..8	FIFO_READ_PHASE				RO	0x0				Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																											
7..6	Reserved				RO	0x0				Reserved																											
5	FIFO_EMPTY_BYTE				RO	0x0				Indicates “1” when the number of the valid data byte in the FIFO is “0”																											
4	FIFO_EMPTY_SAMPLE				RO	0x0				Indicates “1” when the number of the valid data sample in the FIFO is “0”																											
3	FIFO_FULL				RO	0x0				Indicates “1” when the FIFO is full																											
2	FIFO_ALMOST_FULL				RO	0x0				Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																											
1	FIFO_UNDER_RUN				RO	0x0				Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																											
0	FIFO_OVER_RUN				RO	0x0				Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																											

3.9.12.10.197 {0x10F0} N3_R1_C_TIMESTAMP0 Details

Table SCU (Sensor Control Unit)-526

Local Address: 0x10F0																		Register Type: RO (read only)														
																		Reset Value: 0x00000000														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.198 {0x10F4} N3_R1_C_TIMESTAMP1 Details

Table SCU (Sensor Control Unit)-527

Local Address: 0x10F4																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.199 {0x1100} N4_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-528

Local Address: 0x1100																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.200 {0x1104} N4_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-529

Local Address: 0x1104																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.201 {0x1108} N4_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-530

Local Address: 0x1108																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		FIFO_AVAIABLE_DATA_NUM						RO	0x0000						The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																

3.9.12.10.202 {0x110C} N4_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-531

Local Address: 0x110C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits		Name		Type	Reset Value		Description																														
31..16		FIFO_READ_PTR		RO	0x0000		Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																														
15..12		Reserved		RO	0x0		Reserved																														
11..8		FIFO_READ_PHASE		RO	0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																														
7..6		Reserved		RO	0x0		Reserved																														
5		FIFO_EMPTY_BYTE		RO	0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																														
4		FIFO_EMPTY_SAMPLE		RO	0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																														
3		FIFO_FULL		RO	0x0		Indicates “1” when the FIFO is full																														
2		FIFO_ALMOST_FULL		RO	0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																														
1		FIFO_UNDER_RUN		RO	0x0		Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																														
0		FIFO_OVER_RUN		RO	0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																														

3.9.12.10.203 {0x1110} N4_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-532

Local Address: 0x1110																		Register Type: RO (read only)															
																		Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.204 {0x1114} N4_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-533

Local Address: 0x1114																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value				Description																						
31..15		Reserved						RO	0x00000				Reserved																						
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																						

3.9.12.10.205 {0x1120} N5_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-534

Local Address: 0x1120																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.206 {0x1124} N5_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-535

Local Address: 0x1124																Register Type: RW (read/write) Reset Value: 0x00000000																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved							FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved					FIFO_RESET		Reserved						FIFO_PHASE_RESET		Reserved						FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																									
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																									
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																									
23..17	Reserved							RO	0x00	Reserved																									
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																									
15..9	Reserved							RO	0x00	Reserved																									
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																									
7..2	Reserved							RO	0x00	Reserved																									
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																									

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.207 {0x1128} N5_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-536

Local Address: 0x1128																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type		Reset Value				Description																			
31..16		Reserved				RO		0x0000				Reserved																			
15..0		FIFO_AVAIABLE_DATA_NUM				RO		0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																			

3.9.12.10.208 {0x112C} N5_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-537

Local Address: 0x112C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name	Type	Reset Value	Description																																	
31..16	FIFO_READ_PTR	RO	0x0000	Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																																	
15..12	Reserved	RO	0x0	Reserved																																	
11..8	FIFO_READ_PHASE	RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																	
7..6	Reserved	RO	0x0	Reserved																																	
5	FIFO_EMPTY_BYTE	RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																	
4	FIFO_EMPTY_SAMPLE	RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																	
3	FIFO_FULL	RO	0x0	Indicates “1” when the FIFO is full																																	
2	FIFO_ALMOST_FULL	RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																	
1	FIFO_UNDER_RUN	RO	0x0	Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																																	
0	FIFO_OVER_RUN	RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																																	

3.9.12.10.209 {0x1130} N5_R1_C_TIMESTAMP0 Details

Table SCU (Sensor Control Unit)-538

Local Address: 0x1130																Register Type: RO (read only) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.210 {0x1134} N5_R1_C_TIMESTAMP1 Details

Table SCU (Sensor Control Unit)-539

Local Address: 0x1134																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.211 {0x1140} N6_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-540

Local Address: 0x1140																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.															

3.9.12.10.212 {0x1144} N6_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-541

Local Address: 0x1144																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.213 {0x1148} N6_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-542

Local Address: 0x1148																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		FIFO_AVAIABLE_DATA_NUM						RO	0x0000						The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																

3.9.12.10.214 {0x114C} N6_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-543

Local Address: 0x114C																Register Type: RO (read only) Reset Value: 0x00000000																																																																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																																																															
FIFO_READ_PTR																Reserved								FIFO_READ_PHASE								Reserved								FIFO_EMPTY_BYTE								FIFO_EMPTY_SAMPLE								FIFO_FULL								FIFO_ALMOST_FULL								FIFO_UNDER_RUN								FIFO_OVER_RUN							

3.9.12.10.215 {0x1150} N6_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-544

Local Address: 0x1150																		Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.216 {0x1154} N6_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-545

Local Address: 0x1154																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.217 {0x1160} N7_R1_C_CTRL0 Details

Table SCU (Sensor Control Unit)-546

Local Address: 0x1160																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		WATER_MARK				RW	0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”.																				

3.9.12.10.218 {0x1164} N7_R1_C_CTRL1 Details

Table SCU (Sensor Control Unit)-547

Local Address: 0x1164																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is "1", the DMA control signal is permitted to output. When "0", the output is fixed to "0".																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the read out error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.219 {0x1168} N7_R1_C_STATUS0 Details

Table SCU (Sensor Control Unit)-548

Local Address: 0x1168																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.220 {0x116C} N7_R1_C_STATUS1 Details

Table SCU (Sensor Control Unit)-549

Local Address: 0x116C																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE	FIFO_EMPTY_SAMPLE	FIFO_FULL	FIFO_ALMOST_FULL	FIFO_UNDER_RUN	FIFO_OVER_RUN
Bits		Name		Type	Reset Value		Description																								
31..16		FIFO_READ_PTR		RO	0x0000		Readout pointer address in the FIFO Start address that is read out as the next data Byte unit																								
15..12		Reserved		RO	0x0		Reserved																								
11..8		FIFO_READ_PHASE		RO	0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																								
7..6		Reserved		RO	0x0		Reserved																								
5		FIFO_EMPTY_BYTE		RO	0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																								
4		FIFO_EMPTY_SAMPLE		RO	0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																								
3		FIFO_FULL		RO	0x0		Indicates “1” when the FIFO is full																								
2		FIFO_ALMOST_FULL		RO	0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																								
1		FIFO_UNDER_RUN		RO	0x0		Indicates "1", when the number of the valid data in the FIFO is "0" and the FIFO data is read out.																								
0		FIFO_OVER_RUN		RO	0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																								

3.9.12.10.221 {0x1170} N7_R1_C_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-550

Local Address: 0x1170																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.222 {0x1174} N7_R1_C_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-551

Local Address: 0x1174																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.223 {0x1180} D0_R3_CH_CTRL0 Details

Table SCU (Sensor Control Unit)-552

Local Address: 0x1180																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		WATER_MARK				RW	0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”																				

3.9.12.10.224 {0x1184} D0_R3_CH_CTRL1 Details

Table SCU (Sensor Control Unit)-553

Local Address: 0x1184																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is “1”, the DMA control signal is permitted to output. When “0”, the output is fixed to “0”.																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset the readout pointer for the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.225 {0x1188} D0_R3_CH_STATUS0 Details

Table SCU (Sensor Control Unit)-554

Local Address: 0x1188																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		FIFO_AVAIABLE_DATA_NUM						RO	0x0000						The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																

3.9.12.10.226 {0x118C} D0_R3_CH_STATUS1 Details

Table SCU (Sensor Control Unit)-555

Local Address: 0x118C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.227 {0x1190} D0_R3_CH_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-556

Local Address: 0x1190																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits	Name							Type	Reset Value							Description															
31..0	OLDEST_TIMESTAMP_MSB							RO	0x00000000							Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO															

3.9.12.10.228 {0x1194} D0_R3_CH_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-557

Local Address: 0x1194																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.229 {0x11A0} D1_R3_CH_CTRL0 Details

Table SCU (Sensor Control Unit)-558

Local Address: 0x11A0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.230 {0x11A4} D1_R3_CH_CTRL1 Details

Table SCU (Sensor Control Unit)-559

Local Address: 0x11A4																Register Type: RW (read/write) Reset Value: 0x00000000																											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																			
Reserved								FIFO_DMA_ENABLE		FIFO_ENABLE		Reserved								FIFO_RESET		Reserved								FIFO_PHASE_RESET		Reserved								FIFO_UNDER_RUN_CLR		FIFO_OVER_RUN_CLR	
31..26	Reserved							RO	0x00	Reserved																																	
25	FIFO_DMA_ENABLE							RW	0x0	Output permission of the DMA control signal When the value is “1”, the DMA control signal is permitted to output. When “0”, the output is fixed to “0”.																																	
24	FIFO_ENABLE							RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																	
23..17	Reserved							RO	0x00	Reserved																																	
16	FIFO_RESET							WO	0x0	Reset the readout pointer for the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																	
15..9	Reserved							RO	0x00	Reserved																																	
8	FIFO_PHASE_RESET							WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																	
7..2	Reserved							RO	0x00	Reserved																																	
1	FIFO_UNDER_RUN_CLR							WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																	

0	FIFO_OVER_RUN_CLR	WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full

3.9.12.10.231 {0x11A8} D1_R3_CH_STATUS0 Details

Table SCU (Sensor Control Unit)-560

Local Address: 0x11A8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type		Reset Value				Description																			
31..16		Reserved				RO		0x0000				Reserved																			
15..0		FIFO_AVAIABLE_DATA_NUM				RO		0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																			

3.9.12.10.232 {0x11AC} D1_R3_CH_STATUS1 Details

Table SCU (Sensor Control Unit)-561

Local Address: 0x11AC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name	Type	Reset Value	Description																																	
31..16	FIFO_READ_PTR	RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																	
15..12	Reserved	RO	0x0	Reserved																																	
11..8	FIFO_READ_PHASE	RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																	
7..6	Reserved	RO	0x0	Reserved																																	
5	FIFO_EMPTY_BYTE	RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																	
4	FIFO_EMPTY_SAMPLE	RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																	
3	FIFO_FULL	RO	0x0	Indicates “1” when the FIFO is full																																	
2	FIFO_ALMOST_FULL	RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																	
1	FIFO_UNDER_RUN	RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																	
0	FIFO_OVER_RUN	RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																	

3.9.12.10.233 {0x11B0} D1_R3_CH_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-562

Local Address: 0x11B0																		Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.234 {0x11B4} D1_R3_CH_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-563

Local Address: 0x11B4																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved															OLDEST_TIMESTAMP_LSB																				
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.235 {0x11C0} D0_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-564

Local Address: 0x11C0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.236 {0x11C4} D0_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-565

Local Address: 0x11C4														Register Type: RW (read/write) Reset Value: 0x00000000																																									
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8														7 6 5 4 3 2 1 0													
Reserved														Reserved														Reserved														Reserved													
FIFO_ENABLE														FIFO_RESET														FIFO_PHASE_RESET														FIFO_UNDER_RUN_CLR FIFO_OVER_RUN_CLR													
Bits		Name		Type		Reset Value		Description																																															
31..25		Reserved		RO		0x00		Reserved																																															
24		FIFO_ENABLE		RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																															
23..17		Reserved		RO		0x00		Reserved																																															
16		FIFO_RESET		WO		0x0		Reset the readout pointer for the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																															
15..9		Reserved		RO		0x00		Reserved																																															
8		FIFO_PHASE_RESET		WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																															
7..2		Reserved		RO		0x00		Reserved																																															
1		FIFO_UNDER_RUN_CLR		WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																															
0		FIFO_OVER_RUN_CLR		WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																																															

3.9.12.10.237 {0x11C8} D0_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-566

Local Address: 0x11C8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.238 {0x11CC} D0_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-567

Local Address: 0x11CC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.239 {0x11D0} D0_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-568

Local Address: 0x11D0																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.240 {0x11D4} D0_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-569

Local Address: 0x11D4																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved															OLDEST_TIMESTAMP_LSB																				
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.241 {0x11E0} D1_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-570

Local Address: 0x11E0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.242 {0x11E4} D1_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-571

Local Address: 0x11E4														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value			Description																					
31..25	Reserved			RO	0x00			Reserved																					
24	FIFO_ENABLE			RW	0x0			Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17	Reserved			RO	0x00			Reserved																					
16	FIFO_RESET			WO	0x0			Reset the readout pointer for the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9	Reserved			RO	0x00			Reserved																					
8	FIFO_PHASE_RESET			WO	0x0			Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2	Reserved			RO	0x00			Reserved																					
1	FIFO_UNDER_RUN_CLR			WO	0x0			Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0	FIFO_OVER_RUN_CLR			WO	0x0			Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.243 {0x11E8} D1_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-572

Local Address: 0x11E8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.244 {0x11EC} D1_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-573

Local Address: 0x11EC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.245 {0x11F0} D1_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-574

Local Address: 0x11F0																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.246 {0x11F4} D1_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-575

Local Address: 0x11F4																		Register Type: RO (read only)													
Reset Value: 0x00000000																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.247 {0x1200} N0_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-576

Local Address: 0x1200																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		WATER_MARK				RW	0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”																				

3.9.12.10.248 {0x1204} N0_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-577

Local Address: 0x1204														Register Type: RW (read/write) Reset Value: 0x00000000																																									
31 30 29 28 27 26 25 24														23 22 21 20 19 18 17 16														15 14 13 12 11 10 9 8														7 6 5 4 3 2 1 0													
Reserved														Reserved														Reserved														Reserved													
FIFO_ENABLE														FIFO_RESET														FIFO_PHASE_RESET														FIFO_UNDER_RUN_CLR FIFO_OVER_RUN_CLR													
Bits		Name		Type	Reset Value	Description																																																	
31..25		Reserved		RO	0x00	Reserved																																																	
24		FIFO_ENABLE		RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																																																	
23..17		Reserved		RO	0x00	Reserved																																																	
16		FIFO_RESET		WO	0x0	Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																																																	
15..9		Reserved		RO	0x00	Reserved																																																	
8		FIFO_PHASE_RESET		WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																																																	
7..2		Reserved		RO	0x00	Reserved																																																	
1		FIFO_UNDER_RUN_CLR		WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																																																	
0		FIFO_OVER_RUN_CLR		WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																																																	

3.9.12.10.249 {0x1208} N0_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-578

Local Address: 0x1208																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.250 {0x120C} N0_R0_H_STATUS1 details

Table SCU (Sensor Control Unit)-579

Local Address: 0x120C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when FIFO is full																															

3.9.12.10.251 {0x1210} N0_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-580

Local Address: 0x1210																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.252 {0x1214} N0_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-581

Local Address: 0x1214																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.253 {0x1220} N1_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-582

Local Address: 0x1220																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.254 {0x1224} N1_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-583

Local Address: 0x1224														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.255 {0x1228} N1_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-584

Local Address: 0x1228																Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits				Name				Type		Reset Value				Description																	
31..16				Reserved				RO		0x0000				Reserved																	
15..0				FIFO_AVAIABLE_DATA_NUM				RO		0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																	

3.9.12.10.256 {0x122C} N1_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-585

Local Address: 0x122C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																															

3.9.12.10.257 {0x1230} N1_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-586

Local Address: 0x1230																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type		Reset Value				Description																			
31..0		OLDEST_TIMESTAMP_MSB				RO		0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																			

3.9.12.10.258 {0x1234} N1_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-587

Local Address: 0x1234																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.259 {0x1240} N2_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-588

Local Address: 0x1240																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.260 {0x1244} N2_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-589

Local Address: 0x1244														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.261 {0x1248} N2_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-590

Local Address: 0x1248																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.262 {0x124C} N2_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-591

Local Address: 0x124C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits		Name		Type		Reset Value		Description																													
31..16		FIFO_READ_PTR		RO		0x0000		Readout pointer address in the FIFO The next data is read out on the start address Byte unit																													
15..12		Reserved		RO		0x0		Reserved																													
11..8		FIFO_READ_PHASE		RO		0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																													
7..6		Reserved		RO		0x0		Reserved																													
5		FIFO_EMPTY_BYTE		RO		0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																													
4		FIFO_EMPTY_SAMPLE		RO		0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																													
3		FIFO_FULL		RO		0x0		Indicates “1” when the FIFO is full																													
2		FIFO_ALMOST_FULL		RO		0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																													
1		FIFO_UNDER_RUN		RO		0x0		Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																													
0		FIFO_OVER_RUN		RO		0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																													

3.9.12.10.263 {0x1250} N2_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-592

Local Address: 0x1250																		Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.264 {0x1254} N2_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-593

Local Address: 0x1254																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.265 {0x1260} N3_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-594

Local Address: 0x1260																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.266 {0x1264} N3_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-595

Local Address: 0x1264														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.267 {0x1268} N3_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-596

Local Address: 0x1268																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.268 {0x126C} N3_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-597

Local Address: 0x126C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																															

3.9.12.10.269 {0x1270} N3_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-598

Local Address: 0x1270																Register Type: RO (read only)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type		Reset Value				Description																			
31..0		OLDEST_TIMESTAMP_MSB				RO		0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																			

3.9.12.10.270 {0x1274} N3_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-599

Local Address: 0x1274																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.271 {0x1280} N4_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-600

Local Address: 0x1280																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.272 {0x1284} N4_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-601

Local Address: 0x1284														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type	Reset Value		Description																									
31..25		Reserved						RO	0x00		Reserved																									
24		FIFO_ENABLE						RW	0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																									
23..17		Reserved						RO	0x00		Reserved																									
16		FIFO_RESET						WO	0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																									
15..9		Reserved						RO	0x00		Reserved																									
8		FIFO_PHASE_RESET						WO	0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																									
7..2		Reserved						RO	0x00		Reserved																									
1		FIFO_UNDER_RUN_CLR						WO	0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																									
0		FIFO_OVER_RUN_CLR						WO	0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																									

3.9.12.10.273 {0x1288} N4_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-602

Local Address: 0x1288																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.274 {0x128C} N4_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-603

Local Address: 0x128C																				Register Type: RO (read only) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.275 {0x1290} N4_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-604

Local Address: 0x1290																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type		Reset Value				Description																			
31..0		OLDEST_TIMESTAMP_MSB				RO		0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																			

3.9.12.10.276 {0x1294} N4_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-605

Local Address: 0x1294																		Register Type: RO (read only)													
																		Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name						Type	Reset Value				Description																		
31..15		Reserved						RO	0x00000				Reserved																		
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.277 {0x12A0} N5_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-606

Local Address: 0x12A0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		WATER_MARK				RW	0xFFFF				Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”																				

3.9.12.10.278 {0x12A4} N5_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-607

Local Address: 0x12A4														Register Type: RW (read/write)															
														Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value			Description																					
31..25	Reserved			RO	0x00			Reserved																					
24	FIFO_ENABLE			RW	0x0			Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17	Reserved			RO	0x00			Reserved																					
16	FIFO_RESET			WO	0x0			Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9	Reserved			RO	0x00			Reserved																					
8	FIFO_PHASE_RESET			WO	0x0			Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2	Reserved			RO	0x00			Reserved																					
1	FIFO_UNDER_RUN_CLR			WO	0x0			Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0	FIFO_OVER_RUN_CLR			WO	0x0			Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.279 {0x12A8} N5_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-608

Local Address: 0x12A8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.280 {0x12AC} N5_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-609

Local Address: 0x12AC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.281 {0x12B0} N5_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-610

Local Address: 0x12B0																		Register Type: RO (read only)														
																		Reset Value: 0x00000000														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.282 {0x12B4} N5_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-611

Local Address: 0x12B4																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name					Type	Reset Value					Description																		
31..15		Reserved					RO	0x00000					Reserved																		
14..0		OLDEST_TIMESTAMP_LSB					RO	0x0000					Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																		

3.9.12.10.283 {0x12C0} N6_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-612

Local Address: 0x12C0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.284 {0x12C4} N6_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-613

Local Address: 0x12C4														Register Type: RW (read/write)															
														Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits		Name		Type		Reset Value		Description																					
31..25		Reserved		RO		0x00		Reserved																					
24		FIFO_ENABLE		RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17		Reserved		RO		0x00		Reserved																					
16		FIFO_RESET		WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9		Reserved		RO		0x00		Reserved																					
8		FIFO_PHASE_RESET		WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2		Reserved		RO		0x00		Reserved																					
1		FIFO_UNDER_RUN_CLR		WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0		FIFO_OVER_RUN_CLR		WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.285 {0x12C8} N6_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-614

Local Address: 0x12C8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.286 {0x12CC} N6_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-615

Local Address: 0x12CC														Register Type: RO (read only) Reset Value: 0x00000000																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits		Name		Type	Reset Value		Description																														
31..16		FIFO_READ_PTR		RO	0x0000		Readout pointer address in the FIFO The next data is read out on the start address Byte unit																														
15..12		Reserved		RO	0x0		Reserved																														
11..8		FIFO_READ_PHASE		RO	0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																														
7..6		Reserved		RO	0x0		Reserved																														
5		FIFO_EMPTY_BYTE		RO	0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																														
4		FIFO_EMPTY_SAMPLE		RO	0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																														
3		FIFO_FULL		RO	0x0		Indicates “1” when the FIFO is full																														
2		FIFO_ALMOST_FULL		RO	0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																														
1		FIFO_UNDER_RUN		RO	0x0		Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																														
0		FIFO_OVER_RUN		RO	0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																														

3.9.12.10.287 {0x12D0} N6_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-616

Local Address: 0x12D0																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.288 {0x12D4} N6_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-617

Local Address: 0x12D4																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.289 {0x12E0} N7_R0_H_CTRL0 Details

Table SCU (Sensor Control Unit)-618

Local Address: 0x12E0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.290 {0x12E4} N7_R0_H_CTRL1 Details

Table SCU (Sensor Control Unit)-619

Local Address: 0x12E4														Register Type: RW (read/write)															
														Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits		Name		Type		Reset Value		Description																					
31..25		Reserved		RO		0x00		Reserved																					
24		FIFO_ENABLE		RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17		Reserved		RO		0x00		Reserved																					
16		FIFO_RESET		WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9		Reserved		RO		0x00		Reserved																					
8		FIFO_PHASE_RESET		WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2		Reserved		RO		0x00		Reserved																					
1		FIFO_UNDER_RUN_CLR		WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0		FIFO_OVER_RUN_CLR		WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.291 {0x12E8} N7_R0_H_STATUS0 Details

Table SCU (Sensor Control Unit)-620

Local Address: 0x12E8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.292 {0x12EC} N7_R0_H_STATUS1 Details

Table SCU (Sensor Control Unit)-621

Local Address: 0x12EC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.293 {0x12F0} N7_R0_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-622

Local Address: 0x12F0																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.294 {0x12F4} N7_R0_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-623

Local Address: 0x12F4																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.295 {0x1300} V0_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-624

Local Address: 0x1300																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.296 {0x1304} V0_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-625

Local Address: 0x1304														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.297 {0x1308} V0_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-626

Local Address: 0x1308																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.298 {0x130C} V0_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-627

Local Address: 0x130C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.299 {0x1310} V0_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-628

Local Address: 0x1310																		Register Type: RO (read only)															
																		Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.300 {0x1314} V0_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-629

Local Address: 0x1314																				Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value				Description																						
31..15		Reserved						RO	0x00000				Reserved																						
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																						

3.9.12.10.301 {0x1320} V1_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-630

Local Address: 0x1320																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.302 {0x1324} V1_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-631

Local Address: 0x1324														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.303 {0x1328} V1_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-632

Local Address: 0x1328																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.304 {0x132C} V1_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-633

Local Address: 0x132C																						Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.305 {0x1330} V1_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-634

Local Address: 0x1330																Register Type: RO (read only)																
																Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.306 {0x1334} V1_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-635

Local Address: 0x1334																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value				Description																						
31..15		Reserved						RO	0x00000				Reserved																						
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																						

3.9.12.10.307 {0x1340} V2_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-636

Local Address: 0x1340																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		WATER_MARK						RW	0xFFFF						Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”																

3.9.12.10.308 {0x1344} V2_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-637

Local Address: 0x1344														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.309 {0x1348} V2_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-638

Local Address: 0x1348																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.310 {0x134C} V2_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-639

Local Address: 0x134C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name			Type	Reset Value	Description																															
31..16	FIFO_READ_PTR			RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																															
15..12	Reserved			RO	0x0	Reserved																															
11..8	FIFO_READ_PHASE			RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																															
7..6	Reserved			RO	0x0	Reserved																															
5	FIFO_EMPTY_BYTE			RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																															
4	FIFO_EMPTY_SAMPLE			RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																															
3	FIFO_FULL			RO	0x0	Indicates “1” when the FIFO is full																															
2	FIFO_ALMOST_FULL			RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																															
1	FIFO_UNDER_RUN			RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																															
0	FIFO_OVER_RUN			RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																															

3.9.12.10.311 {0x1350} V2_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-640

Local Address: 0x1350																		Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.312 {0x1354} V2_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-641

Local Address: 0x1354																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.313 {0x1360} V3_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-642

Local Address: 0x1360																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.314 {0x1364} V3_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-643

Local Address: 0x1364														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value			Description																					
31..25	Reserved			RO	0x00			Reserved																					
24	FIFO_ENABLE			RW	0x0			Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17	Reserved			RO	0x00			Reserved																					
16	FIFO_RESET			WO	0x0			Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9	Reserved			RO	0x00			Reserved																					
8	FIFO_PHASE_RESET			WO	0x0			Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2	Reserved			RO	0x00			Reserved																					
1	FIFO_UNDER_RUN_CLR			WO	0x0			Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0	FIFO_OVER_RUN_CLR			WO	0x0			Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.315 {0x1368} V3_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-644

Local Address: 0x1368																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.316 {0x136C} V3_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-645

Local Address: 0x136C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits		Name		Type	Reset Value		Description																														
31..16		FIFO_READ_PTR		RO	0x0000		Readout pointer address in the FIFO The next data is read out on the start address Byte unit																														
15..12		Reserved		RO	0x0		Reserved																														
11..8		FIFO_READ_PHASE		RO	0x0		Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																														
7..6		Reserved		RO	0x0		Reserved																														
5		FIFO_EMPTY_BYTE		RO	0x0		Indicates “1” when the number of the valid data byte in the FIFO is “0”																														
4		FIFO_EMPTY_SAMPLE		RO	0x0		Indicates “1” when the number of the valid data sample in the FIFO is “0”																														
3		FIFO_FULL		RO	0x0		Indicates “1” when the FIFO is full																														
2		FIFO_ALMOST_FULL		RO	0x0		Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																														
1		FIFO_UNDER_RUN		RO	0x0		Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																														
0		FIFO_OVER_RUN		RO	0x0		Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																														

3.9.12.10.317 {0x1370} V3_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-646

Local Address: 0x1370																				Register Type: RO (read only)											
																				Reset Value: 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.318 {0x1374} V3_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-647

Local Address: 0x1374																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.319 {0x1380} V4_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-648

Local Address: 0x1380																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value						Description																
31..16		Reserved						RO	0x0000						Reserved																
15..0		WATER_MARK						RW	0xFFFF						Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”																

3.9.12.10.320 {0x1384} V4_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-649

Local Address: 0x1384														Register Type: RW (read/write)															
														Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits		Name		Type		Reset Value		Description																					
31..25		Reserved		RO		0x00		Reserved																					
24		FIFO_ENABLE		RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																					
23..17		Reserved		RO		0x00		Reserved																					
16		FIFO_RESET		WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																					
15..9		Reserved		RO		0x00		Reserved																					
8		FIFO_PHASE_RESET		WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																					
7..2		Reserved		RO		0x00		Reserved																					
1		FIFO_UNDER_RUN_CLR		WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																					
0		FIFO_OVER_RUN_CLR		WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																					

3.9.12.10.321 {0x1388} V4_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-650

Local Address: 0x1388																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.322 {0x138C} V4_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-651

Local Address: 0x138C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.323 {0x1390} V4_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-652

Local Address: 0x1390																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.324 {0x1394} V4_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-653

Local Address: 0x1394																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.325 {0x13A0} V5_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-654

Local Address: 0x13A0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.326 {0x13A4} V5_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-655

Local Address: 0x13A4														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value	Description																							
31..25	Reserved			RO	0x00	Reserved																							
24	FIFO_ENABLE			RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																							
23..17	Reserved			RO	0x00	Reserved																							
16	FIFO_RESET			WO	0x0	Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																							
15..9	Reserved			RO	0x00	Reserved																							
8	FIFO_PHASE_RESET			WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																							
7..2	Reserved			RO	0x00	Reserved																							
1	FIFO_UNDER_RUN_CLR			WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																							
0	FIFO_OVER_RUN_CLR			WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																							

3.9.12.10.327 {0x13A8} V5_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-656

Local Address: 0x13A8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.328 {0x13AC} V5_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-657

Local Address: 0x13AC																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.329 {0x13B0} V5_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-658

Local Address: 0x13B0																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLDEST_TIMESTAMP_MSB																															
Bits		Name				Type	Reset Value				Description																				
31..0		OLDEST_TIMESTAMP_MSB				RO	0x00000000				Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																				

3.9.12.10.330 {0x13B4} V5_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-659

Local Address: 0x13B4																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.331 {0x13C0} V6_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-660

Local Address: 0x13C0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.332 {0x13C4} V6_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-661

Local Address: 0x13C4														Register Type: RW (read/write) Reset Value: 0x00000000																						
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0												
Reserved								FIFO_ENABLE	Reserved								FIFO_RESET	Reserved								FIFO_PHASE_RESET	Reserved								FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR
Bits		Name						Type		Reset Value		Description																								
31..25		Reserved						RO		0x00		Reserved																								
24		FIFO_ENABLE						RW		0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																								
23..17		Reserved						RO		0x00		Reserved																								
16		FIFO_RESET						WO		0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																								
15..9		Reserved						RO		0x00		Reserved																								
8		FIFO_PHASE_RESET						WO		0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																								
7..2		Reserved						RO		0x00		Reserved																								
1		FIFO_UNDER_RUN_CLR						WO		0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																								
0		FIFO_OVER_RUN_CLR						WO		0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																								

3.9.12.10.333 {0x13C8} V6_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-662

Local Address: 0x13C8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.334 {0x13CC} V6_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-663

Local Address: 0x13CC																Register Type: RO (read only) Reset Value: 0x00000000																							
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0															
FIFO_READ_PTR																Reserved								FIFO_READ_PHASE								Reserved FIFO_EMPTY_BYTE FIFO_EMPTY_SAMPLE FIFO_FULL FIFO_ALMOST_FULL FIFO_UNDER_RUN FIFO_OVER_RUN							
Bits	Name		Type	Reset Value	Description																																		
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																		
15..12	Reserved		RO	0x0	Reserved																																		
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																		
7..6	Reserved		RO	0x0	Reserved																																		
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																		
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																		
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																		
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																		
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																		
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																		

3.9.12.10.335 {0x13D0} V6_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-664

Local Address: 0x13D0																Register Type: RO (read only) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.336 {0x13D4} V6_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-665

Local Address: 0x13D4																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																OLDEST_TIMESTAMP_LSB															
Bits		Name						Type	Reset Value						Description																
31..15		Reserved						RO	0x00000						Reserved																
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																

3.9.12.10.337 {0x13E0} V7_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-666

Local Address: 0x13E0																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.338 {0x13E4} V7_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-667

Local Address: 0x13E4														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value	Description																							
31..25	Reserved			RO	0x00	Reserved																							
24	FIFO_ENABLE			RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																							
23..17	Reserved			RO	0x00	Reserved																							
16	FIFO_RESET			WO	0x0	Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																							
15..9	Reserved			RO	0x00	Reserved																							
8	FIFO_PHASE_RESET			WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																							
7..2	Reserved			RO	0x00	Reserved																							
1	FIFO_UNDER_RUN_CLR			WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																							
0	FIFO_OVER_RUN_CLR			WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																							

3.9.12.10.339 {0x13E8} V7_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-668

Local Address: 0x13E8																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.340 {0x13EC} V7_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-669

Local Address: 0x13EC																				Register Type: RO (read only) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.341 {0x13F0} V7_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-670

Local Address: 0x13F0																		Register Type: RO (read only) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0									
OLDEST_TIMESTAMP_MSB																																	
Bits		Name						Type		Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO		0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.342 {0x13F4} V7_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-671

Local Address: 0x13F4																		Register Type: RO (read only) Reset Value: 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Reserved																OLDEST_TIMESTAMP_LSB																			
Bits		Name						Type	Reset Value						Description																				
31..15		Reserved						RO	0x00000						Reserved																				
14..0		OLDEST_TIMESTAMP_LSB						RO	0x0000						Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.343 {0x1400} V8_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-672

Local Address: 0x1400																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.344 {0x1404} V8_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-673

Local Address: 0x1404														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits		Name		Type	Reset Value		Description																						
31..25		Reserved		RO	0x00		Reserved																						
24		FIFO_ENABLE		RW	0x0		Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																						
23..17		Reserved		RO	0x00		Reserved																						
16		FIFO_RESET		WO	0x0		Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																						
15..9		Reserved		RO	0x00		Reserved																						
8		FIFO_PHASE_RESET		WO	0x0		Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																						
7..2		Reserved		RO	0x00		Reserved																						
1		FIFO_UNDER_RUN_CLR		WO	0x0		Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																						
0		FIFO_OVER_RUN_CLR		WO	0x0		Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																						

3.9.12.10.345 {0x1408} V8_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-674

Local Address: 0x1408																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.346 {0x140C} V8_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-675

Local Address: 0x140C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.10.347 {0x1410} V8_R_H_TIMSTAMP0 Details

Table SCU (Sensor Control Unit)-676

Local Address: 0x1410																				Register Type: RO (read only)												
																				Reset Value: 0x00000000												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OLDEST_TIMESTAMP_MSB																																
Bits		Name						Type	Reset Value						Description																	
31..0		OLDEST_TIMESTAMP_MSB						RO	0x00000000						Earliest time stamp (integer part of second) Register for reading out the data in the FIFO Can read out the earliest data in the FIFO																	

3.9.12.10.348 {0x1414} V8_R_H_TIMSTAMP1 Details

Table SCU (Sensor Control Unit)-677

Local Address: 0x1414																		Register Type: RO (read only) Reset Value: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OLDEST_TIMESTAMP_LSB																
Bits		Name				Type	Reset Value				Description																				
31..15		Reserved				RO	0x00000				Reserved																				
14..0		OLDEST_TIMESTAMP_LSB				RO	0x0000				Earliest time stamp (second after the decimal point) Time stamp supporting the earliest data in the FIFO 1/32768 second unit																				

3.9.12.10.349 {0x1420} V9_R_H_CTRL0 Details

Table SCU (Sensor Control Unit)-678

Local Address: 0x1420																Register Type: RW (read/write) Reset Value: 0x0000FFFF															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																WATER_MARK															
Bits		Name						Type	Reset Value							Description															
31..16		Reserved						RO	0x0000							Reserved															
15..0		WATER_MARK						RW	0xFFFF							Watermark value (sample unit) for interrupt/DMA control When the number of valid data in the FIFO is the same as the value or more, an interrupt occurs/a request for DMA transfer begins. The interrupt request only occurs when the corresponding register in INT_ENABLE_MAIN is set to “1”															

3.9.12.10.350 {0x1424} V9_R_H_CTRL1 Details

Table SCU (Sensor Control Unit)-679

Local Address: 0x1424														Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24				23 22 21 20 19 18 17 16				15 14 13 12 11 10 9 8				7 6 5 4 3 2 1 0																	
Reserved				FIFO_ENABLE	Reserved				FIFO_RESET	Reserved				FIFO_PHASE_RESET	Reserved				FIFO_UNDER_RUN_CLR	FIFO_OVER_RUN_CLR									
Bits	Name			Type	Reset Value	Description																							
31..25	Reserved			RO	0x00	Reserved																							
24	FIFO_ENABLE			RW	0x0	Operation permission of the FIFO readout function When “1” is indicated, the operation is permitted. When “0” is indicated, the function operates in a way that the readout side does not recognize that data is written to the FIFO.																							
23..17	Reserved			RO	0x00	Reserved																							
16	FIFO_RESET			WO	0x0	Clear of the FIFO The value of the readout pointer is forced to set the same value of the writing pointer.																							
15..9	Reserved			RO	0x00	Reserved																							
8	FIFO_PHASE_RESET			WO	0x0	Reset of the readout pointer for the FIFO If the readout pointer is in the process of sampling, it is forced to set at the head of the next sample.																							
7..2	Reserved			RO	0x00	Reserved																							
1	FIFO_UNDER_RUN_CLR			WO	0x0	Clearing of the readout error at FIFO empty Clears bits which are read out that the number of valid data of the FIFO is “0”																							
0	FIFO_OVER_RUN_CLR			WO	0x0	Clearing of the write error at FIFO full Clears an error occurred by writing at FIFO full																							

3.9.12.10.351 {0x1428} V9_R_H_STATUS0 Details

Table SCU (Sensor Control Unit)-680

Local Address: 0x1428																Register Type: RO (read only) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																FIFO_AVAIABLE_DATA_NUM															
Bits		Name				Type	Reset Value				Description																				
31..16		Reserved				RO	0x0000				Reserved																				
15..0		FIFO_AVAIABLE_DATA_NUM				RO	0x0000				The number of data stored in the FIFO The number of data remaining in the FIFO Number of sample unit																				

3.9.12.10.352 {0x142C} V9_R_H_STATUS1 Details

Table SCU (Sensor Control Unit)-681

Local Address: 0x142C																Register Type: RO (read only) Reset Value: 0x00000000																					
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0													
FIFO_READ_PTR																Reserved				FIFO_READ_PHASE				Reserved		FIFO_EMPTY_BYTE		FIFO_EMPTY_SAMPLE		FIFO_FULL		FIFO_ALMOST_FULL		FIFO_UNDER_RUN		FIFO_OVER_RUN	
Bits	Name		Type	Reset Value	Description																																
31..16	FIFO_READ_PTR		RO	0x0000	Readout pointer address in the FIFO The next data is read out on the start address Byte unit																																
15..12	Reserved		RO	0x0	Reserved																																
11..8	FIFO_READ_PHASE		RO	0x0	Readout phase of the data in the FIFO The data position in a sample data stored in the FIFO (by Byte unit) “0” indicates that it is delimited of the sample data.																																
7..6	Reserved		RO	0x0	Reserved																																
5	FIFO_EMPTY_BYTE		RO	0x0	Indicates “1” when the number of the valid data byte in the FIFO is “0”																																
4	FIFO_EMPTY_SAMPLE		RO	0x0	Indicates “1” when the number of the valid data sample in the FIFO is “0”																																
3	FIFO_FULL		RO	0x0	Indicates “1” when the FIFO is full																																
2	FIFO_ALMOST_FULL		RO	0x0	Indicates “1” when the number of the valid data in the FIFO is WATER_MARK or more																																
1	FIFO_UNDER_RUN		RO	0x0	Indicates “1”, when the number of the valid data in the FIFO is “0” and the FIFO data is read out.																																
0	FIFO_OVER_RUN		RO	0x0	Indicates that the write occurs at FIFO full Indicates “1” if the write occurs in the FIFO when the FIFO is full																																

3.9.12.11 SCU_RAM Parameters

The following table shows the parameters within the SCU_RAM. Since these parameters are within the memory, they are undefined after a reset is performed, and therefore, their initial values must be set from the CPU or the internal sequencer. When Reserved regions are not initialized by the CPU, undefined values are read out. The SCU_RAM parameters are used to run the firmware that controls the sequencers.

Table SCU (Sensor Control Unit)-682 SCU_RAM Parameters

Parameter Name	Address Offset	RW	Description
SCU_SW_REVISION_DATE	0x0000	RO	Year, month, date that the SCU SW was built
SCU_SW_REVISION_TIME	0x0004	RO	Time that the SCU SW was built
SCU_SW_REVISION_GIT_HASH	0x0008	RO	Configuration management data of the SCU SW
SEQ_SRC_SEL	0x000c	RW	Source setting of the sequencer
Reserved	0x0010		Reserved
Reserved	0x0014 to 0x001c		Reserved
SEQ_PROPERTY_n	0x0020 + n x 0x20	RW	Attribute settings of sequencer n (n = 0, ..., 9)
SEQ_OUT_FORMAT_n	0x0024 + n x 0x20	RW	Output format setting of sequencer n (n = 0, ..., 9)
SEQ_MATH_PROC_OFST_GAIN_n _m	0x0028 + n x 0x04 + m x 0x20	RW	Offset value and gain value of vector element n of sequencer m (n = 0, ..., 2, m = 0, ..., 9) Corresponds to n = 0: X value, n = 1: Y value, n = 2: Z value
Reserved	0x0034 + n x 0x20 to 0x003c + n x 0x20		Reserved (n = 0, ..., 9)
SEQ_INSTRUCTION_n	0x0160 + n x 0x04	RW	Sequencer n instructions (n = 0, ..., 127)
ADC_PROPERTY	0x0260	RW	Attribute settings of ADC
ADC_MATH_PROC_OFST_GAIN_n	0x0264 + n x 0x04	RW	Offset value and gain value of ADC (n = 0, ..., 6)
FIFO_WRITE_EVENT_CTRL_n	0x0280 + n x 0x04	RW	Event control setting of FIFO (n = 0, ..., 14)
FIFO_SRAM_POWER_CTRL	0x02c0	RW	Power supply control setting of SRAM for FIFO
SYNCHRO_CPU2iSoP	0x02c4	RW	Sequencer ID that issues interrupt upon completion or suspension
SYNCHRO_iSoP2CPU	0x02c8	RW	After the sequencer ID suspend interrupt, if the sequencer is executed, the error is notified
Reserved	0x02c4 to 0x02c8		Reserved
SEQ_RAM_OUT_n_READ_DATA_ m	0x02cc + n x 0x20 + m x 0x04	RW	Data read out from sensor by One-shot Sequencer (n = 0, ..., 2, m = 0, ..., 3)
SCU_SW_STATUS	0x02fc to 0x310	RO	Status flag of firmware of SCU internal sequencer

			For debugging
SCU_FIFO_COPY_INFO_n	0x0314 + n x 0x04	RW	Copy enable flag and copy destination Write FIFO ID of write partition

3.9.12.11.1 SCU_SW_REVISION_DATE

Table SCU (Sensor Control Unit)-683

OFFSET: 0x0000

NAME	Field Name	Bit	RW	Description
SCU_SW_REVISION_DATE		[31:0]	RO	Year, month, and date that SCU SW was built. The YYYYMMDD can be obtained on hexadecimal. (E.g. 20140819)

This parameter must be written during startup of the internal sequencer and cannot be updated later.

3.9.12.11.2 SCU_SW_REVISION_TIME

Table SCU (Sensor Control Unit)-684

OFFSET: 0x0004

NAME	Field Name	Bit	RW	Description
SCU_SW_REVISION_TIME	Reserved	[31:24]		Reserved
		[23:0]	RO	Time that the SCU SW was built. The HHMMSS can be obtained in hexadecimal. (E.g. 100615)

This parameter must be written during startup of the internal sequencer and cannot be updated later.

3.9.12.11.3 SCU_SW_REVISION_GIT_HASH

Table SCU (Sensor Control Unit)-685

OFFSET: 0x0008

NAME	Field Name	Bit	RW	Description
SCU_SW_REVISION_GIT_HASH	Reserved	[31:28]		Reserved
		[27:0]	RO	Configuration management information of the SCU SW. The leading seven characters of the git hash value can be obtained in hexadecimal. (E.g. 8b447cd)

This parameter must be written during startup of the internal sequencer and cannot be updated later.

3.9.12.11.4 SEQ_SRC_SEL

Table SCU (Sensor Control Unit)-686

OFFSET: 0x000c

NAME	Field Name	Bit	RW	Description
SEQ_SRC_SEL	Reserved	[31:30]		Reserved
	I2C1_SRC_SEL	[29:20]	RW	Selects the I2C1 sequencer using each bit. (When the I2C1 sequencer is 4 or 6, select 0x50)
	I2C0_SRC_SEL	[19:10]	RW	Selects the I2C0 sequencer using each bit. (When the I2C0 sequencer is 3 or 5, select 0x28)
	SPI_SRC_SEL	[9:0]	RW	Selects the SPI sequencer using each bit. (When the SPI sequencer is 0,1, or 2, select 0x07)

Each bit of this parameter cannot be written when the corresponding sequencer is in operation.

3.9.12.11.5 SEQ_PROPERTY_n

Table SCU (Sensor Control Unit)-687

OFFSET: 0x0020 + n x 0x20 (n = 0, ..., 9)

NAME	Field Name	Bit	RW	Description
SEQ_PROPERTY_ n	Reserved	[31:29]		Reserved
	INST_LEN	[28:24]	RW	Sets the number of sequence commands of the sequencer. "0" corresponds to 1 command. (0 to 31)
	INST_OFST	[22:16]	RW	Sets the start offset of the sequence command of the sequencer. "0" corresponds to no offset. (0 to 127)
	SEQ_OUT_SEL	[13:12]	RW	Sets the writing destination of the data read out from the sensor. 0: FIFO 1: SEQ_RAM_OUT_0 2: SEQ_RAM_OUT_1 3: SEQ_RAM_OUT_2
	SEQ_SRC_SEL_ SUB	[10:0]	RW	Sets the supplementary information of the data source of the sequencer. When SRC_SEL_0 is "0": SPI SlaveSelect ID(0 to 2) When SRC_SEL_1 is "1" or "2": I2C SlaveAddress

This parameter cannot be rewritten when the corresponding sequencer n is in operation.

3.9.12.11.6 SEQ_OUT_FORMAT_n

Table SCU (Sensor Control Unit)-688

OFFSET: 0x0024 + n x 0x20 (n = 0, ..., 9)

NAME	Field Name	Bit	RW	Description
SEQ_OUT_FORMAT_n	Reserved	[31:30]		Reserved
	MATH_WRITE_VEC_ELE_NUM	[29:28]	RW	Format for writing to the MATH_PROC. Number of vector elements. "0" corresponds to one element. Set this from "0" to "2".
	MATH_WRITE_STAR_T_OFST	[26:24]	RW	Format for writing to the MATH_PROC. The data to process is selected using the number of Bytes from the start of the reading buffer. "0" corresponds to no offset. (0 to 7)
	Reserved	[23]		Reserved
	MATH_WRITE_SHIF_T_SIZE	[22:20]	RW	Format for writing to the MATH_PROC. Selects the amount of left bit shift of the 16 bit data. "1" corresponds to 1 bit shift (0 to 7)
	Reserved	[19:15]		Reserved
	MATH_WRITE_BYTE_SWAPT	[16]	RW	Format for writing to the MATH_PROC. Set to "1" when swapping 8 bit 2 Byte data to 16 bits
	Reserved	[15:8]		Reserved
	FIFO_WRITE_LEN	[7:4]	RW	Selects how many Bytes of data read out from the sensor to write to the FIFO. "0" means 1 Byte (0 to 15)
	FIFO_WRITE_START_OFST	[3:0]	RW	Selects from which Byte of data read out from the sensor to start writing to the FIFO. "0" means 1 Byte (0 to 15)

Each bit of this parameter cannot be rewritten when the corresponding sequencer n is in operation.

3.9.12.11.7 SEQ_MATH_PROC_OFST_GAIN_n_m

Table SCU (Sensor Control Unit)-689

OFFSET: 0x0028 + n x 0x04 + m x 0x20

NAME	Field Name	Bit	RW	Description
SEQ_MATH_PROC_OFST_GAIN_n_m	GAIN_n	[31:16]	RW	Gain value of vector n of sequencer m (n = 0, ..., 2, m = 0, ..., 9)
	OFST_n	[15:0]	RW	Offset value of vector n of sequencer m (n = 0, ..., 2, m = 0, ..., 9)

Each bit of this parameter can be rewritten when its corresponding sequencer m is in operation.

3.9.12.11.8 SEQ_INSTRUCTION_n

Table SCU (Sensor Control Unit)-690)

OFFSET: 0x0264 + n x 0x02 (n = 0, ..., 127)

NAME	Field Name	Bit	RW	Description
SEQ_INSTRUCTION_n	INSTRUCTION	[15:0]	RW	Sequencer instructions

This parameter cannot be rewritten when the corresponding sequencer is in operation.

The following table shows the instruction formats.

(the value in the first row indicates the bit position)

Table SCU (Sensor Control Unit)-691 Sequencer Instruction Formats

INST. NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RX	0	REPEAT_COUNT			TERMIN ATE	RESTA RT	STOP	IS_READ	WDATA							
I2C_SLAVE	1	0	0	IS_10_BITS	0		SLAVE_ADDRESS									
WAIT	1	1	0	0					WAIT_COUNT							
RESERVED	1	1	1	Reserved												

TX_RX

Instructions for Tx or Rx transfer

- REPEAT_COUNT is the number of times the instruction is repeated. The actual number of repeats - 1 is set.
- When TERMINATE is “1”, the sequencer is completed within the main loop being executed after the data transfer has been completed. After confirming the data, the sequencer executes instructions from the next instruction after TERMINATE during the next execution.
[Caution]When I2C command is executed only writing or the last command of I2C command strings is “write”, you cannot set TERMINATE to “1”.
- When RESTART is “1”, the transfer starts by the RESTART condition (this is ignored in SPI transfers).
- When STOP is “1”, STOP of I2C is executed after the transfer (this is ignored in SPI transfers).
- When RESTART and STOP are both “1”, the transfer starts at RESTART and completes at STOP.
- When IS_READ is “1”, this indicates Rx transfer, when “0”, it indicates Tx transfer.
- WDATA is writing data.

I2C_SLAVE

Instructions that set the I2C slave address (this is ignored in SPI transfers).

- When IS_10_BITS is “1”, this indicates the 10 bit addressing mode.

- SLAVE_ADDRESS is the slave address.

WAIT

Instruction to insert WAIT

- The sequencer waits for the number of main loops which is set to WAIT_COUNT and then executes the instruction. Set the actual number of waits – 1.

RESERVED

The values written to Reserved are ignored.

3.9.12.11.9 ADC_PROPERTY

Table SCU (Sensor Control Unit)-692

OFFSET:0x0260

NAME	Field Name	Bit	RW	Description
ADC_PROPERTY	Reserved	[31:30]		Reserved
	HPADC1_ENABLE	[29]	RW	When using the sequencer to read out values from the HPADC1, this is “1”.
	HPADC0_ENABLE	[28]	RW	When using the sequencer to read out values from the HPADC0, this is “1”.
	LPADC3_ENABLE	[27]	RW	When using the sequencer to read out values from the LPADC3, this is “1”.
	LPADC2_ENABLE	[26]	RW	When using the sequencer to read out values from the LPADC2, this is “1”.
	LPADC1_ENABLE*1	[25]	RW	When using the sequencer to read out values from the LPADC1, this is “1”.
	LPADC0_ENABLE	[24]	RW	When using the sequencer to read out values from the LPADC0, this is “1”.
	HPADC1_FIFO_WRITE_ID	[23:20]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the HPADC1 is written
	HPADC0_FIFO_WRITE_ID	[19:16]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the HPADC0 is written
	LPADC3_FIFO_WRITE_ID	[15:12]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the LPADC3 is written
	LPADC2_FIFO_WRITE_ID	[11:8]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the LPADC2 is written
	LPADC1_FIFO_WRITE_ID	[7:4]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the LPADC1 is written
	LPADC0_FIFO_WRITE_ID	[3:0]	RW	Selects the FIFO_ID (0 to 15) to which data read out from the LPADC0 is written

- Only *_ENABLE of this parameter can be rewritten during operation of the ADC. To rewrite only *_ENABLE, Read/Modify/Write access is required.

The following tables shows the FIFO_IDs and the FIFOs linked to FIFO_ID.

Table SCU (Sensor Control Unit)-693 FIFO_IDs and the FIFOs linked to FIFO_ID

FIFO_ID	FIFO	
0	D0_W0_S	
1	D0_W1_S	Prohibited setting at ADC_PRIORITY
2	D0_W2_S	Prohibited setting at ADC_PRIORITY
3	D0_W3_S	Prohibited setting at ADC_PRIORITY
4	D1_W0_S	
5	D1_W1_S	Prohibited setting at ADC_PRIORITY
6	D1_W2_S	Prohibited setting at ADC_PRIORITY
7	D1_W3_S	Prohibited setting at ADC_PRIORITY
8	N0_W_S	
9	N1_W_S	
10	N2_W_S	
11	N3_W_S	
12	N4_W_S	
13	N5_W_S	
14	N6_W_S	
15	N7_W_S	

3.9.12.11.10 ADC_MATH_PROC_OFST_GAIN_n

Table SCU (Sensor Control Unit)-694

OFFSET: 0x0264 + n x 0x04 (n = 0, ..., 6)

NAME	Field Name	Bit	RW	Description
ADC_MATH_PROC_OFST_GAIN_n	GAIN	[31:30]	RW	n = 0: LPADC0 gain value (X) n = 1: LPADC1 gain value (X) n = 2: LPADC2 gain value (X) n = 3: LPADC3 gain value (X) n = 4: HPADC0 gain value (X) n = 5: HPADC0 gain value (Y) n = 6: HPADC1 gain value (X)

	OFST	[29:20]	RW	n = 0: LPADC0 offset value (X) n = 1: LPADC1 offset value (X) n = 2: LPADC2 offset value (X) n = 3: LPADC3 offset value (X) n = 4: HPADC0 offset value (X) n = 5: HPADC0 offset value (Y) n = 6: HPADC1 offset value (X)

Each bit of this parameter can be rewritten when the ADC is in operation.

3.9.12.11.11 FIFO_WRITE_EVENT_CTRL_n

Table SCU (Sensor Control Unit)-695

OFFSET: 0x0280 + n x 0x04 (n = 0, ..., 14)

NAME	Field Name	Bit	RW	Description
FIFO_WRITE_EVENT_CTRL_n	Reserved	[31:25]		Reserved
	OUTPUT_8BITS	[24]	RW	Set to "1" when writing only the upper 8 bits of the results from the Math Function to the FIFO.
	Reserved	[23:20]		Reserved
	WRITE_SAMPLE_NUM	[19:8]	RW	When WRITE_CTRL is "2", if selected condition is satisfied, the number of samples selected here are written to the FIFO. "0" means one time. (0 to 4095)
	Reserved	[7:6]		Reserved
	EVENT_ID	[5:4]		When WRITE_CTRL is "1" or "2", the condition ID selected here is referenced. Select from 0 to 2.
	Reserved	[3:2]		Reserved
	WRITE_CTRL	[1:0]		0: Always writes. 1: Does not write until the condition selected by the EVENT_ID is satisfied, and starts writing after the condition is satisfied. 2: Writes until the condition selected by the EVENT_ID is satisfied, and after the condition is satisfied, writes the number of samples selected by WRITE_SAMPLE_NUM. 3: Never writes (assumes use only for conditional statement)

Each bit of this parameter cannot be rewritten when the corresponding sequencer n is in operation.

n corresponds to the following Write FIFOs.

n = 0, 1, 2, 3	D0_W0_S, D0_W1_S, D0_W2_S, D0_W3_S
n = 4, 5, 6, 7	D1_W0_S, D1_W1_S, D1_W2_S, D1_W3_S
n = 8, 9, 10, 11, 12, 13, 14, 15	N0_W_S, N1_W_S, N2_W_S, N3_W_S, N4_W_S, N5_W_S, N6_W_S, N7_W_S

3.9.12.11.12 FIFO_SRAM_POWER_CTRL

Table SCU (Sensor Control Unit)-696

OFFSET: 0x02c0

NAME	Field Name	Bit	RW	Description
FIFO_SRAM_POWER_CTRL	Reserved	[31:25]		Reserved
	PW_STT_IGNORE1	[24]	RW	When writing data to the FIFO, SEQ ignores the power supply status of the later-half 32 Kbytes of FIFO SRAM.
	Reserved	[23:17]		Reserved
	PW_STT_IGNORE0	[16]	RW	When writing data to the FIFO, SEQ ignores the power supply status of the first-half 8 KBytes of FIFO SRAM.
	Reserved	[15:9]		Reserved
	PW_CTRL_EN1	[8]	RW	Performs power down control of the later-half 32 KBytes region of the FIFO SRAM. Turns ON the SRAM when any of the sequencers within the SCU starts up, and switches to the low power mode which holds values of SRAM when writing to the FIFO is completed.
	Reserved	[7:1]		Reserved
	PW_CTRL_EN0	[0]	RW	Performs power down control of the first-half 8 KBytes region of the FIFO SRAM. Turns ON the SRAM when any of the sequencers within the SCU starts up, and switches to the low power mode which holds values of SRAM when writing to the FIFO is completed.

Power supply control of the FIFO by the SCU is not supported. Neither turn OFF nor set the FIFO power supply to retention during operation of the SCU.

3.9.12.11.13 SEQ_RAM_OUT_n_READ_DATA_m

Table SCU (Sensor Control Unit)-697

OFFSET: 0x02cc + n x 0x20 + m x 0x040 (n = 0, ..., 2, m = 0, ..., 3)

NAME	Field Name	Bit	RW	Description

SEQ_RAM_OUT_n_ READ_DATA_m	DATA3	[31:24]	RO	The (m x 4 + 4) th Byte of the data read out from the One-shot Sequencer n
	DATA2	[23:16]	RO	The (m x 4 + 3) th Byte of the data read out from the One-shot Sequencer n
	DATA1	[15:8]	RO	The (m x 4 + 2) th Byte of the data read out from the One-shot Sequencer n
	DATA0	[7:0]	RO	The (m x 4 + 1) th Byte of the data read out from the One-shot Sequencer n

n corresponds to the channel of the One-shot Sequencer, and three channels of One-shot Sequencer can be used.

3.9.12.11.14 SYNCHRO_CPU2iSoP

Table SCU (Sensor Control Unit)-698

OFFSET:0x02c4

NAME	Field Name	Bit	RW	Description
SYNCHRO_CPU2iSoP	Reserved	[31:4]		Reserved
	SEQ_ID	[3:0]	RW	The sequencer ID that raises an interrupt at completion or suspension

The following describes the procedures of sequencer complete interrupt request.

- (1) Sequencer completion request (change the bit of the corresponding sequencer of START_MODE0 within SCU_REG from “1” to “0”)
- (2) Check that Sleep setting is released. If not released, set HPADC0_ACCESS_INHIBIT_REQ within SCU_REG to “1” (SLEEP release and prohibition)
- (3) Clear the SCU interrupt factor
- (4) Disable the iSoP3 IRQ interrupt mask
- (5) Set the complete/suspend request sequencer number to the SYNCHRO_CPU2iSoP
- (6) Set LPADC_ACCESS_INHIBIT_REQ within the SCU_REG to “1” (complete interrupt request)
- (7) Wait for the interrupt
- (8) Within the following interrupt context:
 - (i) Set LPADC_ACCESS_INHIBIT_REQ to “0” (release the complete interrupt request)
 - (ii) Set the iSoP3 IRQ interrupt mask
 - (iii) Clear the interrupt factor
- (9) When SLEEP needs to be enabled, set HPADC0_ACCESS_INHIBIT_REQ to “0” (SLEEP enable)
- (10) End of procedure

The following describes the procedures of sequencer suspend interrupts.

- (1) Set the HPADC0_ACCESS_INHIBIT_REQ to “1” (SCU SLEEP release and prohibition)
- (2) Clear the SCU interrupt factor
- (3) Disable the iSoP3 IRQ interrupt mask
- (4) Set the complete/suspend request sequencer number to the SYNCHRO_CPU2iSoP
- (5) Set the HPADC1_ACCESS_INHIBIT_REQ to “1” (suspend interrupt request)
- (6) Wait for the interrupt
- (7) Within the following interrupt context:
 - (i) Update the MATH_PROC setting (when required)
 - (ii) Set HPADC1_ACCESS_INHIBIT_REQ to “0”
 - (iii) Set the iSoP3 IRQ interrupt mask
 - (iv) Interrupt factor clear
- (8) Check whether there is “1” in sample data loss flag (SCU_RAM internal parameter SYNCHRO_iSoP2CPU (refer to Section 3.9.12.11)). if there is “1”, there may be sample data loss. Perform readout twice, and after checking, clear the sample data loss flag to "0".
- (9) Set HPADC0_ACCESS_INHIBIT_REQ to “0” (SLEEP enable)
- (10) End of the procedure

3.9.12.11.15 SYNCHRO_iSoP2CPU

Table SCU (Sensor Control Unit)-699

OFFSET: 0x02c8

NAME	Field Name	Bit	RW	Description
SYNCHRO_iSoP2CPU	Reserved	[31:30]		Reserved
	SEQ_ID	[0]	RW	After the sequencer ID suspend interrupt, if the sequencer is executed, the error is notified “1” means an error The internal sequencer sets “1” when an error is detected but does not return this to “0” (the CPU needs to return it to “0”)

Follow the description in Section 3.9.12.11.14 and perform readout and clear according to the procedure.

3.9.12.11.16 SCU_FIFO_COPY_INFO_n

OFFSET: 0x0314 + n x 0x04 (n = 0, 1, ..., 9)

NAME	Field Name	Bit	RW	Description
SCU_FIFO_COPY_INFO_n	Reserved	[31:6]		Reserved
	COPY_ID	[5:1]	RW	The copy destination FIFO_ID (ignored when the enable flag of the 0 th bit is negated) of the write partition of sequencer n

	COPY_ENABLE	[0]	RW	The copy enable flag of the write partition of sequencer n

Each bit of this parameter can be rewritten when the corresponding sequencer n is in operation.

3.9.13 SCU Control Sequence

The following describes the control sequence. For details on the control, refer to Section 3.9.13.6.

3.9.13.1 Power Supply Startup to Initialization

Power supply startup to initialization is performed by the following procedure.

- (1) PWD_SCU power supply On
- (2) XOSC power supply On
- (3) RCOSC power supply On
- (4) LPADC, HPADC power supply On
- (5) PWD_SCU reset release
- (6) LPADC functional block reset release
- (7) HPADC functional block reset release
- (8) XOSC, RCOSC clock set
- (9) PWD_SCU clock set
- (10) SPI clock supply start
- (11) I2C0, I2C1 clock supply start
- (12) LPADC clock supply start
- (13) HPADC clock supply start
- (14) LPADC, HPADC operation enable
- (15) Sensor interrupt input terminal set
- (16) SPI terminal set
- (17) I2C0 terminal set
- (18) I2C1 terminal set
- (19) LPADC, HPADC terminal set
- (20) PWM terminal set
- (21) SCU_REG sequencer-related set
- (22) Program download to SEQ_IRAM
- (23) SEQ_DRAM sequencer-related set
- (24) SCU_FIFO initialization
- (25) SPI sequencer operation initial value set
- (26) I2C0 sequencer operation initial value set
- (27) I2C1 sequencer operation initial value set

- (28) LPADC0 data rate set
- (29) LPADC1 data rate set
- (30) LPADC2 data rate set
- (31) LPADC3 data rate set
- (32) HPADC0 data rate set
- (33) HPADC1 data rate set
- (34) Sequencer boot wait
- (35) Sequencer startup
- (36) LPADC data output enable
- (37) HPADC0 data output enable
- (38) HPADC1 data output enable

3.9.13.2 Power Source Turn OFF

Power supply turn OFF is performed by the following procedures.

- (1) LPADC data output disable
- (2) HPADC0 data output disable
- (3) HPADC1 data output disable
- (4) Sequencer suspend
- (5) Sequencer reset
- (6) LPADC, HPADC operation suspend
- (7) RCOSC, XOSC clock supply stop
- (8) LPADC clock supply stop
- (9) HPADC clock supply stop
- (10) I2C clock supply stop
- (11) SPI clock supply stop
- (12) SCU clock supply stop
- (13) HPADC power supply stop
- (14) LPADC power supply stop
- (15) PWD_SCU power supply stop

3.9.13.3 Sequencer Initialization

Sequencer initialization is performed by the following procedures.

- (1) Sequencer, SEQ_IRAM, SEQ_DRAM power supply
- (2) Sequencer reset
- (3) FIFO initialization
- (4) START_CTRL related register set
- (5) MATH_PROC related register set

- (6) Writing program to SEQ_IRAM
- (7) Writing setting and initial value to SEQ_DRAM
- (8) Sequencer clock stop
- (9) Sequencer reset release
- (10) Sequencer clock supply start
- (11) SPI sequencer operation initial value set
- (12) I2C0 sequencer operation initial value set
- (13) I2C1 sequencer operation initial value set
- (14) Sequencer boot completion wait (optional)
- (15) Sequencer startup
- (16) LPADC operation start
- (17) HPADC0 operation start
- (18) HPADC1 operation start

3.9.13.4 SPI/I2C/ADC Control

For the settings of SPI, I2C0, I2C1, LPADC, HPADC0, and HPADC1, refer to the following Sections.

- SPI sequencer operation initial settings: Section 3.9.13.6.3
- I2C0 sequencer operation initial settings: Section 3.9.13.6.5
- I2C1 sequencer operation initial settings: Section 3.9.13.6.5
- LPADC operation parameter settings: Section 3.9.13.6.6
- LPADC data output start: Section 3.9.13.6.6
- LPADC conversion settings: Section 3.9.13.6.6
- HPADC0 operation parameter settings: Section 3.9.13.6.7
- HPADC0 data output start: Section 3.9.13.6.7
- HPADC1 operation parameter settings: Section 3.9.13.6.8
- HPADC1 data output start settings: Section 3.9.13.6.8

3.9.13.5 FIFO Control

For the following FIFO control procedures, refer to Section 3.9.13.6.9.

- Writing side initial settings
- Readout side initial settings
- FIFO writing process
- FIFO readout process
- Transition process to FIFO (8 KByte) Retention
- Transition process to FIFO (8 KByte) All On
- Transition process to FIFO (8 KByte) All Off
- Transition process to FIFO (32 KByte) Retention

- Transition process to FIFO (32 KByte) All On
- Transition process to FIFO (32 KByte) All Off

3.9.13.6 Control Setting Details by Function

The following describes the control setting details by function.

3.9.13.6.1 Power Supply Control Power ON

Table SCU (Sensor Control Unit)-700 Power Supply Control Power ON

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
PWD_SCU Power ON	---	---	---	---	---	Refer to the PMU Chapter (3.4)
ON XOSC Power ON	TOPREG	0x0008	[25]	ON_XO_OSC_EN_SET	1'b0	The setting parameters differ depending on the XOSC operation mode (internal oscillation mode or external clock mode). The setting here shows the setting for external clock mode (system configuration using TCXO). For the internal oscillation mode (system configuration using crystal oscillator), set ON_XO_OSC_EN_SET, OFF_XO_OSC_EN_CLR, ON_XO_OSCOUT_EN_SET, and OFF_XO_OSCOUT_EN_CLR to "1'b1", and set ON_XO_EXT_EN_SET and OFF_XO_EXT_EN_CLR to "1'b0".
			[24]	OFF_XO_OSC_EN_CLR	1'b0	
			[20]	ON_XO_OSCOUT_EN_SET	1'b0	
			[19]	OFF_XO_OSCOUT_EN_CLR	1'b0	
			[18]	ON_XO_EXT_EN_SET	1'b1	
			[17]	OFF_XO_EXT_EN_CLR	1'b1	
		0x0584	[23:16]	IXO_LV_I_VA_L3	8'd0	The setting value is differs depending on the oscillation frequency of the crystal oscillator. For external clock mode, set each to "8'd0".
			[15:8]	IXO_LV_I_VA_L1	8'd0	
		0x0004	[17]	WEN_XOSC	1'b1	XOSC power supply control Write Enable
			[1]	XOSC	1'b1	XOSC power ON
RSOSC Power ON	TOPREG	0x0004	[16]	WEN_RCOSC	1'b1	RCOSC power supply control Write Enable
			[0]	RCOSC	1'b1	RSOSC Power ON

LPADC, HPADC Power ON	SCU.AD CIF	0x0018d e40	[0]	LV_CLK_OSC _SEL	-->	The clock source selection setting during the high speed sampling mode 0: XOSC, 1: RCOSC
			[5:4]	LV_CLK_XOS C_DIV	-->	The frequency division setting during the use of the XOSC as clock source 0: divided by 2 1: divided by 3 2: divided by 4 3: divided by 6
		0x0018d e44	[0]	LV_BGR_EN	1'b1	LV BGR circuit enable
		0x0018d e50	[0]	VECTOR_SEL	-->	Enable/disable of two element vector
		0x0018d e80	[0]	LV_CLK_U32_ SEL0	-->	Clock selection 0: High-speed clock 1: Low-speed clock
		0x0018d ec0	[0]	LV_CLK_U32_ SEL1	-->	Clock selection 0: High-speed clock 1: Low-speed clock
		0x0018d f80	[0]	LV_ADC0_SE LSTAGE	1'b0	ADC0 stage selection
			[7:4]	LV_ADC0_DE LAYADJUST	4'b1100	ADC0 internal clock delay amount adjustment signal
		0x0018d fc0	[0]	LV_ADC1_SE LSTAGE	1'b0	ADC0 stage selection
			[7:4]	LV_ADC1_DE LAYADJUST	4'b1100	ADC0 internal clock delay amount adjustment signal
		0x0018d f04	[7:0]	LV_RSV	8'h04	
		0x0018d f00	[0]	LV_SELSTAG E	1'b0	Stage selection
	TOPREG	0x0004	[29]	WEN_LPADC	1'b1	LPADC power supply control Write Enable
			[13]	LPADC	1'b1	LPADC power ON
			[28]	WEN_HPADC	1'b1	HPADC power supply control Write Enable
			[12]	HPADC	1'b1	HPADC power ON

Power ON Common Setting	TOPREG	0x0048	[11:0]	CLR	=12'h00D (Read Modify Write (OR))	Sets the following bits to "1". RMW (OR) [3] I2C interrupt during power supply control [2] Timeout error occurrence interrupt during power supply control [0] Power supply control completion interrupt
		0x004C	[11:0]	MSK	&=12'hFF2 (Read Modify Write (AND))	Sets the following bits to "0". RMW (AND) [3] I2C communication error interrupt during power supply control [2] Timeout error occurrence interrupt during power supply control [0] Power supply control completion interrupt
		0x0030	[0]	POWER_CTRL_ON	1'b1	Power supply control execution note: SRAM for SCU starts operation when power supply for PWD_SCU is turned ON.
PMU Interrupt Wait	---	---	---	---	---	Waits for a power supply control completion interrupt from the PMU
Interrupt Confirmati on	TOPREG	0x0040	[11:0]	STAT	(&=12'h00D)==1	Interrupt Confirmation: Check that only [0] DONE is "1"
PWD_SCU Power ON Wait RCOSC, XOSC, LPADC, HPADC Power ON	TOPREG	0x0048	[11:0]	CLR	= 12'h00D	Sets the following bits to "1". RMW (OR) [3] I2C communication error interrupt during power supply control [2] Timeout error occurrence interrupt during power supply control
		0x004C	[11:0]	MSK	&=12'hFF2	Sets the following bits to "0". RMW (AND) [3] I2C communication error interrupt during power supply control [2] Timeout error occurrence interrupt during power supply control [0] Power supply control completion interrupt
		0x009C	[0]	POWER_CTRL_ON	1'b1	Power supply control execution (All SRAMs start from ON when the PWD_SCU starts up)

Note 1: The setting parameters differ depending on the XOSC operation mode (internal oscillation mode or external clock mode). The ones shown here are the settings of the external clock mode (configuration using TCXO), which are the initial values of the TOPREG.

For the internal oscillation mode (configuration using a crystal oscillator), set ON_XO_OSC_EN_SET, OFF_XO_OSC_EN_CLR, ON_XO_OSCOUT_EN_SET, and OFF_XO_OSCOUT_EN_CLR to "1'b1", and set ON_XO_EXT_EN_SET, and OFF_XO_EXT_EN_CLR to "1'b0".

Caution: The frequencies supported for internal oscillation mode is 26 MHz.

The frequencies supported for external clock mode is 26 MHz.

Note 2: The settings differ for each crystal oscillator frequency. The IXO_LV_I_VAL1 (before oscillation starts) and IXO_LV_I_VAL3 (after changing the current setting) parameter values are tentative values. During external clock mode, set to “8'd0”.

Table SCU (Sensor Control Unit)-701 Main Reset Control

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
PWD_SCU Reset Release	TOPREG	0x0060	[16]	WEN_PWD_SCU	1'b1	PWD_SCU reset control Write Enable
			[0]	PWD_SCU	1'b1	PWD_SCU reset release
LPADC Reset Release	TOPREG	0x0704	[4]	XRST_SCU_LPADC	1'b1	LPADC reset release
HPADC Reset Release	TOPREG	0x0704	[2]	XRST_SCU_HPADC	1'b1	LPADC reset release

For clock control refer to the PMU (3.4) Chapter.

Table SCU (Sensor Control Unit)-702 Sub Reset Control

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
LPADC Operation Enable	SCU.ADC IF	0x0018de00	[0]	LV_ADC_EN	1'b1	LPADC operation enable
		0x0018de10	[0]	SW_RESET	1'b1	FIFO reset
HPADC0 Operation Enable	SCU.ADC IF	0x0018de84	[0]	LV_ADC0_EN	1'b1	HPADC0 operation permission /stop
			[1]	LV_ADC0_REF_EN	1'b1	LPF0 Enable control terminal.
			[2]	LV_LPF0_EN	1'b1	ADC0 REF circuit enable
		0x0018de88	[0]	LV_CLKOUT0_EN	1'b1	ADC0 clock output enable
		0x0018de90	[0]	SW_RESET	1'b1	FIFO reset
HPADC1 Operation Enable	SCU.ADC IF	0x0018dec4	[0]	LV_ADC0_EN	1'b1	HPADC1 operation permission/stop
			[1]	LV_ADC0_REF_EN	1'b1	LPF1 enable control terminal
			[2]	LV_LPF0_EN	1'b1	ADC1 REF circuit enable
		0x0018dec8	[0]	LV_CLKOUT0_EN	1'b1	ADC1 clock output enable
		0x0018ded0	[0]	SW_RESET	1'b1	FIFO reset
Reset	SCU.ADC	0x0018de10	[0]	SW_RESET	==0	Confirms whether turns to “0”

Confirmation	IF	0x0018de90	[0]	SW_RESET	==0	Confirms whether turns to “0”
		0x0018ded0	[0]	SW_RESET	==0	Confirms whether turns to “0”

Table SCU (Sensor Control Unit)-703 AD Conversion Settings

Control Register Location	Address	bit	Name	Setting Value	Descriptions
SCU.ADCIF	0x0018de04	[9:8]	LV_CH_SEL_INV	--> Refer to descriptions	ADCH selector for GNSS (set for only the following operating channels) 2'b00 CH0 2'b01 CH1 2'b10 CH2 2'b11 CH3
		[2:0]	LV_CH_SEL_MODE	--> Refer to descriptions	LPADC channel switching mode 3'b000 CH0 3'b001 CH1 3'b010 CH2 3'b011 CH3 3'b100 CH0 ==>CH1 3'b101 CH0 ==>CH1==>CH2==>CH3

Table SCU (Sensor Control Unit)-704 Startup Settings

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
Sequencer Operation Parameter Settings	SCU.SCU_REG	---	---	---	---	Follow the API
Sequencer Program Download	SCU.SCU_REG	---	---	---	---	Follow the API
Sequencer Operation Parameter Setting	SCU.SCU_REG	---	---	---	---	Follow the API
Interrupt Clear	TOPREG	0x04EC	[21:0]	CLR	= 22'h002000	Sets the following bit to "1" RMW (OR) [13]:CK_SCU_SEQ On/Off
Interrupt Mask	TOPREG	0x04F0	[21:0]	MSK	&= 22'h3FDFFF	Sets the following bit to "0" RMW (AND) [13]:CK_SCU_SEQ On/Off

Sequencer Clock Stop	TOPREG	0x071C	[4]	SCU_REQ	1'b0	PWD_SCU sequencer clock enable (CK_SCU_SEQ)
CRG Interrupt Wait	---	---	---	---	---	Waits for the clock enable completion interrupt from the Clock Reset Generator (CRG)
Interrupt Confirmation	TOPREG	0x04F4	[21:0]	STAT	(&= 22'h002000) != 0	Interrupt confirmation: Confirms that the following bit turns to "1" [13]: CK_SCU_SEQ On/Off
Interrupt Clear	TOPREG	0x04EC	[21:0]	CLR	= 22'h002000	Sets the following bit to "1" RMW (OR) [13]: CK_SCU_SEQ On/Off
Reset Release	TOPREG	0x0704	[7]	XRST_SCU_ISOP	1'b1	
Interrupt Mask	TOPREG	0x04F0	[21:0]	MSK	&= 22'h3FDFFF	Sets the following bit to "0" RMW (AND) [13]: CK_SCU_SEQ On/Off
Clock Supply	TOPREG	0x071C	[4]	SCU_REQ	1'b1	PWD_SCU sequencer clock enable (CK_SCU_SEQ)
CRG Interrupt Wait	---	---	---	---	---	Waits for the clock enable completion interrupt from the CRG
Interrupt Confirmation	TOPREG	0x04F4	[21:0]	STAT	(&= 22'h002000) != 0	Interrupt confirmation: confirms that the following bit turns to "1" [13]: CK_SCU_SEQ On/Off
Interrupt Clear	TOPREG	0x04EC	[21:0]	CLR	= 22'h002000	Sets the following bit to "1" RMW (OR) [13]: CK_SCU_SEQ On/Off
FIFO Partition Setting	SCU.FIFO_REG	---	---	---	---	Refer to Table SCU (Sensor Control Unit)-721, Table SCU (Sensor Control Unit)-722, Table SCU (Sensor Control Unit)-723, Table SCU (Sensor Control Unit)-724
SPI Initial Setting	SCU.SPI	---	---	---	---	Refer to the SPI (3.10) Chapter
I2C0 Initial Settings	SCU.I2C0	---	---	---	---	Refer to the I2C (3.7) Chapter
I2C1 Initial Settings	SCU.I2C1	---	---	---	---	Refer to the I2C (3.7) Chapter

LPADC Operation Parameter Settings	SCU.ADC IF	0x0018d e14	[3:0]	FIFO_WAT ERMARK	4'd8	LPADC FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	LPADC DMA Signal usage enable/disable
			[11:8]	SAMP_RA TIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
LPADC Operation Parameter Settings	SCU.ADC IF	0x0018d e1c	[3:0]	FIFO_WAT ERMARK	4'd8	LPADC FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	LPADC DMA signal usage enable/disable
			[11:8]	SAMP_RA TIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
LPADC Operation Parameter Settings	SCU.ADC IF	0x0018d e20	[3:0]	FIFO_WAT ERMARK	4'd8	LPADC FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	LPADC DMA signal usage enable/disable
			[11:8]	SAMP_RA TIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
LPADC Operation Parameter Settings	SCU.ADC IF	0x0018d e24	[3:0]	FIFO_WAT ERMARK	4'd8	LPADC FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	LPADC DMA signal usage enable/disable
			[11:8]	SAMP_RA TIO	-->	LPADC sampling ratio selection (0: bypass, 1:1/2, -, 15:1/32768)
HPADC0 Operation Parameter Settings	SCU.ADC IF	0x0018d e94	[4:0]	FIFO_WAT ERMARK	5'd16	HPADC0 FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	HPADC0 DMA signal usage enable/disable
			[10:8]	DECI_RAT IO	3'd7	HPADC0 decimation ratio selection (0: bypass, 0: 1/2, -, 7: 1/128)
HPADC1 HPADC0 Operation Parameter Settings	SCU.ADC IF	0x0018d ed4	[4:0]	FIFO_WAT ERMARK	5'd16	HPADC1 FIFO Watermark
			[5]	DMA_HS_ EN	1'b0	HPADC1 DMA signal usage enable/disable
			[10:8]	DECI_RAT IO	3'd7	HPADC1 decimation ratio selection (0: bypass, 0: 1/2, -, 7: 1/128)
Sequencer Boot Confirmation	SCU.SCU _REG	0x00195 020	[1]	ENABLE_ READY	(&= 2) != 0	Confirm that the following bit turns to “1”

						[1]: ENABLE_READY (Read Only)
Setting for whole Sequencers operation control	SCU.SCU_REG	0x00195020	[0]	ENABLE_ALL_SEQ	1'b1	Permission/prohibition setting for whole sequencers operations, which can be collectively controlled by this bit
LPADC Data Output Start	SCU.ADCIF	0x0018de18	[3:0]	FIFO_EN	arbitrary	Data output start (Sets "1" in the bit of the required LPADC)
HPADC0 Data Output Start	SCU.ADCIF	0x0018de98	[0]	DECIFIFO_EN	1'b1	Data output start
HPADC1 Data Output Start	SCU.ADCIF	0x0018ded8	[0]	DECIFIFO_EN	1'b1	Data output start

3.9.13.6.2 Power Supply Control Power OFF

Table SCU (Sensor Control Unit)-705 Output Disable Settings

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
LPADC Output Disable	SCU.ADCIF	0x0018de18	[3:0]	FIFO_EN	4'h0	Refer to Table SCU (Sensor Control Unit)-708
HPADC0 Output Disable	SCU.ADCIF	0x0018de98	[0]	DECIFIFO_EN	1'b0	Same as above
HPADC1 Output Disable	SCU.ADCIF	0x0018ded8	[0]	DECIFIFO_EN	1'b0	Same as above
Sequencer Suspend	SCU.SCU_REG	0x00195020	[0]	ENABLE_ALL_SEQ	1'b0	Same as above
wait	---	---	---	---	---	Waits for sequencer suspend
Sequencer Reset	TOPREG	0x1028	[7]	XRST_SCU_ISOP	1'b0	Refer to Table SCU (Sensor Control Unit)-708
LPADC Operation Suspend	SCU.ADCIF	0x0018de00	[0]	LV_ADC_EN	1'b0	Same as above
HPADC0 Operation Suspend	SCU.ADCIF	0x0018de84	[0]	LV_ADC0_EN	1'b0	Same as above
			[1]	LV_ADC0_REF_EN	1'b0	Same as above
			[2]	LV_LPF0_EN	1'b0	Same as above
		0x0018de88	[0]	LV_CLKOUT0_EN	1'b0	Same as above

HPADC1 Suspend	Operation	SCU.ADCIF	0x0018dec4	[0]	LV_ADC1_EN	1'b0	Same as above
				[1]	LV_ADC1_REF_EN	1'b0	Same as above
				[2]	LV_LPF1_EN	1'b0	Same as above
			0x0018dec8	[0]	LV_CLKOUT1_EN	1'b0	Same as above

For clock control during Power OFF or Power OFF control, refer to the PMU Chapter (3.4).

3.9.13.6.3 Sequencer

Table SCU (Sensor Control Unit)-706 Sequencer Startup Settings

Event	Control Register Location	Address	bit	Name	Setting Value	Descriptions
Power Supply	---	---	---	---	---	SRAM power supply Refer to the PMU Chapter (3.4)
Sequencer Reset	TOPREG	0x0704	[7]	XRST_SCU_ISOP	1'b1	
FIFO Initialization	---	---	---	---	---	Refer to Table SCU (Sensor Control Unit)-721
START_CTRL Related Register Settings	SCU.SCU	0x00195028	---	START_CTRL_COMMON	---	Refer to Section 3.9.12.3.5
		0x0019502c	---	START_MODE0	0 (e.g.)	Refer to Section 3.9.12.3.6
		0x00195030	---	START_MODE1	0 (e.g.)	Refer to Section 3.9.12.3.7
		0x00195034	---	START_INTERVAL3_0	0x5432 (e.g.)	Refer to Section 3.9.12.3.8
		0x00195038	---	START_INTERVAL7_4	0x9876 (e.g.)	Refer to Section 3.9.12.3.9
		0x0019503c	---	START_INTERVAL9_8	0x0099 (e.g.)	Refer to Section 3.9.12.3.10
		0x00195040	---	START_PHASE1_0	0x00040002	Refer to Section 3.9.12.3.11
		0x00195044	---	START_PHASE3_2	0x00100008	Refer to Section 3.9.12.3.12

		0x001950 48	---	START_PHASE5_4	0x00400020	Refer to Section 3.9.12.3.13
		0x001950 4c	---	START_PHASE7_6	0x01000080	Refer to Section 3.9.12.3.14
		0x001950 50	---	START_PHASE9_8	0x01000100	Refer to Section 3.9.12.3.15
MATH_PRO C Related Register Settings	SCU.SCU	0x001950 70	---	OFST_GAIN_EN	0x00000311 (e.g.)	Refer to Section 3.9.12.3.20
		0x001950 74	---	UNSIGNED_TO_SIGNED	0x00000300 (e.g.)	Refer to Section 3.9.12.3.21
		0x001950 78	---	DEC_CLR	0x000000F F	Refer to Section 3.9.12.3.22
		0x001950 7c	---	MATHFUNC_CLR	0x00000007	Refer to Section 3.9.12.3.23
		0x001950 84	---	DECIMATION_PARAM0	0x0F0F0F0 0 (e.g.)	Refer to Section 3.9.12.3.25
		0x001950 88	---	DECIMATION_PARAM1	0x0F0F0F0 0 (e.g.)	Refer to Section 3.9.12.3.26
		0x001950 8c	---	MATHFUNC_SEL	0 (e.g.)	Refer to Section 3.9.12.3.27
		0x001950 90	---	MATHFUNC_POS0	0 (e.g.)	Refer to Section 3.9.12.3.28
		0x001950 94	---	MATHFUNC_POS1	0 (e.g.)	Refer to Section 3.9.12.3.29
		0x001950 98	---	MATHFUNC_POS2	0 (e.g.)	Refer to Section 3.9.12.3.30
		0x001950 a0	---	MATHFUNC_PARAM_0_0	0 (e.g.)	Refer to Section 3.9.12.3.31
		0x001950 a4	---	MATHFUNC_PARAM_C0_0_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.32
		0x001950 a8	---	MATHFUNC_PARAM_C0_0_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.33
		0x001950 b0	---	MATHFUNC_PARAM_C1_0_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.34
		0x001950 b4	---	MATHFUNC_PARAM_C1_0_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.35
		0x001950 b8	---	MATHFUNC_PARAM_C2_0_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.36

		0x001950 bc	---	MATHFUNC_PARAM_C2_0_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.37
		0x001950 d0	---	MATHFUNC_PARAM_C3_0_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.38
		0x001950 d4	---	MATHFUNC_PARAM_C3_0_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.39
		0x001950 d8	---	MATHFUNC_PARAM_C4_0_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.40
		0x001950 dc	---	MATHFUNC_PARAM_C4_0_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.41
		0x001950 e0	---	MATHFUNC_PARAM_0_1	0 (e.g.)	Refer to Section 3.9.12.3.42
		0x001950 e4	---	MATHFUNC_PARAM_C0_0_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.43
		0x001950 e8	---	MATHFUNC_PARAM_C0_0_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.44
		0x001950 ec	---	MATHFUNC_PARAM_C1_0_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.45
		0x001950 f0	---	MATHFUNC_PARAM_C1_0_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.46
		0x001950 f4	---	MATHFUNC_PARAM_C2_0_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.47
		0x001950 f8	---	MATHFUNC_PARAM_C2_0_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.48
		0x001950 fc	---	MATHFUNC_PARAM_C3_0_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.49
		0x001951 00	---	MATHFUNC_PARAM_C3_0_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.50
		0x001951 04	---	MATHFUNC_PARAM_C4_0_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.51
		0x001951 08	---	MATHFUNC_PARAM_C4_0_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.52
		0x001951 0c	---	MATHFUNC_PARAM_1_0	0 (e.g.)	Refer to Section 3.9.12.3.53
		0x001951 10	---	MATHFUNC_PARAM_C0_1_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.54
		0x001951 14	---	MATHFUNC_PARAM_C0_1_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.55

		0x001951 18	---	MATHFUNC_PARAM_C1_1_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.56
		0x001951 1c	---	MATHFUNC_PARAM_C1_1_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.57
		0x001951 20	---	MATHFUNC_PARAM_C2_1_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.58
		0x001951 24	---	MATHFUNC_PARAM_C2_1_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.59
		0x001951 28	---	MATHFUNC_PARAM_C3_1_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.60
		0x001951 2c	---	MATHFUNC_PARAM_C3_1_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.61
		0x001951 30	---	MATHFUNC_PARAM_C4_1_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.62
		0x001951 34	---	MATHFUNC_PARAM_C4_1_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.63
		0x001951 38	---	MATHFUNC_PARAM_1_1	0 (e.g.)	Refer to Section 3.9.12.3.64
		0x001951 3c	---	MATHFUNC_PARAM_C0_1_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.65
		0x001951 40	---	MATHFUNC_PARAM_C0_1_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.66
		0x001951 44	---	MATHFUNC_PARAM_C1_1_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.67
		0x001951 48	---	MATHFUNC_PARAM_C1_1_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.68
		0x001951 4c	---	MATHFUNC_PARAM_C2_1_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.69
		0x001951 50	---	MATHFUNC_PARAM_C2_1_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.70
		0x001951 54	---	MATHFUNC_PARAM_C3_1_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.71
		0x001951 58	---	MATHFUNC_PARAM_C3_1_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.72
		0x001951 5c	---	MATHFUNC_PARAM_C4_1_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.73
		0x001951 60	---	MATHFUNC_PARAM_C4_1_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.74

		0x001951 64	---	MATHFUNC_PARAM_2_0	0 (e.g.)	Refer to Section 3.9.12.3.75
		0x001951 68	---	MATHFUNC_PARAM_C0_2_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.76
		0x001951 6c	---	MATHFUNC_PARAM_C0_2_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.77
		0x001951 70	---	MATHFUNC_PARAM_C1_2_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.78
		0x001951 74	---	MATHFUNC_PARAM_C1_2_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.79
		0x001951 78	---	MATHFUNC_PARAM_C2_2_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.80
		0x001951 7c	---	MATHFUNC_PARAM_C2_2_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.81
		0x001951 80	---	MATHFUNC_PARAM_C3_2_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.82
		0x001951 84	---	MATHFUNC_PARAM_C3_2_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.83
		0x001951 88	---	MATHFUNC_PARAM_C4_2_0_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.84
		0x001951 8c	---	MATHFUNC_PARAM_C4_2_0_L SB	0 (e.g.)	Refer to Section 3.9.12.3.85
		0x001951 90	---	MATHFUNC_PARAM_2_1	0 (e.g.)	Refer to Section 3.9.12.3.86
		0x001951 94	---	MATHFUNC_PARAM_C0_2_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.87
		0x001951 98	---	MATHFUNC_PARAM_C0_2_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.88
		0x001951 9c	---	MATHFUNC_PARAM_C1_2_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.89
		0x001951 a0	---	MATHFUNC_PARAM_C1_2_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.90
		0x001951 a4	---	MATHFUNC_PARAM_C2_2_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.91
		0x001951 a8	---	MATHFUNC_PARAM_C2_2_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.92
		0x001951 ac	---	MATHFUNC_PARAM_C3_2_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.93

		0x001951 b0	---	MATHFUNC_PARAM_C3_2_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.94
		0x001951 b4	---	MATHFUNC_PARAM_C4_2_1_ MSB	0 (e.g.)	Refer to Section 3.9.12.3.95
		0x001951 b8	---	MATHFUNC_PARAM_C4_2_1_L SB	0 (e.g.)	Refer to Section 3.9.12.3.96
		0x001951 bc	---	EVENT_PARAM0_THRESH	0 (e.g.)	Refer to Section 3.9.12.3.97
		0x001951 c0	---	EVENT_PARAM0_COUNT0	0 (e.g.)	Refer to Section 3.9.12.3.98
		0x001951 c4	---	EVENT_PARAM0_COUNT1	0 (e.g.)	Refer to Section 3.9.12.3.99
		0x001951 c8	---	EVENT_PARAM0_COUNT2	0 (e.g.)	Refer to Section 3.9.12.3.100
		0x001951 cc	---	EVENT_PARAM1_THRESH	0 (e.g.)	Refer to Section 3.9.12.3.101
		0x001951 d0	---	EVENT_PARAM1_COUNT0	0 (e.g.)	Refer to Section 3.9.12.3.102
		0x001951 d4	---	EVENT_PARAM1_COUNT1	0 (e.g.)	Refer to Section 3.9.12.3.103
		0x001951 d8	---	EVENT_PARAM1_COUNT2	0 (e.g.)	Refer to Section 3.9.12.3.104
		0x001951 dc	---	EVENT_PARAM2_THRESH	0 (e.g.)	Refer to Section 3.9.12.3.105
		0x001951 e0	---	EVENT_PARAM2_COUNT0	0 (e.g.)	Refer to Section 3.9.12.3.106
		0x001951 e4	---	EVENT_PARAM2_COUNT1	0 (e.g.)	Refer to Section 3.9.12.3.107
		0x001951 e8	---	EVENT_PARAM2_COUNT2	0 (e.g.)	Refer to Section 3.9.12.3.108
Power Supply Confirmation of SRAM for Sequencer	TOPREG	0x0214	[5:4]	SCUSEQ (Read Only)	2'd3	optional Confirms 2'd3
Write Program to SEQ_IRAM	SCU.SCU	---	---	---	---	Writes 8 KBytes of data Refer to Figure SCU (Sensor Control

						Unit)-53
Write Setting and Initial Values to SEQ_DRAM	SCU.SCU	---	---	---	---	Writes 512Byte + α . For the address, refer to Figure SCU (Sensor Control Unit)-53.
Clock Stop	TOPREG	0x071c	[5]	SCU_SEQ	1'b0	
Reset Release	TOPREG	0x0704	[7]	XRST_SCU_ISOP	1'b1	
Clock Supply	TOPREG	0x071c	[5]	SCU_SEQ	1'b1	
Initial Settings for SPI Sequencer Operation	SCU.SPI	---	---	---	---	Refer to Section 3.9.13.6.4
Initial Settings for I2C0 Sequencer Operation	SCU.I2C0	---	---	---	---	Refer to Section 3.9.13.6.5
Initial Setting for I2C1 Sequencer Operation	SCU.I2C1	---	---	---	---	Refer to Section 3.9.13.6.5
Boot Completion Wait	SCU.SCU	0x001950 20	[1]	ENABLE_READY (Read Only)	1'b1	optional Confirms "1'b1"
Sequencer Startup	SCU.SCU	0x001950 20	[0]	ENABLE_ALL_SEQ	1'b1	
LPADC Operation Start	SCU.ADC IF	---	---	---	---	Refer to Section 3.9.13.6.6
HPADC0 Operation Start	SCU.ADC IF	---	---	---	---	Refer to Section 3.9.13.6.7
HPADC1 Operation Start	SCU.ADC IF	---	---	---	---	Refer to Section 3.9.13.6.8

Table SCU (Sensor Control Unit)-707 SPI Direct Control from CPU during Sequencer Operation

Event	Control Register Location	Address	bit	Name	Setting Values	Descriptions
Inhibit Request	SCU.SCU	0x00195024	[0]	SPI_ACCESS_INHIBIT_REQ	1'b1	
Request Acceptance Confirmation	SCU.SCU	0x00195024	[8]	SPI_ACCESS_INHIBIT_ACK (Read Only)	1'b1	Confirms that it is "1'b1"
SPI Register Setting	SCU.SPI	---	---	---	as necessary	Refer to Section 3.9.13.6.4
SPI Sequencer Operation Initial Setting	SCU.SPI	---	---	---	---	Refer to Section 3.9.13.6.4
Inhibit Request Release	SCU.SCU	0x00195024	[0]	SPI_ACCESS_INHIBIT_REQ	1'b0	

Table SCU (Sensor Control Unit)-708 I2C0 Direct Control from CPU during Sequencer Operation

Event	Control Register Location	Address	bit	Name	Setting Values	Descriptions
Inhibit Request	SCU.SCU	0x00195024	[1]	I2C0_ACCESS_INHIBIT_REQ	1'b1	
Request Acceptance Confirmation	SCU.SCU	0x00195024	[9]	I2C0_ACCESS_INHIBIT_ACK (Read Only)	1'b1	Confirm that it is "1'b1"
I2C0 Register Setting	SCU.SPI	---	---	---	as necessary	Refer to Section 3.9.13.6.5
I2C0 Sequencer Operation Initial Setting	SCU.SPI	---	---	---	---	Refer to Section 3.9.13.6.5
Inhibit Request Release	SCU.SCU	0x00195024	[1]	I2C0_ACCESS_INHIBIT_REQ	1'b0	

Table SCU (Sensor Control Unit)-709 I2C1 Direct Control from CPU during Sequencer Operation

Event	Control Register Location	Address	bit	Name	Setting Values	Descriptions
Inhibit Request	SCU.SCU	0x00195024	[2]	I2C1_ACCESS_INHIBIT_REQ	1'b1	
Request Acceptance Confirmation	SCU.SCU	0x00195024	[10]	I2C1_ACCESS_INHIBIT_ACK (Read Only)	1'b1	Confirm that it is "1'b1"
I2C1 Register	SCU.SPI	---	---	---	as	Refer to Section

Setting					necessary	3.9.13.6.5
I2C1 Sequencer Operation Initial Setting	SCU.SPI	---	---	---	---	Refer to Section 3.9.13.6.5
Inhibit Request Release	SCU.SCU	0x00195024	[2]	I2C1_ACCESS_INHIBIT_REQ	1'b0	

3.9.13.6.4 SPI Operation Initial Settings

Refer to the SPI Chapter (3.10).

3.9.13.6.5 I2C Operation Initial Settings

For the I2C0 and I2C1 settings, refer to the I2C Chapter (3.7).

3.9.13.6.6 LPADC Settings

For the control register specifications, also refer to the ADC Chapter (3.21).

Table SCU (Sensor Control Unit)-710 LPADC Operation Initial Settings

Address	bit	Name	Setting Values	Description
0x0018d e14	[3:0]	FIFO_WATERMARK	-->	LPADC FIFO Watermark
	[5]	DMA_HS_EN	-->	LPADC DMA signal usage enable/disable
	[11:8]	SAMP_RATIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
0x0018d e1c	[3:0]	FIFO_WATERMARK	-->	LPADC FIFO Watermark
	[5]	DMA_HS_EN	-->	LPADC DMA signal usage enable/disable
	[11:8]	SAMP_RATIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
0x0018d e20	[3:0]	FIFO_WATERMARK	-->	LPADC FIFO Watermark
	[5]	DMA_HS_EN	-->	LPADC DMA signal usage enable/disable
	[11:8]	SAMP_RATIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
0x0018d e24	[3:0]	FIFO_WATERMARK	-->	LPADC FIFO Watermark
	[5]	DMA_HS_EN	-->	LPADC DMA signal usage enable/disable
	[11:8]	SAMP_RATIO	-->	LPADC sampling ratio selection (0: bypass, 1: 1/2, -, 15: 1/32768)
0x0018d e18	[3:0]	FIFO_EN	-->	LPADC FIFO operation enable/disable

0x0018de04	[9:8]	LV_CH_SEL_INV	-->	ADCH selector for GNSS (set for only the following operating channels) 2'b00: CH0 2'b01: CH1 2'b10: CH2 2'b11: CH3
	[2:0]	LV_CH_SEL_MODE	-->	LPADC channel switching mode 3'b000: CH0 3'b001: CH1 3'b010: CH2 3'b011: CH3 3'b100: CH0 ==>CH1 3'b101: CH0 ==>CH1==>CH2==>CH3

3.9.13.6.7 HPADC0 Operation Settings

For the control register specifications, refer to the ADC Chapter (3.21).

Table SCU (Sensor Control Unit)-711 HPADC0 Operation Initial Settings

Address	bit	Name	Setting Values	Descriptions
0x0018de94	[4:0]	FIFO_WATERMARK	-->	HPADC0 FIFO Watermark
	[5]	DMA_HS_EN	-->	HPADC0 DMA signal usage enable/disable
	[10:8]	DECI_RATIO	-->	HPADC0 decimation ratio selection (0: bypass, 1: 1/2, -, 7: 1/128)
0x0018de98	[0]	DECIFIFO_EN	1	HPADC0 Decimation, FIFO operation enable/disable

3.9.13.6.8 HPADC1 Operation Settings

For the control register specifications, refer to the ADC Chapter (3.21).

Table SCU (Sensor Control Unit)-712 HPADC1 Operation Initial Settings

Address	bit	Name	Setting Values	Descriptions
0x0018ded4	[4:0]	FIFO_WATERMARK	-->	HPADC1 FIFO Watermark
	[5]	DMA_HS_EN	-->	HPADC1 DMA signal usage enable/disable
	[10:8]	DECI_RATIO	-->	HPADC1 decimation ratio selection (0: bypass, 1: 1/2, -, 7: 1/128)
0x0018de98	[0]	DECIFIFO_EN	1	HPADC1 Decimation, FIFO operation

				enable/disable

3.9.13.6.9 FIFO Settings

For details on the control registers, refer to Section 3.9.12.10.

Table SCU (Sensor Control Unit)-713 FIFO Writing Side Initial Settings

FIFO Partition	Address	bit	Name	Setting Values	Descriptions
D0_W0_S	0x0018_0000	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_0004	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per samples
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full Sets {STOP_WRITING, OVER_WRITE}
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D0_W1_S	0x0018_0020	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_0024	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D0_W2_S	0x0018_0040	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_0044	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D0_W3_S	0x0018_0060	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_0064	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per samples
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D1_W0_S	0x0018_0080	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_0084	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D1_W1_S	0x0018_00a0	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018_00a4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full

		[16]	FIFO_RESET	1	Resets the FIFO writing side
D1_W2 _S	0x0018 00c0	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 00c4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
D1_W3 _S	0x0018 00e0	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 00e4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N0_W_ S	0x0018 0100	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition start address
	0x0018 0104	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N1_W_ S	0x0018 0120	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0124	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N2_W_ S	0x0018 0140	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0144	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N3_W_ S	0x0018 0160	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0164	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N4_W_ S	0x0018 0180	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0184	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N5_W_ S	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	01a0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size

	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	01a4	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N6_W_ S	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	01c0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	01c4	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
N7_W_ S	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	01e0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	01e4	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
V0_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	0200	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	0204	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0218	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition) This value is added to the LATEST_TIME_STAMP each time writing to the FIFO_WRITE_REG is performed.
V1_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	0220	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	0224	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0238	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition).
V2_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	0240	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	0244	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0258	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition).
V3_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address

C	0260	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	0264	[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIGI full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0278	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition)
V4_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	0280	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0284	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0298	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition)
V5_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	02a0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 02a4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 02b8	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition)
V6_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	02c0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 02c4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 02d8	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition)
V7_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	02e0	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 02e4	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 02f8	[30:16]	TIME_STAMP_INTERVAL		Sets the intervals of FIFO writing (only for virtual sensor partition)
V8_W_ C	0x0018	[31:16]	FIFO_START_OFST		Selects the partition start address
	0300	[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
	0304	[4]	OVERWRITE_IF_FULL		Selects operation mode during FIFO full

V9_W_ C		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0318	[30:16]	TIME_STAMP_INTERV AL		Sets the intervals of FIFO writing (only for virtual sensor partition)
	0x0018 0320	[31:16]	FIFO_START_OFST		Selects the partition start address
		[15:0]	FIFO_PARTITION_SIZE		Selects the partition size
	0x0018 0324	[3:0]	FIFO_SAMPLE_SIZE		Selects the number of Bytes per sample
		[4]	OVERWRITE_IF_FULL		Selects the operation mode during FIFO full
		[16]	FIFO_RESET	1	Resets the FIFO writing side
	0x0018 0338	[30:16]	TIME_STAMP_INTERV AL		Sets the intervals of FIFO writing (only for virtual sensor partition).

Table SCU (Sensor Control Unit)-714 FIFO Readout Side Initial Settings

FIFO Partition	Address	bit	Name	Setting Values	Descriptions
---	0x00195400	[22:9]	ALMOST_FULL	1	Almost Full Interrupt Permission (optional) [9]D0_R1_C [10]D0_R2_C [11]D1_R1_C [12]D1_R2_C [13]N0_R1_C [14]N1_R1_C [15]N2_R1_C [16]N3_R1_C [17]N4_R1_C [18]N5_R1_C [19]N6_R1_C [20]N7_R1_C [21]D0_R3_CH [22]D1_R3_CH
---	0x00195420	[22:9]	OVER_RUN	1	Enables writing occurrence error interrupt during Full (optional) For bit assignment, refer to ALMOST_FULL
---	0x00195440	[22:9]	UNDER_RUN	1	Enables readout occurrence error interrupt during Empty (optional) For bit assignment, refer to ALMOST_FULL
D0_R1_ C	0x00181000	[15:0]	WATER_MARK		Sets Watermark
	0x00181004	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal 0: disable 1: enable
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission 0: disable 1: enable
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D0_R2_ C	0x00181020	[15:0]	WATER_MARK		Sets Watermark
	0x00181024	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO

D1_R1_ C	0x00181040	[15:0]	WATER_MARK		Sets Watermark
	0x00181044	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D1_R2_ C	0x00181060	[15:0]	WATER_MARK		Sets Watermark
	0x00181064	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N0_R1_ C	0x00181080	[15:0]	WATER_MARK		Sets Watermark
	0x00181084	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N1_R1_ C	0x001810a0	[15:0]	WATER_MARK		Sets Watermark
	0x001810a4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N2_R1_ C	0x001810c0	[15:0]	WATER_MARK		Sets Watermark
	0x001810c4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N3_R1_ C	0x001810e0	[15:0]	WATER_MARK		Sets Watermark
	0x001810e4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N4_R1_ C	0x00181100	[15:0]	WATER_MARK		Sets Watermark
	0x00181104	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N5_R1_ C	0x00181120	[15:0]	WATER_MARK		Sets Watermark
	0x00181124	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal

		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N6_R1_ C	0x00181140	[15:0]	WATER_MARK		Sets Watermark
	0x00181144	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N7_R1_ C	0x00181160	[15:0]	WATER_MARK		Sets Watermark
	0x00181164	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D0_R3_ CH	0x00181180	[15:0]	WATER_MARK		Sets Watermark
	0x00181184	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D1_R3_ CH	0x001811a0	[15:0]	WATER_MARK		Sets Watermark
	0x001811a4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D0_R0_ H	0x001811c0	[15:0]	WATER_MARK		Sets Watermark
	0x001811c4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
D1_R0_ H	0x001811e0	[15:0]	WATER_MARK		Sets Watermark
	0x001811e4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N0_R0_ H	0x00181200	[15:0]	WATER_MARK		Sets Watermark
	0x00181204	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N1_R0_	0x00181220	[15:0]	WATER_MARK		Sets Watermark

H	0x00181224	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N2_R0_	0x00181240	[15:0]	WATER_MARK		Sets Watermark
H	0x00181244	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N3_R0_	0x00181260	[15:0]	WATER_MARK		Sets Watermark
H	0x00181264	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N4_R0_	0x00181280	[15:0]	WATER_MARK		Sets Watermark
H	0x00181284	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N5_R0_	0x001812a0	[15:0]	WATER_MARK		Sets Watermark
H	0x001812a4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N6_R0_	0x001812c0	[15:0]	WATER_MARK		Sets Watermark
H	0x001812c4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
N7_R0_	0x001812e0	[15:0]	WATER_MARK		Sets Watermark
H	0x001812e4	[25]	FIFO_DMA_ENAB LE		Sets output permission of DMA handshake signal
		[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V0_R_H	0x00181300	[15:0]	WATER_MARK		Sets Watermark
	0x00181304	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V1_R_H	0x00181320	[15:0]	WATER_MARK		Sets Watermark

	0x00181324	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V2_R_H	0x00181340	[15:0]	WATER_MARK		Sets Watermark
	0x00181344	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V3_R_H	0x00181360	[15:0]	WATER_MARK		Sets Watermark
	0x00181364	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V4_R_H	0x00181380	[15:0]	WATER_MARK		Sets Watermark
	0x00181384	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V5_R_H	0x001813a0	[15:0]	WATER_MARK		Sets Watermark
	0x001813a4	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V6_R_H	0x001813c0	[15:0]	WATER_MARK		Sets Watermark
	0x001813c4	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V7_R_H	0x001813e0	[15:0]	WATER_MARK		Sets Watermark
	0x001813e4	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V8_R_H	0x00181400	[15:0]	WATER_MARK		Sets Watermark
	0x00181404	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO
V9_R_H	0x00181420	[15:0]	WATER_MARK		Sets Watermark
	0x00181404	[24]	FIFO_ENABLE	1	Readout side FIFO operation permission
		[16]	FIFO_RESET	1	Resets the readout side FIFO

Table SCU (Sensor Control Unit)-715 FIFO Write Processing

FIFO Partition	Address	bit	Name	Setting Values	Descriptions
V0_W_C	0x00180214	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180218	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180208	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write

V1_W_C	0x00180234	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180238	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180228	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V2_W_C	0x00180254	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180258	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180248	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V3_W_C	0x00180274	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180278	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180268	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V4_W_C	0x00180294	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180298	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180288	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V5_W_C	0x001802b4	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x001802b8	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x001802a8	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V6_W_C	0x001802d4	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)

	0x001802d8	[14:0]	LATEST_BASE_TIME STAMP_LSB		optional)
	0x001802c8	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V7_W_C	0x001802f4	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x001802f8	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x001802e8	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V8_W_C	0x00180314	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180318	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180308	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write
V9_W_C	0x00180334	[31:0]	LATEST_BASE_TIME STAMP_MSB		Writes the reference time stamp (1st time is mandatory, 2nd time on is optional)
	0x00180338	[14:0]	LATEST_BASE_TIME STAMP_LSB		
	0x00180328	[3:0]	FIFO_WRITE_PHASE		Confirmation (optional) and readout of the writing phase
	---	---	---	---	FIFO data write

Table SCU (Sensor Control Unit)-716 FIFO Readout Processing

FIFO Partit ion	Address	bit	Name	Setting Values	Descriptions
D0_	---		---	---	FIFO data readout
R1_ C	0x00181010	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181014	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018100c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181004	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018100c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		

	0x00181004	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear
		[1]	FIFO_UNDER_RUN_CLR		(optional)
D0_	---		---	---	FIFO data readout
R2_	0x00181030	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181034	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018102c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181024	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018102c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor
		[1]	FIFO_UNDER_RUN		confirmation (optional)
	0x00181024	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear
		[1]	FIFO_UNDER_RUN_CLR		(optional)
D1_	---		---	---	FIFO data readout
R1_	0x00181050	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181054	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018104c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181044	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018104c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor
		[1]	FIFO_UNDER_RUN		confirmation (optional)
	0x00181044	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear
		[1]	FIFO_UNDER_RUN_CLR		(optional)
D1_	---		---	---	FIFO data readout
R2_	0x00181070	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181074	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018106c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181064	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018106c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor
		[1]	FIFO_UNDER_RUN		confirmation (optional)
	0x00181064	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear
		[1]	FIFO_UNDER_RUN_CLR		(optional)
N0_	---		---	---	FIFO data readout
R1_	0x00181090	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181094	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018108c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181084	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018108c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor
		[1]	FIFO_UNDER_RUN		confirmation (optional)
	0x00181084	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear
		[1]	FIFO_UNDER_RUN_CLR		(optional)

N1_	---		---	---	FIFO data readout
R1_	0x001810b0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x001810b4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001810ac	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001810a4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001810ac	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001810a4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N2_	---		---	---	FIFO data readout
R1_	0x001810d0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x001810d4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001810cc	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001810c4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001810cc	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001810c4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N3_	---		---	---	FIFO data readout
R1_	0x001810f0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x001810f4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001810ec	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001810e4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001810ec	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001810e4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N4_	---		---	---	FIFO data readout
R1_	0x00181110	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181114	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018110c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181104	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018110c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181104	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N5_	---		---	---	FIFO data readout
R1_	0x00181130	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)

C	0x00181134	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018112c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181124	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018112c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181124	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N6_	---		---	---	FIFO data readout
R1_	0x00181150	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181154	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018114c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181144	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018114c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181144	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N7_	---		---	---	FIFO data readout
R1_	0x00181170	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
C	0x00181174	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018116c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181164	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018116c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181164	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
D0_	---		---	---	FIFO data readout
R3_	0x00181190	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
CH	0x00181194	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018118c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181184	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018118c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181184	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
D1_	---		---	---	FIFO data readout
R3_	0x001811b0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
CH	0x001811b4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001811ac	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)

	0x001811a4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001811ac	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001811a4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
D0_	---		---	---	FIFO data readout
R0_ H	0x001811d0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x001811d4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001811cc	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001811c4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001811cc	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001811c4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
D1_	---		---	---	FIFO data readout
R0_ H	0x001811f0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x001811f4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001811ec	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001811e4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001811ec	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001811e4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N0_	---		---	---	FIFO data readout
R0_ H	0x00181210	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181214	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018120c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181204	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018120c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181204	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N1_	---		---	---	FIFO data readout
R0_ H	0x00181230	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181234	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018122c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181224	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018122c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor

		[1]	FIFO_UNDER_RUN		confirmation (optional)
	0x00181224	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N2_	---		---	---	FIFO data readout
R0_	0x00181250	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x00181254	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018124c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181244	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018124c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181244	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N3_	---		---	---	FIFO data readout
R0_	0x00181270	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x00181274	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018126c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181264	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018126c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181264	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N4_	---		---	---	FIFO data readout
R0_	0x00181290	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x00181294	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018128c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181284	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018128c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181284	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N5_	---		---	---	FIFO data readout
R0_	0x001812b0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x001812b4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001812ac	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001812a4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001812ac	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001812a4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear

		[1]	FIFO_UNDER_RUN_CLR		(optional)
N6_	---		---	---	FIFO data readout
R0_	0x001812d0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x001812d4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001812cc	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001812c4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001812cc	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001812c4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
N7_	---		---	---	FIFO data readout
R0_	0x001812f0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
H	0x001812f4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001812ec	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001812e4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001812ec	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001812e4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V0_	---		---	---	FIFO data readout
R_H	0x00181310	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181314	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018130c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181304	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018130c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181304	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V1_	---		---	---	FIFO data readout
R_H	0x00181330	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181334	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018132c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181324	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018132c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181324	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V2_	---		---	---	FIFO data readout

R_H	0x00181350	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181354	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018134c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181344	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018134c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181344	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V3_	---		---	---	FIFO data readout
R_H	0x00181370	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181374	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018136c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181364	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018136c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181364	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V4_	---		---	---	FIFO data readout
R_H	0x00181390	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181394	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018138c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181384	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018138c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181384	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V5_	---		---	---	FIFO data readout
R_H	0x001813b0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x001813b4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001813ac	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001813a4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001813ac	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001813a4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V6_	---		---	---	FIFO data readout
R_H	0x001813d0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x001813d4	[14:0]	OLDEST_TIMESTAMP_LSB		

	0x001813cc	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001813c4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001813cc	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001813c4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V7_	---		---	---	FIFO data readout
R_H	0x001813f0	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x001813f4	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x001813ec	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x001813e4	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x001813ec	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x001813e4	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V8_	---		---	---	FIFO data readout
R_H	0x00181410	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181414	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018140c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181404	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018140c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181404	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		
V9_	---		---	---	FIFO data readout
R_H	0x00181430	[31:0]	OLDEST_TIMESTAMP_MSB		Time stamp readout (optional)
	0x00181434	[14:0]	OLDEST_TIMESTAMP_LSB		
	0x0018142c	[11:8]	FIFO_READ_PHASE		Readout phase confirmation (optional)
	0x00181424	[8]	FIFO_PHASE_RESET		Readout phase reset (optional)
	0x0018142c	[0]	FIFO_OVER_RUN		Abnormality occurrence factor confirmation (optional)
		[1]	FIFO_UNDER_RUN		
	0x00181424	[0]	FIFO_OVER_RUN_CLR		Abnormality occurrence factor clear (optional)
		[1]	FIFO_UNDER_RUN_CLR		

Table SCU (Sensor Control Unit)-717 Transition Process to FIFO (8 KByte) Retention

Control Register Location	Address	bit	Name	Setting Values	Descriptions

TOPREG	0x0018	[1:0]	SCU_FIFO0	1	

Table SCU (Sensor Control Unit)-718 Transition Process to FIFO (8 KByte) All ON

Control Register Location	Address	bit	Name	Setting Values	Descriptions
TOPREG	0x0018	[1:0]	SCU_FIFO0	3	
	0x0214	[1:0]	SCU_FIFO0	---	Status confirmation 11: Normal 10: Prohibited Setting 01: SRAM off 00: Shut Down

Table SCU (Sensor Control Unit)-719 Transition Process to FIFO (8 KByte) ALL OFF

Control Register Location	Address	bit	Name	Setting Values	Descriptions
TOPREG	0x0018	[1:0]	SCU_FIFO0	0	

Table SCU (Sensor Control Unit)-720 Transition Process to FIFO (32 KByte) Retention

Control Register Location	Address	bit	Name	Setting Values	Descriptions
TOPREG	0x0018	[3:2]	SCU_FIFO1	1	

Table SCU (Sensor Control Unit)-721 Transition Process to FIFO (8 KByte) All ON

Control Register Location	Address	bit	Name	Setting Values	Descriptions
TOPREG	0x0018	[3:2]	SCU_FIFO1	3	
	0x0214	[3:2]	SCU_FIFO1	---	Status confirmation 11: Normal 10: Prohibited Setting 01: SRAM off 00: Shut Down

Table SCU (Sensor Control Unit)-722 Transition Process to FIFO (8 KByte) ALL OFF

Control Register Location	Address	bit	Name	Setting Values	Descriptions
TOPREG	0x0018	[3:2]	SCU_FIFO1	0	

3.9.14 Error Handling

The following table shows the SCU errors and the way they should be handled

Table SCU (Sensor Control Unit)-723 Errors and their Handling

Resource	Cause	Notification Method	How to handle on CPU
SPI	SPI transfer timeout (650240 SCU clock cycles elapsed when reading out data from the FIFO)	EXE_ERR interrupt (1 bit per each sequencer)	Check the SPI setting and choose a setting that does not cause timeout.
I2C	A Master On Hold error was returned from the I2C functional block	EXE_ERR interrupt (1 bit per each sequencer)	Check the slave address of the target and perform the transfer again. The I2C functional block is disabled by the firmware of the SCU internal sequencer
Sequencer	Withdrawal of the suspend interrupt request was not in time by the next execution of the MATH_PROC	Within the SCU_RAM SYNCHRO_iSoP2CPU parameter	None. When sample data loss occurs, this can be known by the time stamp shift.
ADCIF	The FIFO for the LPADC ch.n within the ADCIF has overflowed	LPADC_OVER_RUNn (n = 0, ..., 3)	None
ADCIF	The FIFO for the HPADC ch.n within the ADCIF has overflowed	HPADCn_OVER_RUN (n = 1, 2)	None
ADCIF	An abnormal readout from the FIFO within the ADCIF has occurred	ADCIF_READ_ERR	None
ADCIF	The FIFO partition D0_Rn has overflowed	D0_Rn_C_OVER_RUN (n = 1, 2)	None
ADCIF	The FIFO partition D1_Rn has overflowed	D1_Rn_C_OVER_RUN (n = 1, 2)	None
ADCIF	The FIFO partition Nn_R1 has overflowed	Nn_R1_C_OVER_RUN (n = 0, ..., 7)	None
ADCIF	The FIFO partition Dn_R3 has overflowed	Dn_R3_CH_OVER_RUN (n = 0, 1)	None
ADCIF	The FIFO for the LPADC ch.n within the ADCIF was empty but read out	LPADC_UNDER_RUNn (n = 0, ..., 3)	None
ADCIF	The FIFO for the HPADC ch.n within the ADCIF was empty but read out	HPADCn_UNDER_RUN (n = 1, 2)	None
ADCIF	The FIFO partition D0_Rn was empty but read out	D0_Rn_C_UNDER_RUN (n = 1, 2)	None
ADCIF	The FIFO partition D1_Rn was empty but read out	D1_Rn_C_UNDER_RUN (n = 1, 2)	None

ADCIF	The FIFO partition Nn_R1 was empty but read out	Nn_R1_C_UNDER_RUN (n = 0, ..., 7)	None
ADCIF	The FIFO partition Dn_R3 was empty but read out	Dn_R3_CH_UNDER_RUN (n = 0, 1)	None

3.9.15 Restrictions

3.9.15.1 Parameter Initialization and Change Timing

- Overall SCU_RAM
 - The SCU_RAM must be initialized before releasing the reset of the internal sequencer.
 - In general, the parameters within the SCU_RAM can only be changed when the functions of the related internal sequencers are stopped.

For the restrictions on each parameter, refer to the descriptions in Section 3.9.12.11.

- ADC_PROPERTY.*_ENABLE
 - Set ADC_PROPERTY.*_ENABLE to enable before enabling the *_D2.*_EN within the SCU_ADCIF_REG.
 - The SCU_RAM cannot be accessed during SLEEP.

3.9.15.2 Decimation Partition Input Data

The data input to the decimation partition (all paths to the Write FIFOs) must be Calculation Operable Type. This restriction is the same during FORTH_THROUGH mode and when the decimation ratio is 1.

3.9.15.3 Preprocessing of MATH_PROC

During preprocessing of the MATH_PROC, when the flag to convert from Unsigned to Signed is ON, the input performs conversion to 2's complement format as offset binary (the offset is equal to (input value binary maximum value + 1)/2).

The following table shows conversion examples to 2's complement format when 4 bits.

Table SCU (Sensor Control Unit)-724 Conversion to 2's Complement Format (e.g. four bit width)

Decimal	Offset Binary (Binary)		2's complement (Binary)	Decimal
0	000	->	100	-4
1	001	->	101	-3
2	010	->	110	-2
3	011	->	111	-1
4	100	->	000	0
5	101	->	001	1
6	110	->	010	2
7	111	->	011	3

3.9.15.4 MATH_PROC Parameter Dynamic Change

Some of the MATH_PROC parameters cannot be dynamically changed (when the data is being input/output to/from the MATH_PROC corresponding to the parameter change). Update is possible only when the operation of the corresponding MATH_PROC is suspended (the states other than from when “the data is input to the MATH_PROC to the completion of preparing the data for output”).

The following shows the registers that cannot be dynamically changed.

Table SCU (Sensor Control Unit)-725 MATH_PROC Registers that cannot be Dynamically Changed

Register	Bit Field	Description	Effect of Changing Dynamically
DEC_CLR	DEC0_COMM ON_CLR	Register Clear of DEC0 integrator	The integrator cannot be reset because the initial state of the integrator's counter is enforced
	DEC1_COMM ON_CLR	Register Clear of DEC1 integrator	Same as above
DECIMAT	N1	Decimation ratio	The decimation ratio cannot be dynamically changed since the data output is sometimes delayed. Also, decimation cannot be turned ON from bypass mode.
ION_PAR AM0	FORCE_THR OUGH1	When set to “1”, regardless of the N1 value, bypass is enforced with no sample delay	
	N2	Decimation ratio	Same as above

	FORCE_THROUGH2	When set to "1", regardless of the N1 value, bypass is enforced with no sample delay	Same as above
	N3	Decimation ratio	
	FORCE_THROUGH3	When set to "1", regardless of the N1 value, bypass is enforced with no sample delay	
DECIMATION_PARAMETERS1	N5	Decimation ratio	The decimation ratio cannot be dynamically changed since the data output is sometimes delayed. Also, decimation cannot be turned ON from bypass mode.
	FORCE_THROUGH5	When set to "1", regardless of the N1 value, bypass is enforced with no sample delay	
	N6	Decimation ratio	Same as above
	FORCE_THROUGH6	When set to "1", regardless of the N1 value, bypass is enforced with no sample delay	
	N7	Decimation ratio	Same as above
	FORCE_THROUGH7	When set to "1", regardless of the N1 value, bypass is enforced with no sample delay	
MATHFUNCTION_SELECTOR	WID0	The FIFO Partition ID assigned to Math Function 0	The MATH_FUNCTION cannot be turned ON dynamically since the calculation results sometimes are not output
	MATHE_EN0	Operation permission of Math Function 0	
	WID1	The FIFO Partition ID assigned to Math Function 1	Same as above
	MATHE_EN1	Operation permission of Math Function 1	
	WID2	The FIFO Partition ID assigned to Math Function 2	Same as above
	MATHE_EN2	Operation permission of Math Function 2	

The change of parameters that cannot be dynamically changed must be completed during the period that the MATH_PROC is not operating using SCU-CPU synchronized communication (Section 3.9.9.12).

Also, to change the MATH_PROC settings, the MATH_PROC must be executed at least one more time after once performing rewrite.

3.9.15.5 Using the Decimation Filter in MATH_PROC processing

The decimation filters (two-stage CIC Filter) that can be used for MATH_PROC processing can be applied to the sensor data captured by sequencers SEQ0 and SEQ1.

3.9.15.6 Excess Detection of MATH_PROC Processing

Do not enter a negative value into the excess detector. The detection result will be incorrect. Take measures

such as using the MATHFUNC_SEL register (Section 3.9.12.3.27) to perform normalization processing as a preprocess.

3.9.15.7 Caution upon Directly Controlling the I2C Block from the CPU

The I2C block equipped on the SCU requires an idle time from when Enable is set to the time when the internal state becomes Active. This is done by setting by IC_ENABLE[0] to “1”. During this idle period, master operation will not begin even when data is written to the IC_DATA_CMD. To avoid this, check TX_EMPTY by reading out the register or stop the functional block (set IC_ENABLE[0] to “0”) after checking whether the MST_ACTIVITY changes from “0” to “1”. See the following flowchart for the procedures.

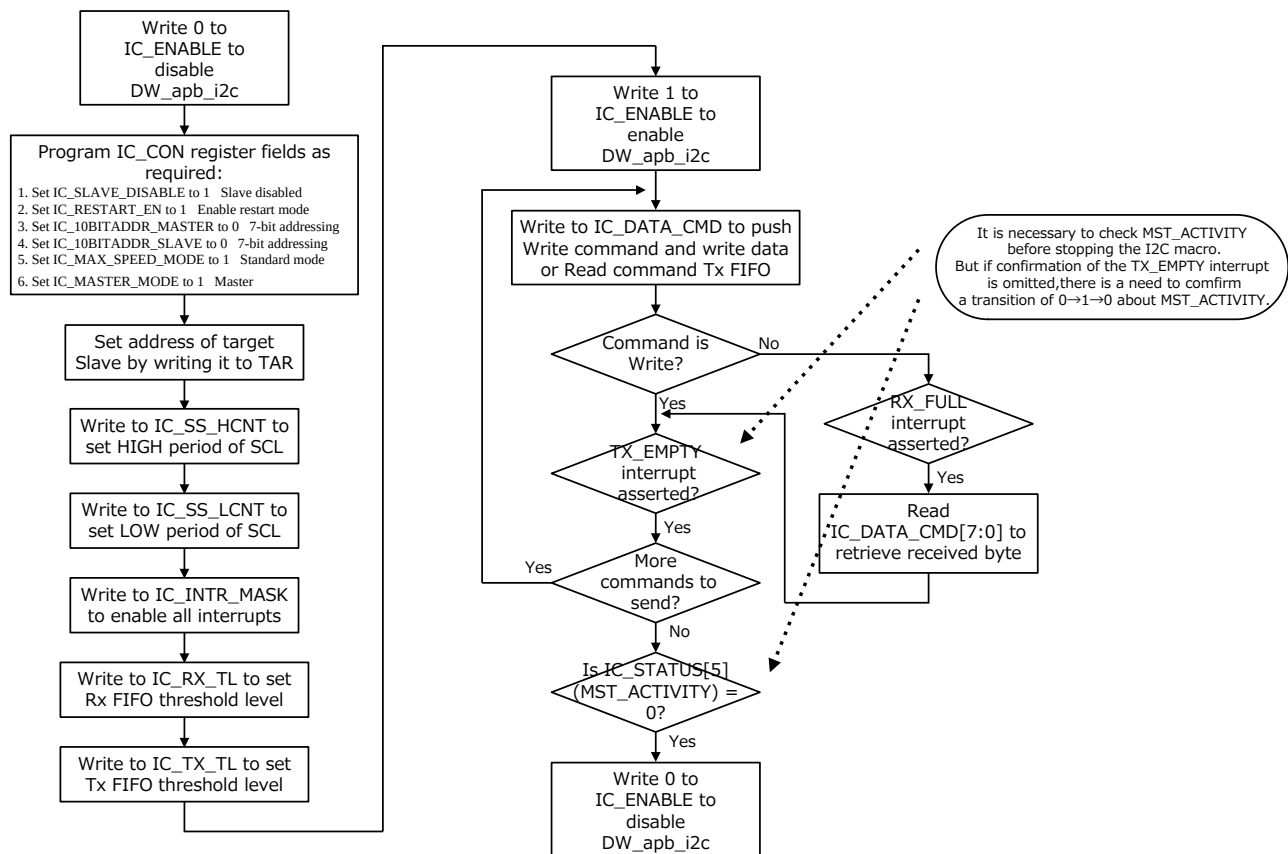


Figure SCU (Sensor Control Unit)-89 I2C Master Control (Example)

3.9.15.8 Sequencer Startup Delay

When the sequencer is first started up by periodic startup, a delay as much as one cycle of the selected startup period occurs until the first startup. In the same way, the time stamp also delays.

When the periodic startup by the timer is set to MODE1 and the following equation is “true”, the START_CTRL block issues an interrupt to the internal sequencer.

$ICOUNT2 \& (2^{(START\_INTERVALn + 1)} - 1) == START\_PHASEn \& (2^{(START\_INTERVALn + 1)} - 1)$
(n is the sequencer number, n = 0, ..., 9)

The ICOUNT2 is a nine bit internal counter that counts up by a clock obtained by frequency dividing ($2^{PRE\_DIVIDER}$) of 32 kHz clock. This counter is reset when the SEQ_ENABLE_ALL is “0”.

The internal sequencer exits the SLEEP state by an interrupt and executes the processes of each sequencer in order within the main loop.

Figure SCU (Sensor Control Unit)-90 shows the basic startup timing.

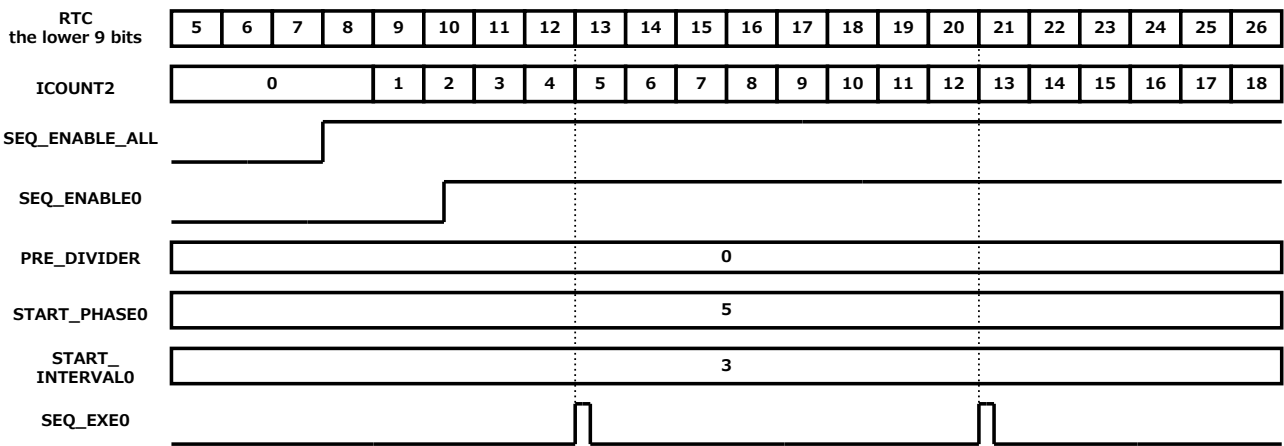


Figure SCU (Sensor Control Unit)-90 Basic Startup Timing

Figure SCU (Sensor Control Unit)-91 shows an example of when the startup delays. The delay of sampling start (T_d in the below Figure) cannot be known from the outside (CPU) because it depends on the relation between the startup timing, the $START\_PHASEn$, and the $ICOUNT2$.

For example, if startup is performed by $START\_PHASEn=0$ immediately after $ICOUNT2$ has started counting, the $ICOUNT2=0$ state has already finished and a startup delay of approximately one cycle occurs.

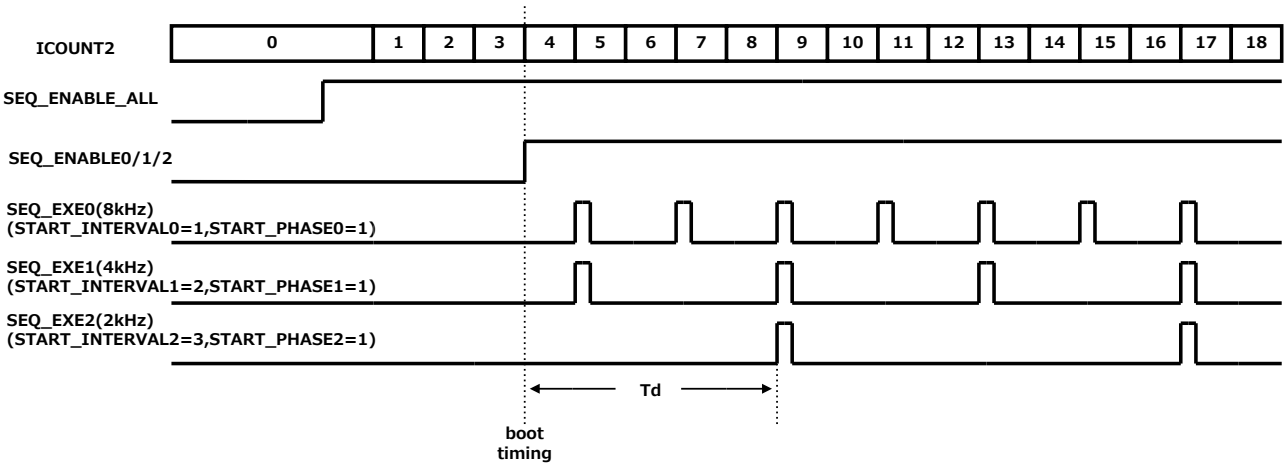


Figure SCU (Sensor Control Unit)-91 Delay at Start (Example)

3.9.15.9 OLDEST Time Stamp Restriction

The OLDEST time stamp calculated by the hardware has the following restrictions. These restrictions can be avoided by using the LATEST time stamp.

- When FORCE_THROUGH within the SCU_REG is set to “1” at the Decimation partition, the decimation ratio must be calculated using “1” but when the decimation ratio of the CIC filter is nine or smaller, that value is used.
- When the XOSC is used at the HPADC, and the sampling frequency is not a power of 2, the time stamp cannot be accurately calculated. This is because the corresponding arithmetic circuit within the hardware is comprised of a bit shift circuit.
- If the One-shot Operation is performed by the sequencer with the same ID as ID assigned for the ADC readout, the time stamp of the ADC will be incorrect. This is because 0xA must be set in the START_INTERVALn field of the START_INTERVAL register within the SCU_REG when using the One-shot Sequencer.

3.9.15.10 Converting the LATEST Time Stamp to the OLDEST Time Stamp

The LATEST_TIMESTAMP can be converted to the OLDEST_TIMESTAMP.

Due to the restrictions of the OLDEST_TIMESTAMP (refer to Section 3.9.15.9), there are cases where you will need to convert the LATEST_TIMESTAMP to the OLDEST_TIMESTAMP.

This can be done by the following equation.

$$\text{OLDEST\_TIMESTAMP} = \text{LATEST\_TIMESTAMP} - \text{INTERVAL} \times \text{remaining FIFOs}$$

(For the LATEST_TIMESTAMP and the remaining number of data, the ones read out after data transfer are used. In the case that readout is performed before the transfer, errors will occur due to writing data during the subsequent data readouts.)

The calculation for INTERVAL will be described later.

The following is an example of pseudo code for LATEST to OLDEST conversion.

```

/* get oldest timestamp from latest timestamp */
void GetOldestFromLatest (UH interval, UH uhAvail, UW *uwMsb, UH *uhLsb) {
    UW tmpDiff;
    UW tmpLsb;

    if (uhAvail == 0) return;
    tmpDiff = interval * uhAvail;
    tmpLsb = (UW)(*uhLsb);
    if (tmpLsb < tmpDiff) {
        tmpLsb += 0x80000000;
        tmpLsb -= tmpDiff;
        (*uhLsb) = (UH)(tmpLsb & 0x00007fff);
        (*uwMsb) = (*uwMsb) + (tmpLsb >> 15) - ((UW)(0x80000000) >> 15);
    } else {
        (*uhLsb) = (*uhLsb) - (UH)tmpDiff;
    }
}

```

3.9.15.11 INTERVAL Calculation Method

The INTERVAL is the value of “How many times data is input to the FIFO per the number of counts of the 32768 Hz counter”.

For example, the INTERVAL is $32768/64 = 512$ when data sampled at 64 Hz is input as-is. The dimension is “time” and the unit is 1/32768 (seconds).

The INTERVAL is used within the hardware for calculating the OLDEST_TIMESTAMP.

The following describes how to calculate the INTERVAL, which is necessary to obtain the OLDEST_TIMESTAMP data by calculating.

LPADC

Obtains the values from the following related registers.

- 32 kHz frequency division setting of TOPREG: CKDIV_SCU.SCU_U32KL(@0x4E4+TOPREG region)
- Channel select mode of SCU_ADCIF: LPADC_A1.LV_CH_SEL_MODE(@0x0204+PWD_SCU region)
Set the SEL_DIV as follows according to the CH_SEL_MODE value (the intermediate parameter used here)

In the case of 4 (two channel mode)	SEL_DIV = 1
In the case of 5 (four channel mode)	SEL_DIV = 2
Other	SEL_DIV = 0
- 32 kHz frequency division setting register of SCU_ADCIF
 - LPADC_D1.SAMP_RATIO(@0x0214 + PWD_SCU region)(for LPADC0)
 - LPADC_D4.SAMP_RATIO(@0x021C + PWD_SCU region)(for LPADC1)
 - LPADC_D5.SAMP_RATIO(@0x0220 + PWD_SCU region)(for LPADC2)
 - LPADC_D6.SAMP_RATIO(@0x0224 + PWD_SCU region)(for LPADC3)
- Pick up the decimation ratio of CIC filter within MATH_PROC which is used
 - DECIMATION_PARAM0. N1 or N2 or N3(0x5084 PWD_SCU region)
or
 - DECIMATION_PARAM0. N4 or N5 or N6(0x5088 PWD_SCU region)
- Set this to “0” when not using decimation.

Calculation Equation

Sampling frequency

$$\text{FREQ\_LPADC} = 32768 / (2^{\text{SCU\_U32KL}}) / (2^{\text{SAMP\_RATIO}}) / (2^{\text{SEL\_DIV}}) / (2^{\text{(one of N1 to N6)}})$$

$$\text{INTERVAL} = 32768 / \text{FREQ\_LPADC}$$

Calculation Equation

Sampling frequency:

$$\text{FREQ\_LPADC} = 32768 / (2^{\text{SCU\_U32KL}}) / (2^{\text{SAMP\_RATIO}}) / (2^{\text{SEL\_DIV}}) / (2^{\text{(one of N1 to N6)}})$$

$$\text{INTERVAL} = 32768 / \text{FREQ\_LPADC}$$

HPADC

Obtains the values from the following related registers.

- 32 kHz frequency division setting of TOPREG: CKDIV_SCU.SCU_U32KH(@0x4E4 + TOPREG region)
- XOSC frequency division register of SCU_ADCIF, common to the two HPADCs
 - HPADC_AC0.LV_CLK_XOSC_DIV(@0x0240 + PWD_SCU region)
 - When LV_CLK_XOSC_DIV == 0, XOSC_DIV = 2
 - When LV_CLK_XOSC_DIV == 1, XOSC_DIV = 3
 - When LV_CLK_XOSC_DIV == 2, XOSC_DIV = 4
 - When LV_CLK_XOSC_DIV == 3, XOSC_DIV = 6
- Sets whether to use XOSC/RCOSC of SCU_ADCIF or 32 kHz input, for each HPADC
 - HPADC0_A0.LV_CLK_U32_SEL0(@0x0280 + PWD_SCU region)
 - HPADC1_A0.LV_CLK_U32_SEL1(@0x02C0 + PWD_SCU region)
- Decimation ratio of CIC filter, for each HPADC
 - HPADC0_D1.DECL_RATIO(@0x0294 + PWD_SCU region)
 - HPADC1_D1.DECL_RATIO(@0x02D4 + PWD_SCU region)
- Pick up the decimation ratio of CIC filter within MATH_PROC which is used
 - DECIMATION_PARAM0. N1 or N2 or N3(0x5084 PWD_SCU region)
 - or
 - DECIMATION_PARAM0. N4 or N5 or N6(0x5088 PWD_SCU region)
 - Set this to “0” when not using decimation

Calculation Equation

When LV_CLK_U32_SEL0/1 == 1

Sampling frequency:

$$\text{FREQ\_HPADC} = 32768 / (2^{\text{SCU\_U32KH}}) / (2^{\text{DECL\_RATIO}}) / (2^{\text{(one of N1 to N6)}})$$

When LV_CLK_U32_SEL0/1 == 0

When LV_CLK_OSC_SEL0 == 0 (XOSC is selected)

Sampling frequency:

$$\text{FREQ\_HPADC} = \text{XOSC frequency} / \text{XOSC\_DIV} / (2^{\text{DECL\_RATIO}}) / 4 / (2^{\text{(one of N1 to N6)}})$$

When LV_CLK_OSC_SEL0 == 1 (RCOSC is selected)

Sampling frequency: $\text{FREQ\_HPADC} = \text{RCOSC frequency} / (2^{\text{DECI\_RATIO}}) / 4 / (2^{\text{(one of N1 to N6)}}$

$\text{INTERVAL} = 32768 / \text{FREQ\_LPADC}$

Sequencer

Obtains the values from the following related registers.

- Frequency division of 32768 Hz that is common to all sequencers
 - START_CTRL_COMMON.PRE_DIVIDER(@0x5028 PWD_SCU region)
- START_INTERVAL of each sequencer
 - START_INTERVAL3_0.START_INTERVAL0, or 1, or 2, or 3(@0x5034 PWD_SCU region)
 - START_INTERVAL7_4.START_INTERVAL4, or 5, or 6, or 7(@0x5038 PWD_SCU region)
 - START_INTERVAL9_8.START_INTERVAL8, or 9(@0x503c PWD_SCU region)
- Decimation ratio of CIC filter within MATH_PROC
 - DECIMATION_PARAM0.N1, or N2, or N3(0x5084 PWD_SCU region)
 - DECIMATION_PARAM0.N4, or N5, or N6(0x5088 PWD_SCU region)
 - Set this to "0" when not using decimation

Calculation Equation

Sampling frequency:

$\text{FREQ\_SEQ} = 32768 / (\text{PRE\_DIVIDER} + 1) / (2^{\text{START\_INTERVAL0, or 1, or 2, or 3, or 4, or 5, or 6, or 7, or 8, or 9}}) / (2^{\text{(one of N1 to N6)}}$

$\text{INTERVAL} = 32768 / \text{FREQ\_LPADC}$

3.9.15.12 Time Stamp Fluctuation

The fluctuation of time stamps depends on the execution time of each task. When tasks that were not executed in the main loop are executed, or when tasks that were executed are not executed, the time stamps fluctuate. Table SCU (Sensor Control Unit)-734 shows the approximate execution times of tasks.

Table SCU (Sensor Control Unit)-726 Approximate Execution Times of Tasks

Task	Number of Processing Clocks	Time Stamp Fluctuation Number of 32 kHz counts (1/32768 seconds)
When Main Loop Idles	720	3
HPADC 8 Sample Processing	1550	7
SPI 6 Byte (3-axis sensor) Processing	370	2
I2C 6 Byte (3-axis sensor) Processing	1100	5
LPADC 1 Sample Processing	1260	6

(The number of 32 kHz counts is the value when the main clock of the SCU is 8.192 MHz)

The following table shows the estimated values of time stamp fluctuation (maximum) when a task's execution start time is affected by the presence of a different task. (in this table, the SCU clock is RCOSC 8.192 MHz)

Table SCU (Sensor Control Unit)-727 Time Stamp Fluctuation Estimated Values

Task	Number of Fluctuation Clocks	Time Stamp Fluctuation (maximum) (1/32768 seconds)
HPADC	2737	11
LPADC	3907	16
SPI	3794	16
I2C	4259	18

Figure SCU (Sensor Control Unit)-92 shows a case when fluctuation is caused by the effects of HPADC. In this example, the fluctuation is approximately 7 (32 kHz count) in Table SCU (Sensor Control Unit)-734. Note that in the below Figure, the fluctuation of the sequencer start time is not considered.

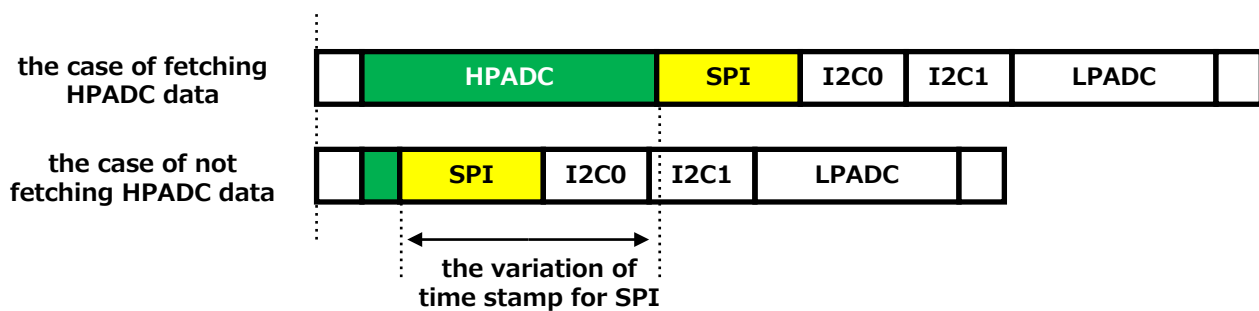


Figure SCU (Sensor Control Unit)-92 Time Stamp Fluctuation by the Presence/Absence of HPADC Execution

3.9.15.13 Time Stamp Readout Restrictions

The time stamp within the SCU is comprised of MSB 32 bits (the seconds digits) and LSB 15 bits (the seconds and smaller than seconds digits). However, atomic access is not supported during readout from the APB. Therefore, when readout is performed by APB access two times, the time stamp readout value may shift by a maximum of ± 1 seconds.

Within the hardware, “LSB and MSB, and remaining number of FIFO data update are atomic” is compensated for. Therefore, the only problem is when update occurs during two bus accesses, which can be avoided by performing two continuous readouts (four APB accesses).

The following is an example pseudo code of reading out the OLDEST_TIMESTAMP two times. Using the change of the MSB, the carry of the MSB during the two bus accesses is detected.

```

readOldestTimeStamp(){
  PreLsb = readLsb();
  PreMsb = readMsb();
  PostLsb = readLsb();
  PostMsb = readMsb();
  if(PreMsb == PostMsb){
    msb = PostMsb;
    lsb = PostLsb;
  }else{
    msb = PreMsb;
    lsb = PreLsb;
  }
}

```

Also, the following is an example pseudo code of reading out the LATEST_TIMESTAMP. Using the remaining number of FIFOs (PreAvail/PostAvail), the carry of the MSB during the two readouts is detected. (In the readout of the LATEST_TIMESTAMP, the remaining number of FIFOs must be read out for the LATEST_TIMESTAMP to the OLDEST_TIMESTAMP conversion, and because of this, detection is performed by the readout of the remaining number of FIFOs.)

```

readLatestTimeStamp(){
  PreAvail = readAvail();
  PreLsb = readLsb();
  PreMsb = readMsb();
  PostAvail = readAvail();
  PostLsb = readLsb();
  PostMsb = readMsb();
  if(PreAvail == PostAvail){
    msb = PreMsb;
    lsb = PreLsb;
  }else{
    msb = PostMsb;
    lsb = PostLsb;
    timestamp = msb<<15+lsb-INTERVAL;
  }
}

```

3.9.15.14 LPADC Sample Decimation Parameter Dynamic Change

When converting the sampling rate using the LPADC sample decimation function within the ADCIF, a maximum delay equal to the [original sampling period of the LPADC analog region] x 32768 will occur when the sampling rate is dynamically changed (with the sampling input of the FIFO inside the ADCIF kept ON) to a higher rate than the one currently in use.

The sample decimation circuit of the LPADC is controlled by the counter (the output value is cnt_out) which increments each time data is output from the LPADC.

- The counter operates at a clock of 32 kHz, and countup is performed at the timing that data is output from the LPADC (the LPADC_DATAEN in Figure SCU (Sensor Control Unit)-93).
- When $\text{cnt\_out} == 2^{\text{SAMP\_RATIO}} - 1$, the value of the cnt_out is reset to "0" (comparison is always performed in 16 bit).
- Data is input to the FIFO when cnt_out is reset.
- E.g.: When $\text{SAMP\_RATIO} = 2$, reset is performed at $\text{cnt\_out} == 3$, which results in 0-1-2-3-0-1-2-3-, ..., and sampling is performed to the FIFO at a rate of 1/4 (Figure SCU (Sensor Control Unit)-93).

- The maximum value of cnt_out is $32767(2^{15}-1)$.
- Since the SAMP_RATIO is directly connected from the register to the comparator for comparing the counter value, when the software is changed, it is immediately reflected.
- Counter reset is common to all four channels (reset cannot be done on a counter basis).

Dynamic update of the SAMP_RATIO is not considered (the specification is such that parameters are updated when the internal counter is reset).

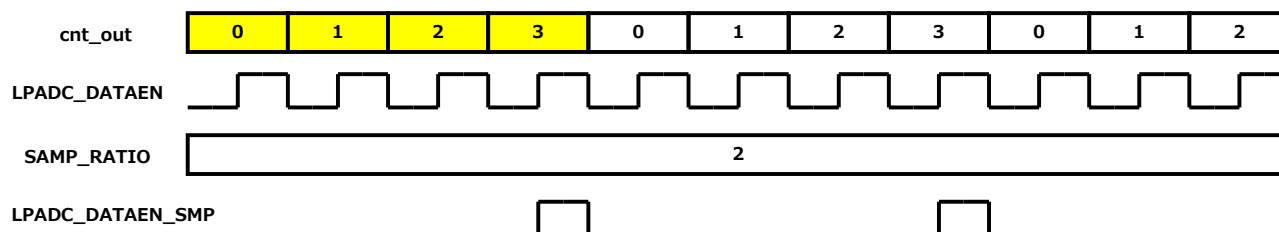


Figure SCU (Sensor Control Unit)-93 Counter Basic Operation

When a reset of the internal counter is not performed, and the sampling frequency is changed from low to high, a large delay may occur.

The delay until the first datum can be extracted is as follows:

- When the first time each channel of LPADC is started up
 $1/RPOST$ (RPOST = RPRE) [seconds]
 E.g.: When 256 Hz, approximately 3.9 ms
- After the LPADC stops, startup with sampling frequency changed, not resetting the LPADC
 - In the case of sampling frequency change (High => Low) (SAMP_RATIO Low => High)
 Maximum
 $1/RPOST$ [seconds]
 Minimum
 $1/RPOST - 1/RPRE + 1/RADC$ [seconds]
 - In the case of sampling frequency change (Low => High) (SAMP_RATIO High => Low)
 Minimum
 $1/RADC$ [seconds]
 Maximum
 $32768/RADC$ [seconds]
 E.g.: when 256 Hz, 128s

Here,

RADC: Sampling rate of LPADC (Hz)

RPRE: Sampling rate after decimation before change (Hz)

RPOST: Sampling rate after decimation after change (Hz)

Also, the possibility of a large delay longer than the sampling period is:

Condition:

Sampling frequency change (Low => High) (SAMP_RATIO High => Low)

The current count value Count value at register change $> (2^{\text{RPOST}} - 1)$

Possibility of occurrence:

$1 - 1/(RPRE/RPOST)$

3.9.15.15 HPADC CIC Filter Parameter Dynamic Change

When performing sampling rate conversion using the CIC filter within the ADCIF, a maximum delay equal to the [original sampling period of the HPADC analog region] x 256 will occur when the sampling rate is dynamically changed to a higher rate than the one currently in use.

This is because the CIC filter uses the same counter circuit as the sample decimation circuit of the LPADC (Section 3.9.15.14).

3.9.15.16 Decimation Partition Write FIFO and Read FIFO Connection Combinations

In principle, the Write FIFOs and Read FIFOs of the decimation partition must be connected in a one-to-one relation as shown in the example in Figure SCU (Sensor Control Unit)-94.

One-to-N connections as shown in Figure SCU (Sensor Control Unit)-95 are functionally capable of realizing equivalent processing by one-to-one connections but they are normally not used.

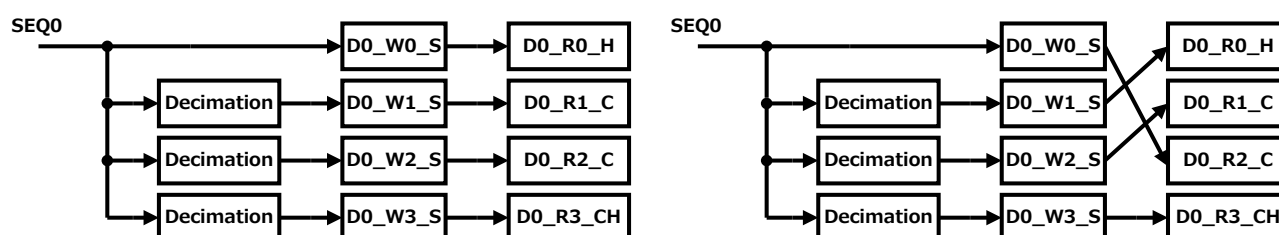


Figure SCU (Sensor Control Unit)-94 1 One-to-One Connection (Example)

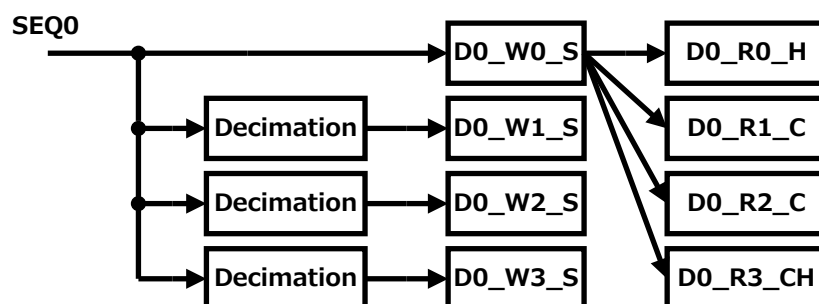


Figure SCU (Sensor Control Unit)-95 One-to-N Connection (Example)

3.9.15.17 One-shot Sequencer Parameter Restrictions

When using the One-shot Sequencer, 0xA must be set in the corresponding START_INTERVALn (n is the sequencer number) fields of the START_INTERVAL3_0, START_INTERVAL7_4, and START_INTERVAL9_8 registers within the SCU_REG.

When this setting has been made, the OLDEST_TIMESTAMP cannot be used because its value cannot be correctly calculated by the sequencer using the same Write FIFO number as the ADC.
(refer to Section 3.9.15.9)

With the One-shot Sequencer, captured data cannot be passed through the MATH_PROC.

3.9.15.18 FIFO Points of Attention

3.9.15.18.1 FIFO Initialization

Initialization of the Write FIFO and Read FIFO have the following restrictions in terms of their order.

- Make sure to perform reset (*_R*_*_CTRL1.FIFO_RESET) of the readout side FIFO after initializing the writing side FIFO.

Before performing reset of the readout side, the initial setting of the Write FIFO must be completed because the hardware uses the reset of the readout side FIFO as the trigger to copy the pointer of the writing side FIFO to the readout side. Initialization of the writing side FIFO means the below sequences.

Table SCU (Sensor Control Unit)-728 Write FIFO Initialization (excluding virtual partition)

Order	Initialization Process	Register(FIFO_REG)
1	Partition start address selection	*_W*_*_CTRL0.START_OFFSET
2	Partition size selection	*_W*_*_CTRL0.PARTITION_SIZE
3	Selection of number of bytes per sample	*_W*_*_CTRL1.FIFO_SAMPLE_SIZE
4	Selection of operation mode during FIFO full	*_W*_*_CTRL1.OVERWRITE_IF_FULL
5	FIFO writing side reset	*_W*_*_CTRL1.FIFO_RESET

Make the Read FIFO initial settings in the following order.

Table SCU (Sensor Control Unit)-729 Read FIFO Initialization

Order	Initialization Process	Register
1	Watermark setting	*_R*_*_CTRL0.WATER_MARK
2	Writing side FIFO reset	*_R*_*_CTRL1.FIFO_RESET

(Simultaneously)	DMA handshake signal output permission setting	*_R*_*_CTRL1.FIFO_DMA_ENABLE
	Readout side FIFO operation permission	*_R*_*_CTRL1.FIFO_ENABLE

For FIFO restrictions, also refer to Section 3.9.8.10.

3.9.15.19 Register and SCU_RAM Reading and Writing

When the internal sequencer is in SLEEP, you cannot read or write from/to the control registers or SCU_RAM. Recover the internal sequencer from SLEEP before reading or writing from/to the control registers or SCU_RAM.

3.10 SPI

3.10.1 Features and Overview

The SPI of this LSI equips the [PrimeCell® Synchronous Serial Port \(PL022\)](#) from ARM Limited.

The SPI0 and SPI3 offer additional functions to the Chip Select control. For details, refer to the [PrimeCell® Synchronous Serial Port \(PL022\)](#) Technical Reference Manual.

SPI List

- SPI0 (Power domain: PWD_SYSIOP_SUB)
Supports only the master mode.
There is only one line of Chip Select.
This is used for data transmit/receive (Tx&Rx mode).
- SPI3 (Power domain: PWD_SCU)
Supports only the master mode. Since it has three lines of Chip Select, it can connect a maximum of three sensors to the SPI bus. SPI is usually controlled from the SCU sequencer. When the SCU sequencer is not used, communication can be performed via the SPI bus by directly controlling the registers of the SPI from the SYSCPU. Since control from the sequencer and control from the SYSCPU are exclusive, they cannot be performed simultaneously.
This is used for data transmit/receive (Tx&Rx mode).
- SPI4 (Power domain: PWD_APP_SUB)
Supports only the master mode.
There is only one line of Chip Select.
This is used for data transmit/receive (Tx&Rx mode) or data transmit (Tx mode) only.
- SPI5 (Power domain: PWD_APP_SUB)
Supports only the master mode.
There is only one line of Chip Select.
This is used for data transmit/receive (Tx&Rx mode)

Additional functions

The SPI0 and SPI3 offer the following additional functions to the [PrimeCell® Synchronous Serial Port \(PL022\)](#).

- Additional functions
 - Chip Select function (SPI3)
By the addition of two lines of Chip Select signals, one Chip Select signal can be selected from the total of three Chip Select signals. The selection of the Chip Select signal is done through exclusive control.

- Switching between the function for fixed-value output and function for control of the PL022
A function has been added to set the Chip Select signal (High/Low) by register control. You can switch between Chip Select control by the register and Chip Select control by the PL022.
In Chip Select control by the register, the Chip Select does not change every 8 bits or 16 bits during the communication, and fixed values can be output during the communication.

Transfer Rate

The maximum transfer rate of the SPI is determined by the combination of the clock selected as the clock source (SYSPLL, XOSC, RCOSC, or RTC), the X'tal Oscillator clock, and the voltage mode (High Performance mode/ Low Power mode). The following tables show each combination and the maximum transfer rates.

Table SPI-730 XOSC (26 MHz), High Performance Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	48.750	39.000	26.000	8.192	0.032768
SPI0 SCK(Tx&Rx mode)	Mbps	12.188	9.750	6.500	4.096	0.016384
SCU (ck_scu_pre)	MHz	-	-	13.000	8.192	0.032768
SPI3 SCK(Tx&Rx mode)	Mbps	-	-	6.500	4.096	0.016384
APP (CK_APP)	MHz	97.500	156.000	26.000	8.192	0.032768
SPI4 SCK(Tx&Rx mode)	Mbps	9.750	9.750	13.000	4.096	0.016384
SPI4 SCK(Tx mode)	Mbps	48.750	39.000	13.000	4.096	0.016384
SPI5 SCK(Tx&Rx mode)	Mbps	12.188	13.000	13.000	4.096	0.016384

Table SPI-731 XOSC (26 MHz), Low Power Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	32.500	31.200	26.000	8.192	0.032768
SPI0 SCK(Tx&Rx mode)	Mbps	8.125	7.800	6.500	4.096	0.016384
SCU (ck_scu_pre)	MHz	-	-	13.000	8.192	0.032768
SPI3 SCK(Tx&Rx mode)	Mbps	-	-	6.500	4.096	0.016384
APP (CK_APP)	MHz	39.000	39.000	26.000	8.192	0.032768
SPI4 SCK(Tx&Rx mode)	Mbps	6.500	6.500	6.500	4.096	0.016384
SPI4 SCK(Tx mode)	Mbps	9.750	9.750	13.000	4.096	0.016384
SPI5 SCK(Tx&Rx mode)	Mbps	6.500	6.500	6.500	4.096	0.016384

3.10.2 SPI0

3.10.2.1 Register List

Table SPI-748 shows a register list of the SPI0.

Table SPI-732 SPI0 Register List

Address	Register Name	Type	Description	Initial Value
0x041AB000 0x041AB024	PrimeCell® Synchronous Serial Port (PL022) register			-
0x041AB028 0x041AB08C	Reserved	RO	Reserved	0x0
0x041AB090	CS_MODE	RW	Chip Select	0x0
0x041AB094	SSP_CS	RW	Chip Select setting	0x1
0x041AB098	Reserved	RW	Reserved	0x0
0x041AB09C 0x041ABFDC	Reserved	RO	Reserved	0x0
0x041ABFE0 0x041ABFFC	PrimeCell® Synchronous Serial Port (PL022) register			-

3.10.2.2 Register Descriptions

Table SPI-749 shows descriptions of the registers added for control of Chip Select.

Table SPI-733 SPI0 register Descriptions

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041AB090	CS_MODE	Reserved	RO	[15:1]	0	Reserved
		cs_mode	RW	[0]	1'b0	Chip Select (CS) 0: Uses CS of PL022 1: Uses CS of SSP_CS (register setting)
0x041AB094	SSP_CS	Reserved	RO	[15:1]	0	Reserved
		ssp_cs	RW	[0]	1'b1	Chip Select setting 0: SPI communication active 1: SPI communication inactive

3.10.2.3 Clock and Reset

Figure SPI-96 shows the clock and reset system diagram of the SPI0.

To access the SPI0 register, supply the clock to the AHB/APB Bus Bridge.

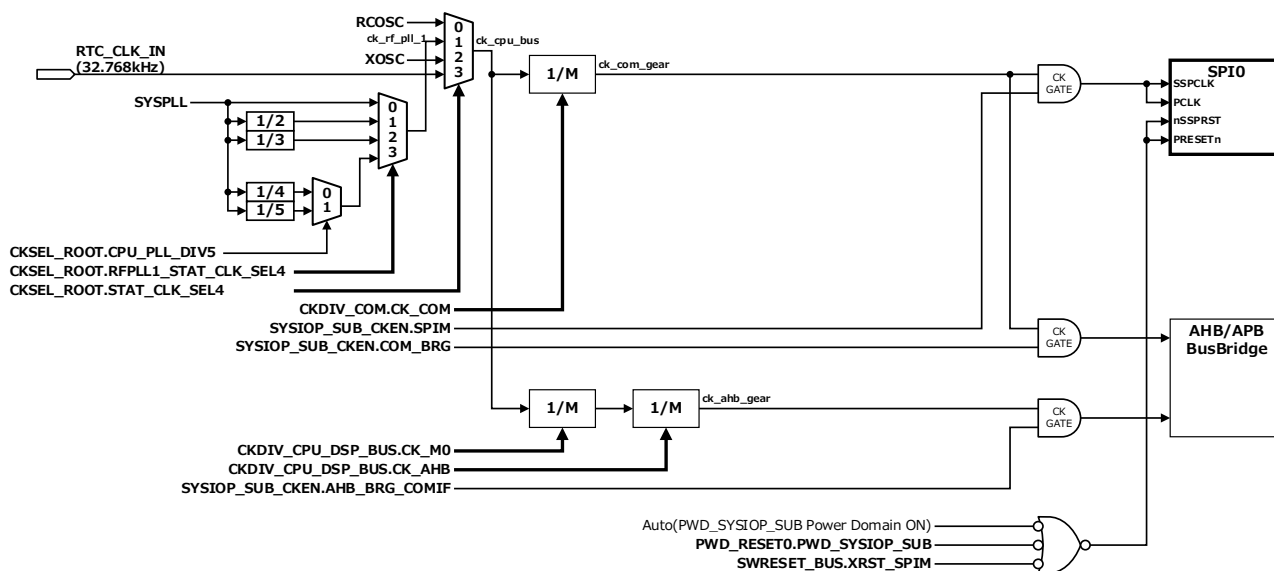


Figure SPI-96 SPI0 Clock and Reset System

3.10.2.4 Clock Supply Start and Stop

3.10.2.4.1 Clock Supply Start

Perform the following control to start supplying the SSPCLK clock and PCLK clock to the SPI0.

1. Clock supply start to the AHB/APB Bus Bridge
SYSIOP_SUB_CKEN.COM_BRG = 1'b1
SYSIOP_SUB_CKEN.AHB_BRG_COMIF = 1'b1
2. Reset release
SWRESET_BUS.XRST_SPIM=1'b1
3. Clock supply start
SYSIOP_SUB_CKEN.SPIM=1'b1

3.10.2.4.2 Clock Supply Stop

Perform the following control to stop supplying the SSPCLK clock and PCLK clock to the SPI0.

1. Clock supply stop
SYSIOP_SUB_CKEN.SPIM=1'b0

3.10.3 SPI3

3.10.3.1 Register List

Table SPI-750 shows a register list of the SPI3.

Table SPI-734 SPI3 Register List

Address	Register Name	Type	Description	Initial Value
0x0418D000 0x0418D024	PrimeCell® Synchronous Serial Port (PL022) register			-
0x0418D028 0x0418D08C	Reserved	RO	Reserved	0x0
0x0418D090	CS_MODE	RW	Chip Select	0x0
0x0418D094	SSP_CS	RW	Chip Select setting	0x1
0x0418D098	SLAVE_TYPE	RW	SPI communication slave selection	0x0
0x0418D09C 0x0418D3FC	Reserved	RO	Reserved	0x0

3.10.3.2 Register Descriptions

Table SPI-751 shows descriptions of the registers added for control of Chip Select.

Table SPI-735 SPI3 Register Descriptions

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0418D090	CS_MODE	Reserved	RO	[15:1]	0	Reserved
		cs_mode	RW	[0]	1'b0	Chip Select (CS) 0: Uses CS of PL022 1: Uses CS of SSP_CS (register setting)
0x0418D094	SSP_CS	Reserved	RO	[15:1]	0	Reserved
		ssp_cs	RW	[0]	1'b1	Chip Select setting 0: SPI communication active 1: SPI communication inactive
0x0418D098	SLAVE_TYPE	Reserved	RO	[15:2]	0	Reserved

		slave_type	RW	[1:0]	2'b00	SPI communication slave selection function
						0,3: SPI3_CS0_X
						1: SPI3_CS1_X
						2: SPI3_CS2_X

3.10.3.3 Clock and Reset

Figure SPI-97 shows the clock and reset system diagram of the SPI3.

When accessing the SPI3 register, set SCU_CKEN.SCU=1'b1 beforehand.

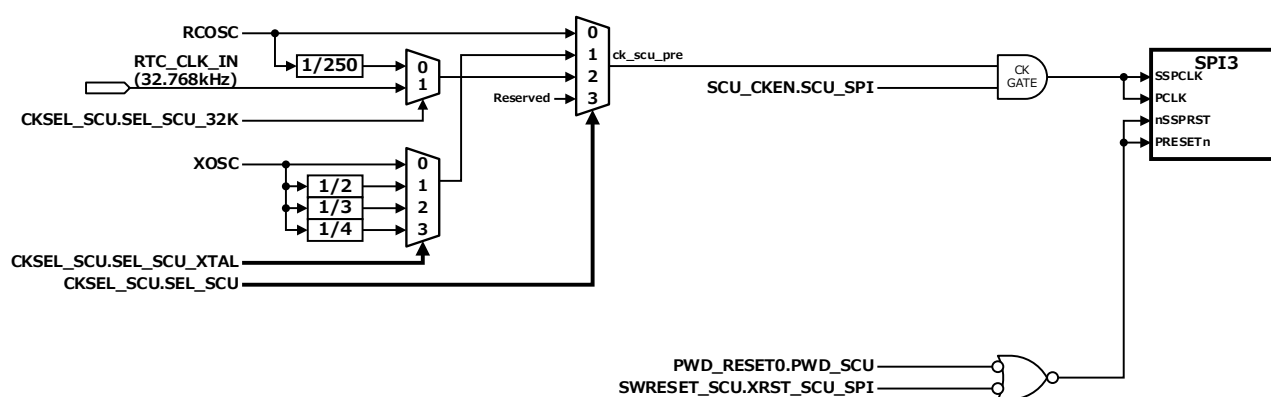


Figure SPI-97 SPI3 Clock and Reset System

3.10.3.4 Clock Supply Start and Stop

3.10.3.4.1 Clock Supply Start

Perform the following control to start supplying the SSCLK clock and PCLK clock to the SPI3.

- Reset release
SWRESET_SCU.XRST_SCU_SPI=1'b1
- Clock supply start
SCU_CKEN.SCU_SPI=1'b1

3.10.3.4.2 Clock Supply Stop

Perform the following control to stop supplying the SSCLK clock and PCLK clock to the SPI3.

- Clock supply stop
SCU_CKEN.SCU_SPI=1'b0

3.10.4 SPI4

3.10.4.1 Register List

Table SPI-752 shows a register list of the SPI4.

In the case of SPI4, the ID code of the [PrimeCell® Synchronous Serial Port \(PL022\)](#) cannot be read out.

Table SPI-736 SPI4 Register List

Address	Register Name	Type	Description	Initial Value
0x0E103400 0x0E103424	PrimeCell® Synchronous Serial Port (PL022) register			-
0x0E103428 0x0E103BFC	Reserved	RO	Reserved	0x0

3.10.4.2 Clock and Reset

Figure SPI-98 shows the clock and reset system diagram of the SPI4.

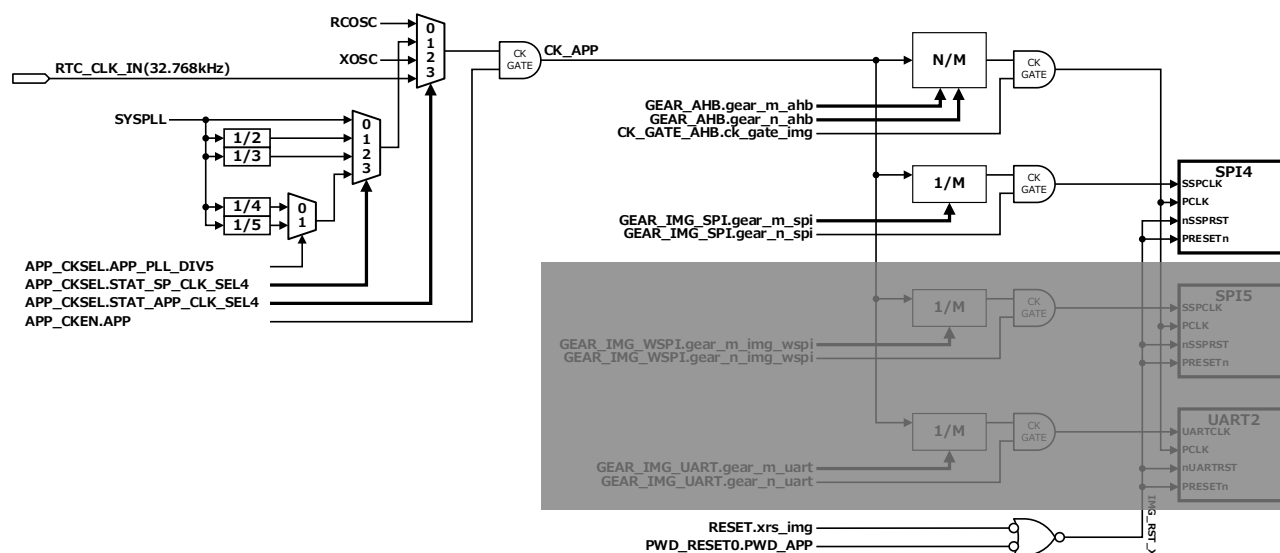


Figure SPI-98 SPI4 Clock and Reset System

3.10.4.3 Clock Supply Start and Stop

3.10.4.3.1 Clock Supply Start

Perform the following control to start supplying the SSPCLK clock and PCLK clock to the SPI4.

1. Reset release

PWD_RESET0.PWD_APP=1'b1

RESET.xrs_img=1'b1

2. Supply the CK_APP (For details, refer to the APP Section (3.13))

3. Clock supply for the SPI4 register and division ratio setting

GEAR_AHB.gear_m_ahb=(arbitrary: denominator setting of the division ratio)

GEAR_AHB.gear_n_ahb=(arbitrary: numerator setting of the division ratio)

CK_GATE_AHB.ck_gate_img=1'b1

4. SPI4 control clock supply and division ratio setting

GEAR_IMG_SPI.gear_m_spi=(arbitrary: denominator setting of the division ratio)

GEAR_IMG_SPI.gear_n_spi=1'b1

3.10.4.3.2 Clock Supply Stop

Perform the following control to stop supplying the SSPCLK clock and PCLK clock to the SPI4.

1. SPI4 control clock stop

GEAR_IMG_SPI.gear_n_spi=1'b0

2. SPI4 register's clock stop

CK_GATE_AHB.ck_gate_img=1'b0

3.10.5 SPI5

3.10.5.1 Register List

Table SPI-753 shows a register list of the SPI5.

Table SPI-737 SPI5 Register List

Address	Register Name	Type	Description	Initial Value
0x0E103C00 0x0E103C24	PrimeCell® Synchronous Serial Port (PL022) register			-
0x0E103C28 0x0E104FFC	Reserved	RO	Reserved	0x0

3.10.5.2 Clock and Reset

Figure SPI-99 shows the clock and reset system diagram of the SPI5.

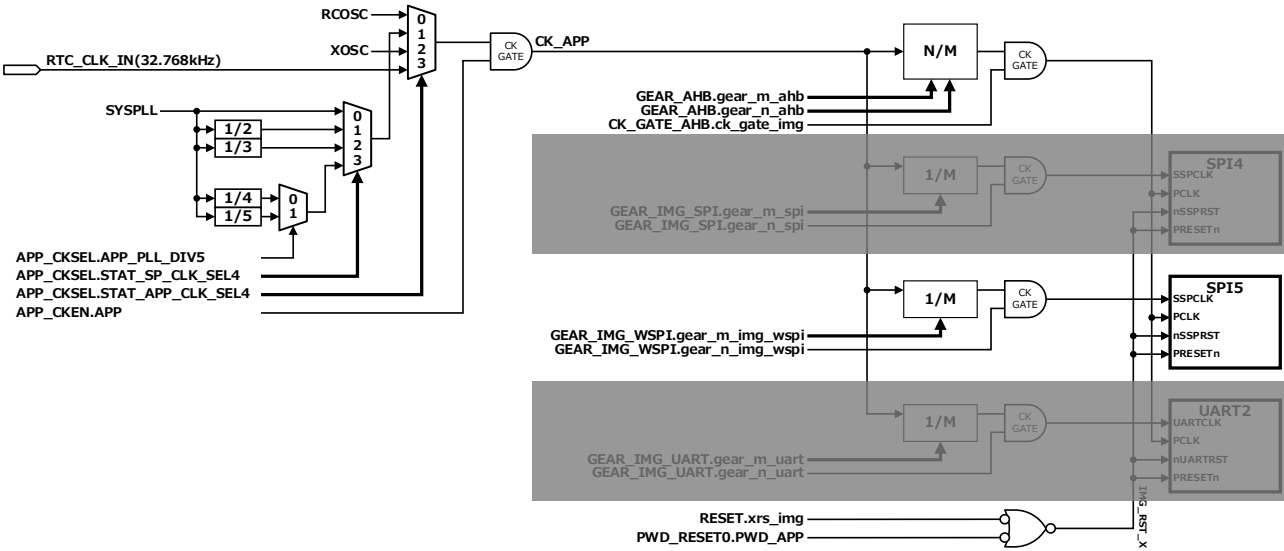


Figure SPI-99 SPI5 Clock and Reset System

3.10.5.3 Clock Supply Start and Stop

3.10.5.3.1 Clock Supply Start

Perform the following control to start supplying the SSPCLK clock and PCLK clock to the SPI5.

1. Reset release

PWD_RESET0.PWD_APP=1'b1

RESET.xrs_img=1'b1

2. Supply the CK_APP (For details, refer to the APP Section (3.13))

3. Clock supply for SPI5 register and division ratio setting

GEAR_AHB.gear_m_ahb=(arbitrary: denominator setting of the division ratio)

GEAR_AHB.gear_n_ahb=(arbitrary: numerator setting of the division ratio)

CK_GATE_AHB.ck_gate_img=1'b1

4. SPI5 control clock supply and division ratio setting

GEAR_IMG_WSPI.gear_m_wspi=(arbitrary: denominator setting of the division ratio)

GEAR_IMG_WSPI.gear_n_wspi=1'b1

3.10.5.3.2 Clock Supply Stop

Perform the following control to stop supplying the SSPCLK clock and PCLK clock to the SPI5.

1. SPI5 control clock stop

GEAR_IMG_WSPI.gear_n_wspi=1'b0

2. SPI5 register's clock stop

CK_GATE_AHB.ck_gate_img=1'b0

3.11 UART

3.11.1 Overview and Features

The UART of this LSI equips the [PrimeCell® UART \(PL011\)](#) from ARM Limited.

It has an independent transmitter and independent receiver built in and allows full-duplex transmission. There is also a dedicated baud rate generator built in, which enables transmissions of a wide range of baud rates. For details, refer to the [PrimeCell® UART \(PL011\)](#) Technical Reference Manual.

UART List

- UART1 (Power domain: PWD_SYSIOP_SUB)
- UART2 (Power domain: PWD_APP_SUB)

Transfer Rate

The maximum baud rate of the UART is determined by the combination of the clock selected as the clock source (SYSPLL, XOSC, RCOSC, or RTC), the X'tal Oscillator clock, and the voltage mode (High Performance mode/ Low Power mode). The following table shows each combination and the maximum transfer rates.

Table

Table UART-738 XOSC (26 MHz), High Performance Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	48.750	39.000	26.000	8.192	0.032768
UART1 baudrate	bps	1843200	1843200	921600	460800	1200
APP (CK_APP)	MHz	97.500	156.000	26.000	8.192	0.032768
UART2 baudrate	bps	1843200	1843200	921600	460800	1200

Table UART-739 XOSC (26 MHz), Low Power Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
SYSIOP (ck_ahb_gear,ck_com_gear)	MHz	32.500	31.200	26.000	8.192	0.032768
UART1 baudrate	bps	1843200	1843200	921600	460800	1200
APP (CK_APP)	MHz	39.000	39.000	26.000	8.192	0.032768
UART2 baudrate	bps	1843200	1843200	921600	460800	1200

3.11.2 UART1

3.11.2.1 Register List

Table UART-764 shows a register list of the UART1.

Table UART-740 UART1 Register List

Address	Register Name	Type	Description	Initial Value
0x041AC000 0x041AC048	PrimeCell® UART (PL011) register			-
0x041AC04C 0x041ACFFC	Reserved	RO	Reserved	0x0

3.11.2.2 Clock and Reset

Figure UART-100 shows the clock and reset system diagram of the UART1.

To access the UART1 register, supply the clock to the AHB/APB Bus Bridge.

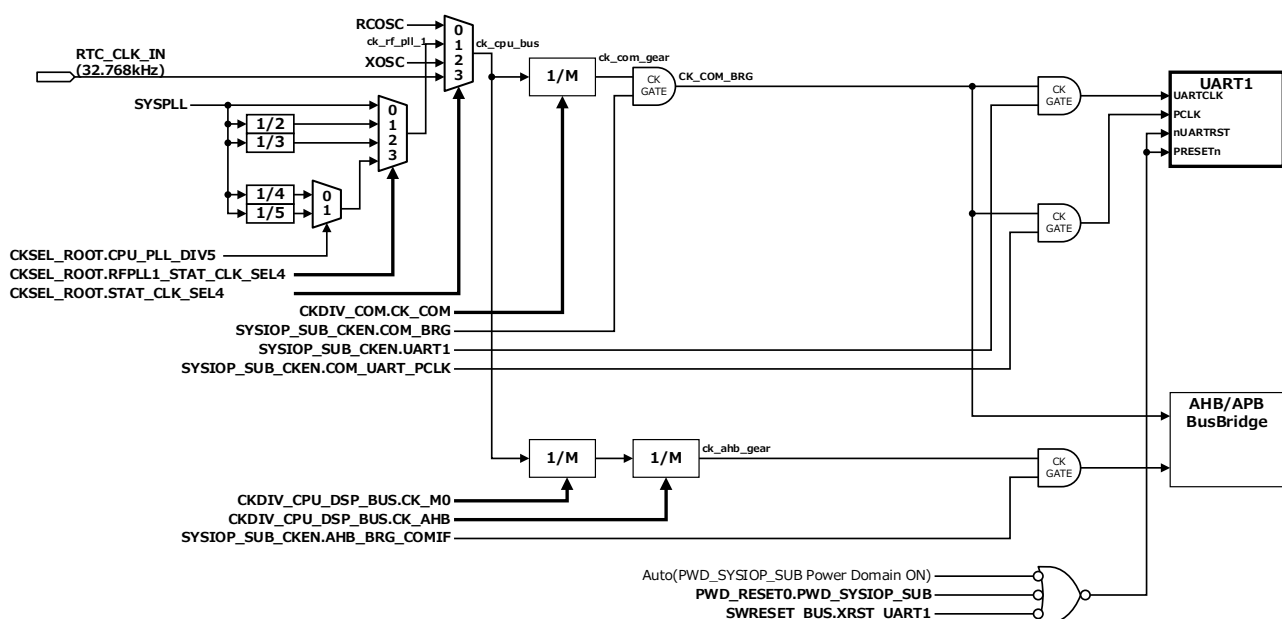


Figure UART-100 UART1 Clock and Reset System

3.11.2.3 Clock supply Start and Stop

3.11.2.3.1 Clock Supply Start

Perform the following control to start supplying the UARTCLK clock and PCLK clock to the UART1.

1. Clock supply start to the AHB/APB Bus Bridge
SYSIOP_SUB_CKEN.COM_BRG=1'b1
SYSIOP_SUB_CKEN.AHB_BRG_COMIF=1'b1
2. Reset release
SWRESET_BUS.XRST_UART1=1'b1
3. Clock supply start
SYSIOP_SUB_CKEN.COM_UART_PCLK=1'b1
SYSIOP_SUB_CKEN.UART1=1'b1

3.11.2.3.2 Clock Supply Stop

Perform the following control to stop supplying the UARTCLK clock and PCLK clock to the UART1.

1. Clock supply stop
SYSIOP_SUB_CKEN.COM_UART_PCLK=1'b0
SYSIOP_SUB_CKEN.UART1=1'b0

3.11.3 UART2

3.11.3.1 Register List

Table UART-765 shows a register list of the UART2.

Table UART-741 UART2 Register List

Address	Register Name	Type	Description	Initial Value
0x0E103000 0x0E103048	PrimeCell® UART (PL011) register			-
0x0E10304C 0x0E1033FC	Reserved	RO	Reserved	0x0

3.11.3.2 Clock and Reset

Figure UART-101 shows the clock and reset system diagram of the UART2.

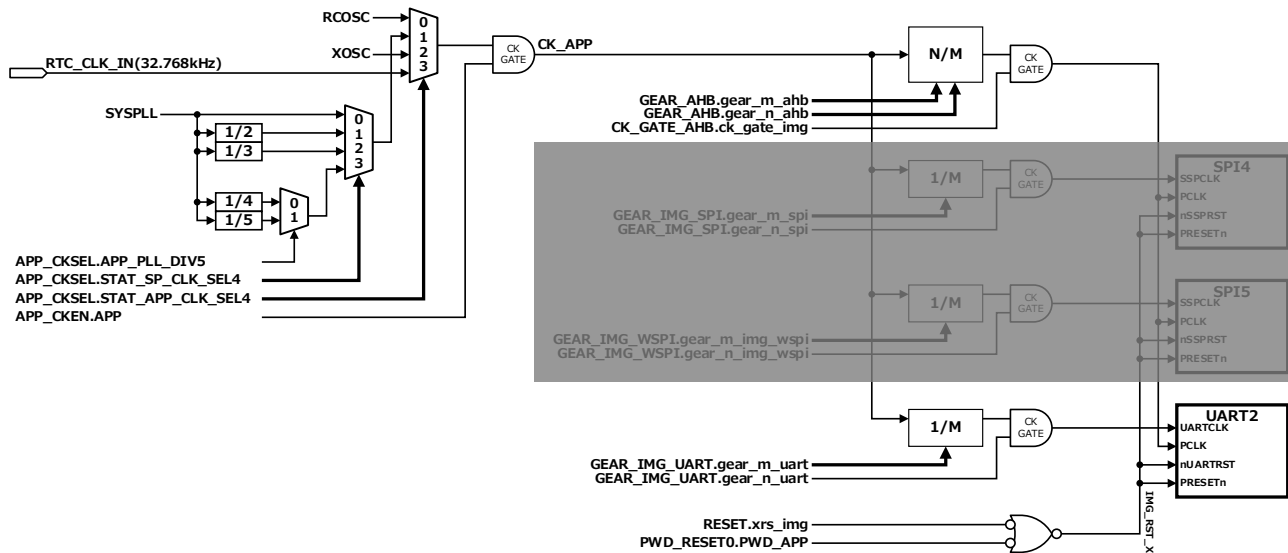


Figure UART-101 UART2 Clock and Reset System

3.11.3.3 Clock Supply Start and Stop

3.11.3.3.1 Clock Supply Start

Perform the following control to start supplying the UARTCLK clock and PCLK clock to the UART2.

1. Reset release

PWD_RESET0.PWD_APP=1'b1

RESET.xrs_img=1'b1

2. Supply the CK_APP (For details, refer to the APP Section (3.13))
3. Clock supply for the UART2 register and division ratio setting

GEAR_AHB.gear_m_ahb=(arbitrary: denominator setting of the division ratio)

GEAR_AHB.gear_n_ahb=(arbitrary: numerator setting of the division ratio)

CK_GATE_AHB.ck_gate_img=1'b1

4. UART2 control clock supply and division ratio setting

GEAR_IMG_UART.gear_m_uart=(arbitrary: denominator setting of the division ratio)

GEAR_IMG_UART.gear_n_uart=1'b1

3.11.3.3.2 Clock Supply Stop

Perform the following control to stop supplying the UARTCLK clock and PCLK clock to the UART2.

1. UART2 control clock stop
GEAR_IMG_UART.gear_n_uart=1'b0
2. UART2 register's clock stop
CK_GATE_AHB.ck_gate_img=1'b0

3.12 GNSS

Multi-GNSS receiver

The features are:

- Multiple Constellation compatibility
 - GPS (L1 C/A)
 - GLONASS (L1OF)
- Position Accuracy

Item	GPS	GPS & GLONASS	Unit	Remark
2DRMS	2.5	2.5	m	Signal strength is -130 dBm Test circuit as shown in the figure below

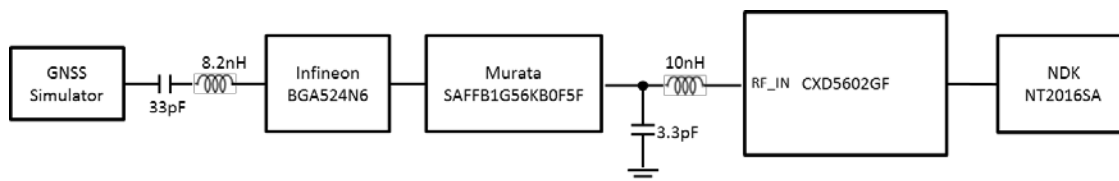
Time-To-First-Fix (TTFF)

Item	GPS	GPS & GLONASS	Unit	Remark
Cold Start	35	35	s	Signal strength is -130 dBm Test circuit as shown in the figure below
Hot Start	2	2	s	

Sensitivity

Item	GPS	GPS & GLONASS	Unit	Remark
Cold Start	-147	-147	dBm	Test circuit as shown in the figure below
Hot Start	-160	-160	dBm	
Tracking	-161	-161	dBm	

Test Circuit



● Noise Filter

An embedded noise filter for GNSS signals. It is automatically enabled at the optimum settings for the input noise.

● RF Performance

Item	Min.	Typ.	Max.	Unit
Total NF	-	3	-	db

3.13 APP

3.13.1 Function Overview

The Application Domain is responsible for a variety of application software of the CXD5602. Centered around the multi core CPU system of the Arm® Cortex®-M4 processor with FPU, it equips high speed interface processing block such as USB and eMMC, Audio, and Imaging multimedia processing.

The following describes the Application Domain's features.

Depending on the combination of X'tal Oscillator clock frequencies and voltage modes (High Performance mode/Low Power mode), the performance such as transfer rate varies. This section explains the performances when 26 MHz is selected as the X'tal Oscillator clock frequency. Overview of APP Maximum Frequency and sections of each function, for example, for SPI, refer to the Section of SPI (3.10).

Application Processor

The application processor integrates six Cortex®-M4 processors with FPU (ADSP) to meet the requirements of wearable and IoT devices, which demand operation in low power and performance-optimized consumer applications with the ability to scale in speed up to 156.0 MHz, the Arm® Cortex®-M4 Processor.

The key features include:

- Arm® Cortex®-M4 processor with FPU
 - ISA Support: Thumb®/Thumb®-2 technology
 - DSP Extension: Single cycle 16/32 bit MAC, Single cycle dual 16 bit MAC, 8/16 bit SIMD arithmetic, Hardware Divide (2-12 Cycles)
 - Floating Point Unit: Single precision floating point unit, IEEE 754 compliant
- Processor system peripherals
 - Programmable Interrupts Controller
 - 128 channel peripheral Interrupt support for each processor
 - Timer
 - AMBA® Design Kit (ADK) SP804
 - Two-channel support
 - One Timer module for each processor (Total: Six Timers)
 - Watchdog Timer
 - AMBA® Design Kit (ADK) SP805
 - One channel for each processor (Total: Six Watchdog Timers)

Crypto Engine in Application Domain

The key features include:

- AES Encryption/Decryption
 - ECB, CBC, CTR, OFB, and CFB and CMAC chaining algorithms, 128, 192 or 256 bit key
- Key generation
 - Up to 128 bit

Embedded Application Memory

The key features include:

- 1.5 MByte SRAM
- operating frequency
 - High Performance mode: Up to 156.0 MHz
 - Low Power mode: Up to 39.0 MHz

Image and Display Processing Domain

The key features Domain include:

- 8 bit parallel Camera Interface input
 - 8 bit ITU-R BT.601/656 Mode
 - compressed data like JPEG supported
 - supports Y/C, JPEG and JPEG+Y/C Interleave formats
 - Programmable polarity of video sync signal
 - Capture frame control supported
 - Input image size
 - JPEG Only : up to 5 M pixels
 - Y/C Only : up to 480 x 360
 - JPEG+Y/C : 2 M + WQVGA (JPEG High Quality mode)
5 M + WQVGA (JPEG Normal Quality mode)
 - Parallel Input rate: Up to 54 MHz
- SPI Interface for external display
 - PrimeCell® Synchronous Serial Port (PL022)
 - Display resolution
 - High Performance mode: Up to 320 240 15 fps 24 bit RGB
 - Low Power Mode: Up to 176 x 144, 15 fps 24 bit RGB
 - Communication at speeds
 - High Performance mode:
 - Master Half duplex mode: up to 39 Mbit/s (transmit only)
 - Master Full duplex mode: up to 9.75 Mbit/s
 - Low Power mode:
 - Master Half duplex mode: up to 9.75 Mbit/s (transmit only)
 - Master Full duplex mode: up to 6.5 Mbit/s
- SPI Interface for Wi-Fi

- PrimeCell® Synchronous Serial Port (PL022)
- Communication at speeds
 - High Performance mode: up to 13.00 Mbit/s
 - Low Power mode: up to 6.5 Mbit/s

2D Graphics Accelerator

- Bit Block Transfer
- Rotator
 - Supported image format: YCbCr422, RGB565
 - Supported rotate degree: 0, 90, 180, 270
- 3-operand raster operation (ROP3)
- Alpha blending
- Scaling
 - Horizontal direction: x1/64 to x64, Vertical direction: x1/64 to x64
Maximum source input 2880x2160, maximum destination output 768x1024
 - YCbCr 422 16 bpp format

Connectivity and Storage Domain

The key features are:

- USB 2.0 Device
 - Complies with USB 2.0 Specification High-speed up to 480 Mbps
 - Not supported at Low Power mode:
 - On-chip USB PHY transceiver
 - Supports MSC, MTP, CDC, PTP, ACM, and HID class
 - Multi-function
 - Interface: #0/#1/#2
- SD Host Controller Interface
 - SD Memory Card Protocol version 3.0 compatible
 - 8 KByte (32 bit x 2048 word) x2 FIFOs for Tx/Rx
 - Communication speeds
 - High Performance mode: Up to 39.000 MHz
 - Low Power mode: Up to 24.552 MHz
- eMMC Interface
 - eMMC 4.41 Protocol compatible
 - 1 KByte (32 bit x 256 word) x2 FIFOs for Tx/Rx
 - Communication speeds
 - High Performance mode: Up to 39.000 MHz
 - Low Power mode: Up to 24.552 MHz
- UART interfaces for external Wi-Fi and Bluetooth devices:

- PrimeCell® UART (PL011)
- Communication speeds
 - High Performance mode: up to 3 Mbit/s
 - Low Power mode: up to 2 Mbit/s

DMAC

- ADMAC (PL081) supports for memory to memory
- IDMAC (like PL080) supports for SPI for display and UART for BT, BLE, Wi-Fi

Audio Codec Domain

The key features are:

- I2S Bus Interface supports:
 - Two I2S-bus for audio-codec interface with DMA-based operation
 - 16/24 bit per channel data transfers
 - I2S, Left-justified data format
 - Various bit clock frequency and codec clock frequency support
 - Master clock:
 - High Performance mode: 256fs, 128fs, 64fs of bit clock frequency
 - Low power mode: 128fs, 64fs of bit clock frequency
 - Slave clock:
 - High Performance mode: 256fs, 128fs, 64fs of bit clock frequency
 - Low power mode: 128fs, 64fs of bit clock frequency
 - Sampling rate
 - High Performance mode
 - Master mode: 192 kHz, 96 kHz, 48 kHz
 - Slave mode: 192 kHz, 96 kHz, 48 kHz, 44.1 kHz, 16 kHz, 8 kHz
 - Low Power mode
 - Master mode: 96 kHz, 48 kHz
 - Slave mode: 96 kHz, 48 kHz, 44.1 kHz, 16 kHz, 8 kHz
 - Two channels each I2S interface
- Unique Audio Data Format (Pulse Density Modulation) between CXD5602GF/GG and CXD5247GF

This part mainly explains the Application Processor and application memory. For explanations of other separate functional blocks, refer to other sections.

3.13.2 Power Supply Control

The Application Domain is divided into four power domains: the PWD_APP, PWD_APP_DSP, PWD_APP_SUB,

and PWD_APP_AUD. The following describes each functional block of the Application Domain and the corresponding power domains.

- PWD_APP
 - All components of Application Domain
 - Including 1.5 MByte SRAM in Application memory and Application Multi-layer Bus
- PWD_APP_DSP
 - Application & DSP processors
 - ADMAC
- PWD_APP_SUB
 - Connectivity, Storage I/F and Camera, Display Interface in Application Domain
- PWD_APP_AUD
 - Audio Codec

3.13.3 Clock Reset Control

3.13.3.1 Overview of APP Maximum Frequency

From Table APP-766 to Table APP-775 describe the APP maximum operating frequencies of the APP MAIN Bus and the APP SUB Bus to which main functional blocks of the Application Domain are connected. Each has a different maximum operating frequency depending on the supported XOSC frequency and the SYSPLL oscillating frequency. In addition, element circuits such as AudioCodec, USB, eMMC, that are connected to the APP SUB Bus, have the same maximum frequencies as the APP MAIN Bus.

For the maximum operating frequencies of external communication interfaces, refer to separate sections.

Table APP-742 XOSC (26 MHz), High Performance Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
APP MAIN Bus/APP SUB Bus	MHz	97.500	156.000	26.000	8.192	0.032768

Table APP-743 XOSC (26 MHz), Low Power Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
APP MAIN Bus/APP SUB Bus	MHz	39.000	39.000	26.000	8.192	0.032768

3.13.3.2 Clock Reset Generator

The following shows the clock system diagram.

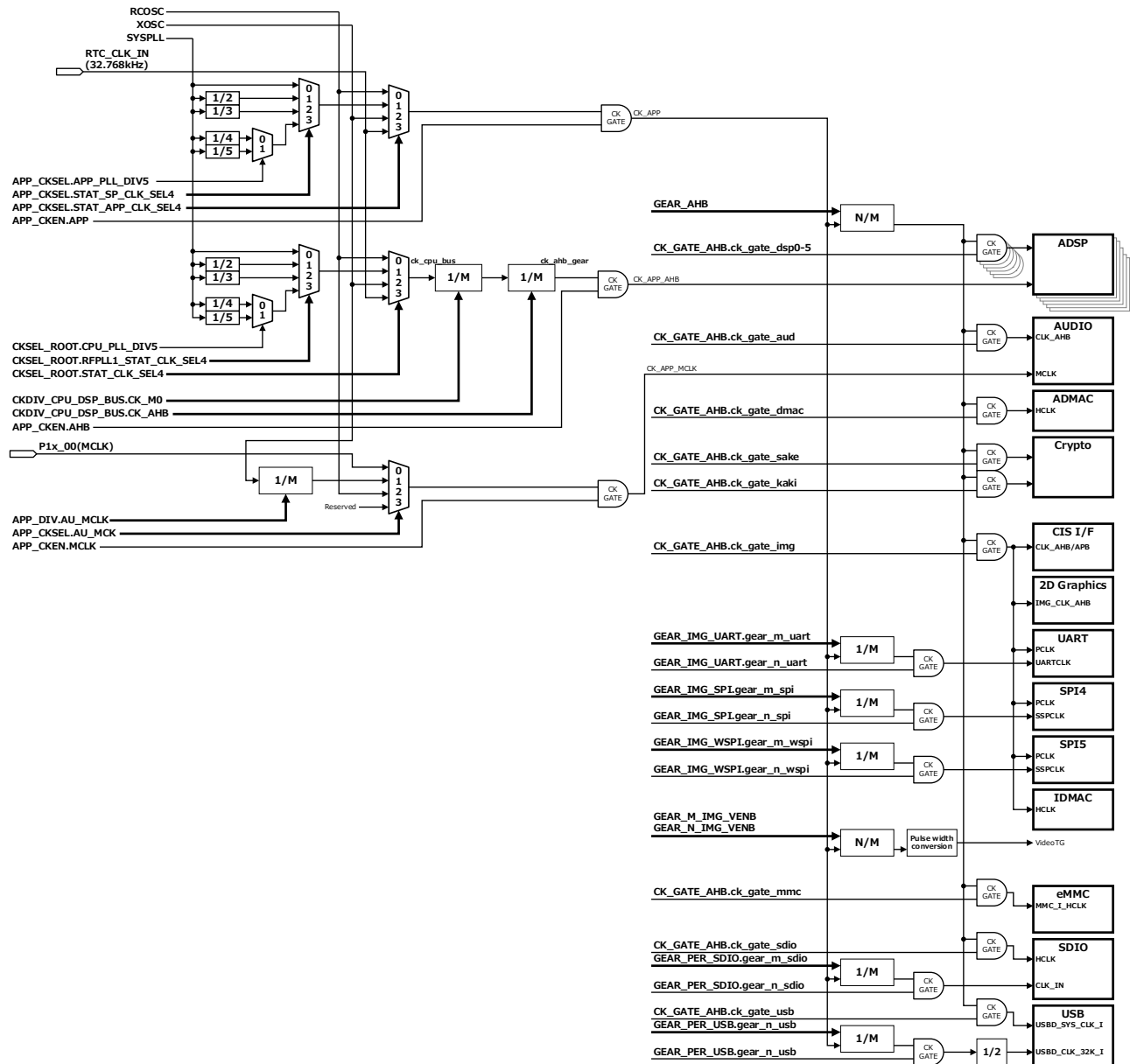


Figure APP-102 Application Domain Clock System

The following shows the reset system diagram.

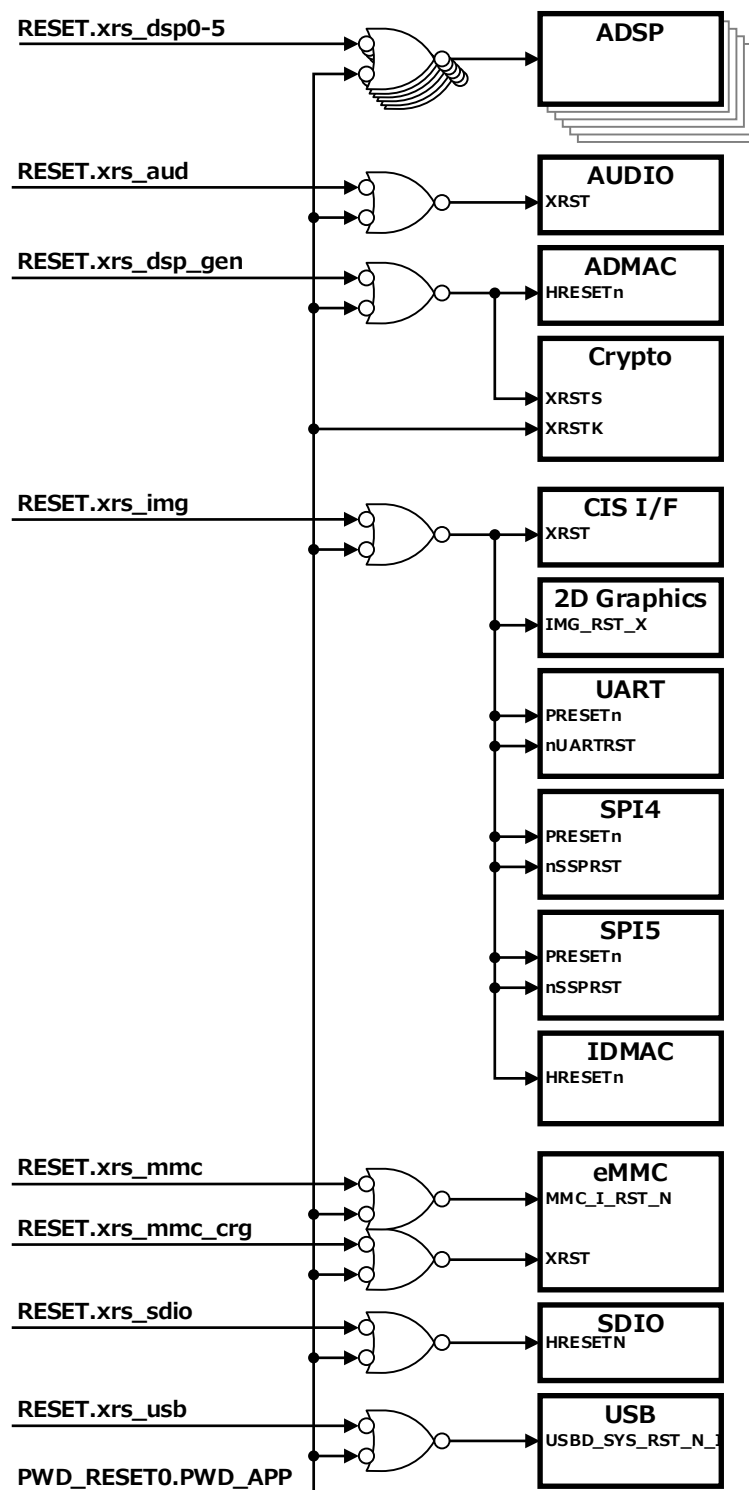


Figure APP-103 Application Domain Reset System

3.13.3.3 Register Descriptions

The following describes setting registers for clock and reset.

Clock division ratio setting and clock switching registers are controlled by the API. The clock setting can be confirmed with the registers described in Table APP-776 and Table APP-777. Make sure to use them as RO registers.

Table APP-744 Clock Division Ratio Setting Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0410341C	APP_DIV	Reserved	RO	[31:3]	0	Reserved
		AU_MCLK	RW	[2:0]	0	AUDIO XOSC division ratio setting 0: clock not divided 1: clock divided by 2 2: clock divided by 3 3: clock divided by 4 4: clock divided by 5 5: clock divided by 6 6: clock divided by 7 7: clock divided by 8

Table APP-745 Clock Switching Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103418	APP_CKSEL	Reserved	RO	[31:18]	0	Reserved
		AU_MCLK	RW	[17:16]	2'b00	Clock source switching for AUDIO 2'b00: External MCLK 2'b01: XOSC divided clock selected by APP_DIV.AU_MCLK 2'b10: RCOSC 2'b11: Prohibited setting
		Reserved	RO	[15:12]	0	Reserved

		STAT_SP_CLK_SEL4	RO	[11:10]	2'b00	Frequency division setting status for CK_APP SYSPLL 2'b00: clock not divided 2'b01: divided by 2 2'b10: divided by 3 2'b11: divided by 4 or 5 (depending on APP_CKSEL.APP_PLL_DIV5)
		STAT_APP_CLK_SEL4	RO	[9:8]	2'b00	Clock source switching status for CK_APP 2'b00: RCOSC 2'b01: SYSPLL divided clock selected by APP_CKSEL.STAT_SP_CLK_SEL4 2'b10: XOSC 2'b11: RTC Clock
		APP_PLL_DIV5	RW	[7]	0	Clock divided by 4 or 5 for CK_APP SYSPLL 0: clock divided by 4 1: clock divided by 5
		Reserved	RW	[6:0]	0	Reserved

Table APP-746 Clock Enable Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103414	APP_CKEN	Reserved	RO	[31:4]	0	Reserved
		AHB	RW	[3]	0	Clock Enable of CK_APP_AHB 0: Clock stopped 1: Clock supplied
		Reserved	RO	[2]	0	Reserved
		MCLK	RW	[1]	0	Clock Enable of CK_APP_MCLK 0: Clock stopped 1: Clock supplied
		APP	RW	[0]	0	Clock Enable of CK_APP 0: Clock stopped 1: Clock supplied

Table APP-747 Clock Reset Generator Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E011000	GEAR_AHB	Reserved	RO	[31:23]	0	Reserved
		gear_n_ahb	RW	[22:16]	7'h1	Division ratio setting of AHB bus clock (numerator) "0" must not be written (because "0" will be overwritten to "1")
		Reserved	RO	[15:7]	0	Reserved
		gear_m_ahb	RW	[6:0]	7'h2	Division ratio setting of AHB bus clock (denominator) "0" or values which are applicable to the formula "gear_n_ahb > gear_m_ahb" must not be written. (If that is done, gear_n_ahb will be overwritten to 7'h7f, and gear_m_ahb, to 7'h7f. (Operationally, it means 1/1.))
0x0E011004	GEAR_IMG_UART	Reserved	RO	[31:17]	0	Reserved
		gear_n_uart	RW	[16]	0	UART2 Clock Enable 0: Clock stopped 1: Clock supplied
		Reserved	RO	[15:7]	0	Reserved
		gear_m_uart	RW	[6:0]	7'h4	Division ratio setting of UART2 clock (denominator) "0" must not be written.
0x0E011008	GEAR_IMG_SPI	Reserved	RO	[31:17]	0	Reserved
		gear_n_spi	RW	[16]	0	SPI4 Clock Enable 0: Clock stopped 1: Clock supplied
		Reserved	RO	[15:7]	0	Reserved
		gear_m_spi	RW	[6:0]	7'h4	Division ratio setting of SPI4 clock (denominator) "0" must not be written.
0x0E01100C	GEAR_PER_SDIO	Reserved	RO	[31:17]	0	Reserved

		gear_n_sdio	RW	[16]	0	SDIO Clock Enable 0: Clock stopped 1: Clock supplied
		Reserved	RO	[15:2]	0	Reserved
		gear_m_sdio	RW	[1:0]	2'h2	Division ratio setting of SDIO Clock (denominator) “0” must not be written.
0x0E011010	GEAR_PER_USB	Reserved	RO	[31:17]	0	Reserved
		gear_n_usb	RW	[16]	0	Division ratio setting of USB Clock (numerator) 0: Clock stopped Clock is output when RESET.xrs_usb equals 1'b1.
		Reserved	RO	[15:12]	0	Reserved
		gear_m_usb	RW	[11:0]	12'h2	Division ratio setting of USB clock (denominator) “0” must not be written.
0x0E011014	GEAR_M_IMG_VENB	gear_m_img_venb	RW	[31:0]	0	Division ratio setting of VideoTG (denominator) Set values are not reflected until they are written in GEAR_N_IMG_VENB. “0” or values which are applicable to the formula “GEAR_N_IMG_VENB > GEAR_M_IMG_VENB” must not be written.
0x0E011018	GEAR_N_IMG_VENB	gear_n_img_venb	RW	[31:0]	0	Division ratio setting of VideoTG (numerator) 0: Clock stopped VideoTG is output when RESET.xrs_img equals 1'b1. Values of GEAR_M_IMG_VENB and GEAR_N_IMG_VENB are reflected in divider circuits by writing them in this register.
0x0E01101C	GEAR_IMG_WSPI	Reserved	RO	[31:17]	0	Reserved

		gear_n_img_wspi	RW	[16]	0	Division ratio setting of SPI5 clock (numerator) 0: Clock stopped 1: Clock supplied
		Reserved	RO	[15:4]	0	Reserved
		gear_m_img_wspi	RW	[3:0]	4'h4	Division ratio setting of SPI5 clock (denominator) "0" must not be written.
0x0E011020	CKEN_EMMC	Reserved	RO	[31:3]	0	Reserved
		cken_emmc_smp	RW	[2]	0	eMMC Sample Clock Enabler 0: Clock stopped 1: Clock supplied
		cken_emmc_drv	RW	[1]	0	eMMC DRV Clock Enabler 0: Clock stopped 1: Clock supplied
		cken_emmc_clkln	RW	[0]	0	eMMC Clock Enabler 0: Clock stopped 1: Clock supplied
0x0E011030	RESET	Reserved	RO	[31:23]	0	Reserved
		xrs_dsp_gen	RW	[22]	0	DSP GENERAL/Reset Register 0: Reset assert 1: Reset release
		xrs_dsp5	RW	[21]	0	Reset Register for ADSP5 0: Reset assert 1: Reset release
		xrs_dsp4	RW	[20]	0	Reset Register for ADSP4 0: Reset assert 1: Reset release
		xrs_dsp3	RW	[19]	0	Reset Register for ADSP3 0: Reset assert 1: Reset release
		xrs_dsp2	RW	[18]	0	Reset Register for ADSP2 0: Reset assert 1: Reset release
		xrs_dsp1	RW	[17]	0	Reset Register for ADSP1 0: Reset assert 1: Reset release

		xrs_dsp0	RW	[16]	0	Reset Register for ADSP0 0: Reset assert 1: Reset release
		Reserved	RO	[15:12]	0	Reserved
		xrs_mmc_crg	RW	[11]	0	eMMC CRG Reset Register 0: Reset assert 1: Reset release
		xrs_mmc	RW	[10]	0	eMMC Reset Register 0: Reset assert 1: Reset release
		xrs_sdio	RW	[9]	0	SDIO Reset Register 0: Reset assert 1: Reset release
		xrs_usb	RW	[8]	0	USB Reset Register 0: Reset assert 1: Reset release
		Reserved	RO	[7:5]	0	Reserved
		xrs_img	RW	[4]	0	Image Reset Register 0: Reset assert 1: Reset release
		Reserved	RO	[3:1]	0	Reserved
		xrs_aud	RW	[0]	0	PWD_AUD/Reset Register 0: Reset assert 1: Reset release
0x0E011040	CK_GATE_AHB	Reserved	RO	[31:29]	0	Reserved
		ck_gate_dmac	RW	[28]	0	ADMAC ClockGate Register 0: Clock stopped 1: Clock supplied
		Reserved	RO	[27:22]	0	Reserved
		ck_gate_dsp5	RW	[21]	0	ADSP5 ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_dsp4	RW	[20]	0	ADSP4 ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_dsp3	RW	[19]	0	ADSP3 ClockGate Register 0: Clock stopped 1: Clock supplied

		ck_gate_dsp2	RW	[18]	0	ADSP2 ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_dsp1	RW	[17]	0	ADSP1 ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_dsp0	RW	[16]	0	ADSP0 ClockGate Register 0: Clock stopped 1: Clock supplied
		Reserved	RO	[15:11]	0	Reserved
		ck_gate_mmc	RW	[10]	0	eMMC (AHB Bus) ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_sdio	RW	[9]	0	SDIO (AHB Bus) ClockGate Register 0: Clock stopped 1: Clock supplied
		ck_gate_usb	RW	[8]	0	USB (AHB Bus) ClockGate Register 0: Clock stopped 1: Clock supplied
		Reserved	RO	[7:5]	0	Reserved
		ck_gate_img	RW	[4]	0	Image (AHB Bus) ClockGate Register 0: Clock stopped 1: Clock supplied
		Reserved	RO	[3:1]	0	Reserved
		ck_gate_aud	RW	[0]	0	Audio (AHB Bus) ClockGate Register 0: Clock stopped 1: Clock supplied

Table APP-748 APP SRAM Tile Clock Gating Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E001084	APP_TILE_CLK_GATEING_ENB	Reserved	RO	[31:12]	0	Reserved
		tile11_clk_gating_enb	RW	[11]	0	APP SRAM Tile 11 ClockGate 0: Clock stopped 1: Clock supplied
		tile10_clk_gating_enb	RW	[10]	0	APP SRAM Tile 10 ClockGate 0: Clock stopped 1: Clock supplied

		tile9_clk_gating_enb	RW	[9]	0	APP SRAM Tile 9 ClockGate 0: Clock stopped 1: Clock supplied
		tile8_clk_gating_enb	RW	[8]	0	APP SRAM Tile 8 ClockGate 0: Clock stopped 1: Clock supplied
		tile7_clk_gating_enb	RW	[7]	0	APP SRAM Tile 7 ClockGate 0: Clock stopped 1: Clock supplied
		tile6_clk_gating_enb	RW	[6]	0	APP SRAM Tile 6 ClockGate 0: Clock stopped 1: Clock supplied
		tile5_clk_gating_enb	RW	[5]	0	APP SRAM Tile 5 ClockGate 0: Clock stopped 1: Clock supplied
		tile4_clk_gating_enb	RW	[4]	0	APP SRAM Tile 4 ClockGate 0: Clock stopped 1: Clock supplied
		tile3_clk_gating_enb	RW	[3]	0	APP SRAM Tile 3 ClockGate 0: Clock stopped 1: Clock supplied
		tile2_clk_gating_enb	RW	[2]	0	APP SRAM Tile 2 ClockGate 0: Clock stopped 1: Clock supplied
		tile1_clk_gating_enb	RW	[1]	0	APP SRAM Tile 1 ClockGate 0: Clock stopped 1: Clock supplied
		tile0_clk_gating_enb	RW	[0]	0	APP SRAM Tile 0 ClockGate 0: Clock stopped 1: Clock supplied

Table APP-749 Reset Control Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04103408	SWRESET_APP	Reserved	RO	[31:1]	0	Reserved
		APP_DBG	RW	[0]	0	Debug Reset of ADSP

3.13.4 Description of APP_DSP Function

3.13.4.1 Overview and Features

The APP_DSP is a sub block in the Application Domain. It consists of the following:

1. six Cortex®-M4 processors with FPU
2. 1.5 Mbyte of SRAM
3. Audio and Imaging (2D Graphics, CIF I/F)
4. Storage (eMMC, USB)
5. buses to connect 1 to 5 functional blocks above.

The APP_DSP is mainly used for executing Main program and controlling other sub blocks.

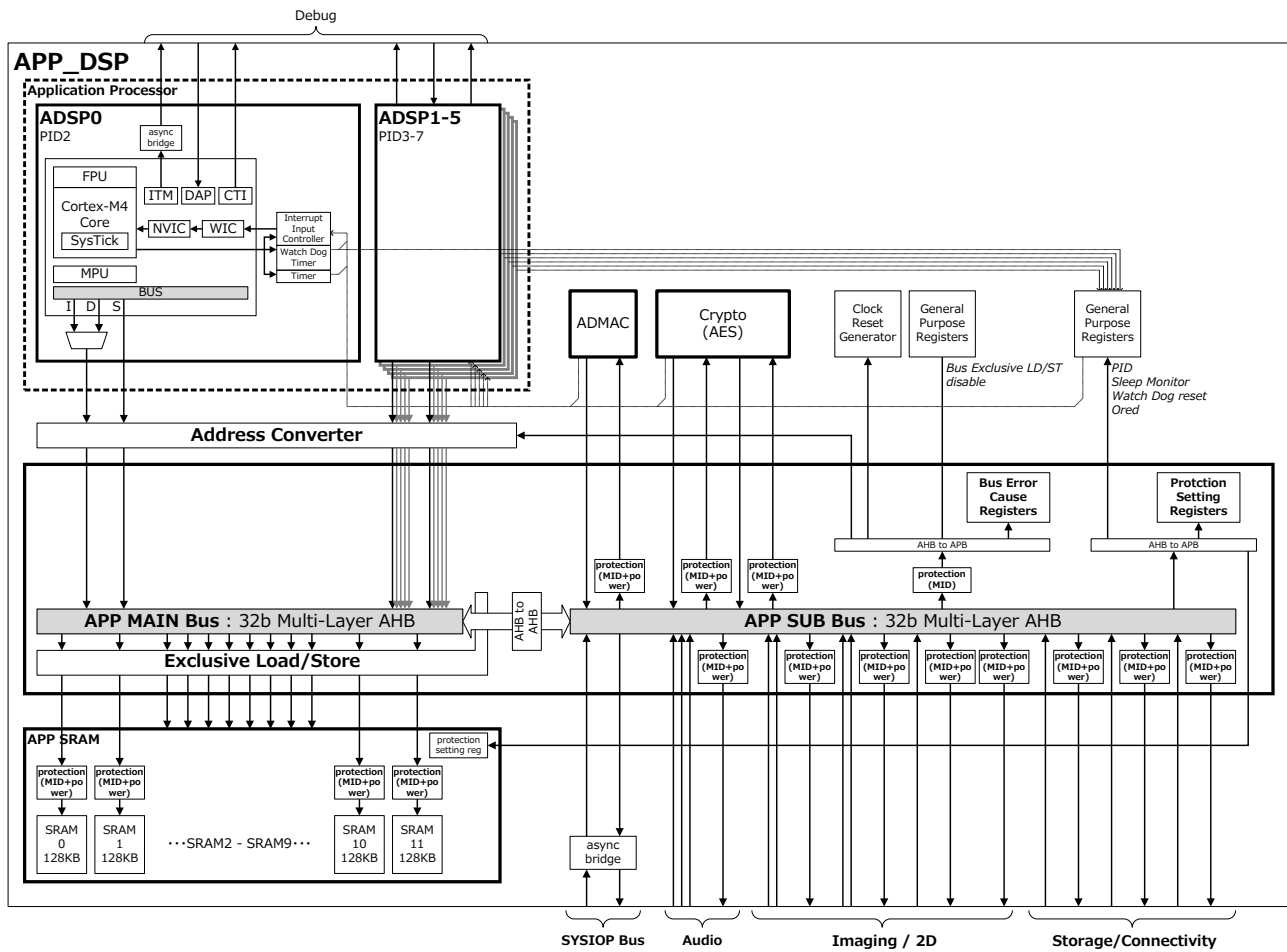


Figure APP-104 APP_DSP Block Diagram

3.13.4.2 Function List

Table APP-782 shows the functions of the APP_DSP.

Table APP-750 APP_DSP Function List

No	Function Name	Description
ADSP		
1	Cortex [®] -M4 processor with FPU	The APP_DSP equips six Cortex [®] -M4 processors with FPU in total.
2	Processor ID	The APP_DSP has unique ID for each processor. Slave access control can be set for each ID. The ID of each processor can be confirmed by reading registers.
3	Interrupt Controller	This function controls interrupts which are input to each processor via Private Peripheral Bus of Cortex [®] -M4 processors with FPU.
4	Timer	The Timer is used for general purpose, with two input ports, and can be controlled via Private Peripheral Bus of the Cortex [®] -M4 processor with FPU
5	Watchdog Timer	The Watchdog Timer can be controlled via Private Peripheral Bus of the Cortex [®] -M4 processor with FPU.
6	SLEEPING Signal Monitor	This function enables to confirm the SLEEPING signal status of each processor by reading registers.
7	Debug Function	The APP_DSP has the debug block which offers SWD, Trace, and Cross-Trigger functions.
8	I/D Multiplexor	This function multiplexes ICode bus and DCode bus of the Cortex [®] -M4 processor with FPU in order of fixed priority (DCode has a higher priority than ICode).
BUS		
9	Address Map	The Address Map enables to access memories and control a variety of programmable functions via buses.
10	Address Converter	This function converts addresses of virtual memory space for every 64 Kbyte logical area.
11	Bus Matrix	The Bus Matrix includes multi-layer matrix in the sub block based on the AMBA [®] 3 AHB-Lite protocol and bridges which connect AHBs between the blocks.
12	Exclusive Load/Store	This function performs monitoring and controlling of exclusive accesses to a specific SRAM Tile.
13	Protection and Error Information Register	This function blocks accesses from unprivileged bus masters to a specific bus slave, or a bus slave which is in the status that the power is turned off. The function has a register to hold access error information when an unprivileged access occurs.
14	SYSIOP Bridge	Bus Matrix of the APP SUB Bus connects to the upper-layer SYSIOP bus of the APP_DSP block via the asynchronous bridge.
15	ADMAC	Refer to the Section of the DMAC (3.8).

Memory		
16	SRAM with protection feature	The SRAM module consists of 128 KByte Logic Tile units, holding access control function for each tile, and AHB slave interface.
Clock Reset		
17	Clock Reset Generator	The Clock Reset Generator generates clocks and resets required for the sub block in the Application Domain.
Other		
18	Interrupt Output	For the main purpose of debugging, this function outputs interrupts which occur in the APP_DSP block for the processors in the SYSIOP block and the GNSS block.

3.13.4.3 Register List

Table APP-751 APP_DSP Register List

Address	Register Name	Type	Description	Initial Value
0x0E002040	PID	RO	Processor ID	-
0x0E002044	DSP_SLEEPING	RO	SLEEPING Signal Monitor	0
0x0E002048	WD_TIM_RES	RO	Watchdog Timer Status	0
0x0E010000	BUS_ERROR0	WO	BUS ERROR Clear Register	0
0x0E010004	BUS_ERROR1	RO	BUS ERROR Cause Register (Error Type)	0
0x0E010008	BUS_ERROR2	RO	BUS ERROR Cause Register (Master ID)	0
0x0E012004 0x0E012020	ACNV_P0_DST_{0-7}	RW	Address Converter (ADSP0)	-
0x0E012024 0x0E012040	ACNV_P1_DST_{0-7}	RW	Address Converter (ADSP1)	-
0x0E012044 0x0E012060	ACNV_P2_DST_{0-7}	RW	Address Converter (ADSP2)	-
0x0E012064 0x0E012080	ACNV_P3_DST_{0-7}	RW	Address Converter (ADSP3)	-
0x0E012084 0x0E0120A0	ACNV_P4_DST_{0-7}	RW	Address Converter (ADSP4)	-
0x0E0120A4 0x0E0120C0	ACNV_P5_DST_{0-7}	RW	Address Converter (ADSP5)	-

0x0E013000	BUS_SNOOP_DISABLE	RW	Exclusive Access Control	1
0xE0043000	Timer	RW	Refer to Section 3.13.4.7	-
0xE0044000	Watchdog Timer	RW	Refer to Section 3.13.4.8	-
0xE0045000	Interrupt controller	RW	Refer to Section 3.13.4.6 For details, refer to Section of the Interrupt (3.3).	-

3.13.4.4 Cortex[®]-M4 processor with FPU

The APP_DSP equips six Cortex[®]-M4 processors with FPU. On the APP_DSP Bus Matrix, regardless of the endianness of the processor, byte lanes in the little endian are used.

Table APP-784 describes the functions of the Cortex[®]-M4 processor with FPU.

Table APP-752 Cortex[®]-M4 processor with FPU Function List

Function	Description
Memory Protection Unit (MPU)	Memory Protection Unit is equipped. It can control eight independent areas.
Floating Point Unit (FPU)	A calculation function of single precision floating point number is supported.
Nested Vectored Interrupt Controller (NVIC)	The NVIC supports 128 interrupts. The priority of each interrupt can be set in 256 steps.
Wakeup Interrupt Controller (WIC)	Wakeup Interrupt Controller (WIC) is equipped.
WIC Support Signal	The WIC interface uses NMI, EDBGRQ, RXEV, and IRQ[127:0] to detect Wakeup Interrupts.
Trace Support Level	The ITM, TPIU, DWT trigger, and counter are supported. The ETM and HTM are not supported.
Debug Support Level	All debug functions except for data matching are supported.
Bit-band	A bit-band function is not supported in this system.

For Intellectual Property cores (IP cores) offered by ARM Limited, refer to the following references.

- Arm[®] Cortex[®]-M4 Processor Technical Reference Manual
- Cortex[®]-M4 Devices Generic User Guide
- ARMv7-M Architecture Reference Manual

3.13.4.5 Processor ID

Processor ID register is used for each processor to recognize its own ID. Each processor can obtain its own ID by accessing the address, which can be seen the same from each processor, to read the register. (Each processor cannot access the ID of other processors.)

Table 3.31 20 shows Processor ID registers which can be seen from each processor.

Table APP-753 Register List

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E002040	PID	PID	RO	[3:0]	(1*)	Processor ID (1*) Each processor can read the value which are indicated in Table APP-786.

Table APP-754 Processor List

Processor Name	Processor ID
ADSP0	2
ADSP1	3
ADSP2	4
ADSP3	5
ADSP4	6
ADSP5	7

3.13.4.6 Interrupt Controller

The 128 bit interrupt signals are connected to each processor. By using the interrupt controller, confirmation of the interrupt state, interrupt enable or disable, and the polarity reverse of the interrupt can be performed.

Since the control registers of the interrupt controller for each processor are in the Private Peripheral Bus area, they can be accessed in Privileged Mode only. For details, refer to Section of Interrupt (3.3).

3.13.4.7 Timer

As general-purpose timers, Dual input Timers of AMBA® Design Kit Technical Reference Manual are equipped. One timer for every processor, six timers in total are equipped. Since the control registers of the timer for each processor are in the Private Peripheral Bus area, they can be accessed in Privileged Mode only.

For detailed control method, refer to AMBA® Design Kit Technical Reference Manual.

The base address of the control register is 0xE0043000. Each control register can be accessed with the same address from each processor.

3.13.4.8 Watchdog Timer

As Watchdog Timers, Watchdog units of AMBA® Design Kit Technical Reference Manual are equipped.

One timer for every processor, six timers in total are equipped. Since the registers of the Watchdog Timer for each processor are in the Private Peripheral Bus area, they can be accessed in Privileged Mode only.

For detailed control method, refer to AMBA® Design Kit Technical Reference Manual.

The base address of the control register is 0xE0044000. Each control register can be accessed with the same address from each processor.

WDTRES signals of each Watchdog Timer are not connected to the reset signals of the corresponding processor, but to the NMI. (Enable control of the WDTRES signals can be performed.)

Furthermore, 1 bit signal which is ORed among all WDTRES signals of the ADSP are connected to the WIC of the ADSP through the interrupt controller of each ADSP. The same 1 bit signal is also connected to the System and I/O Processor.

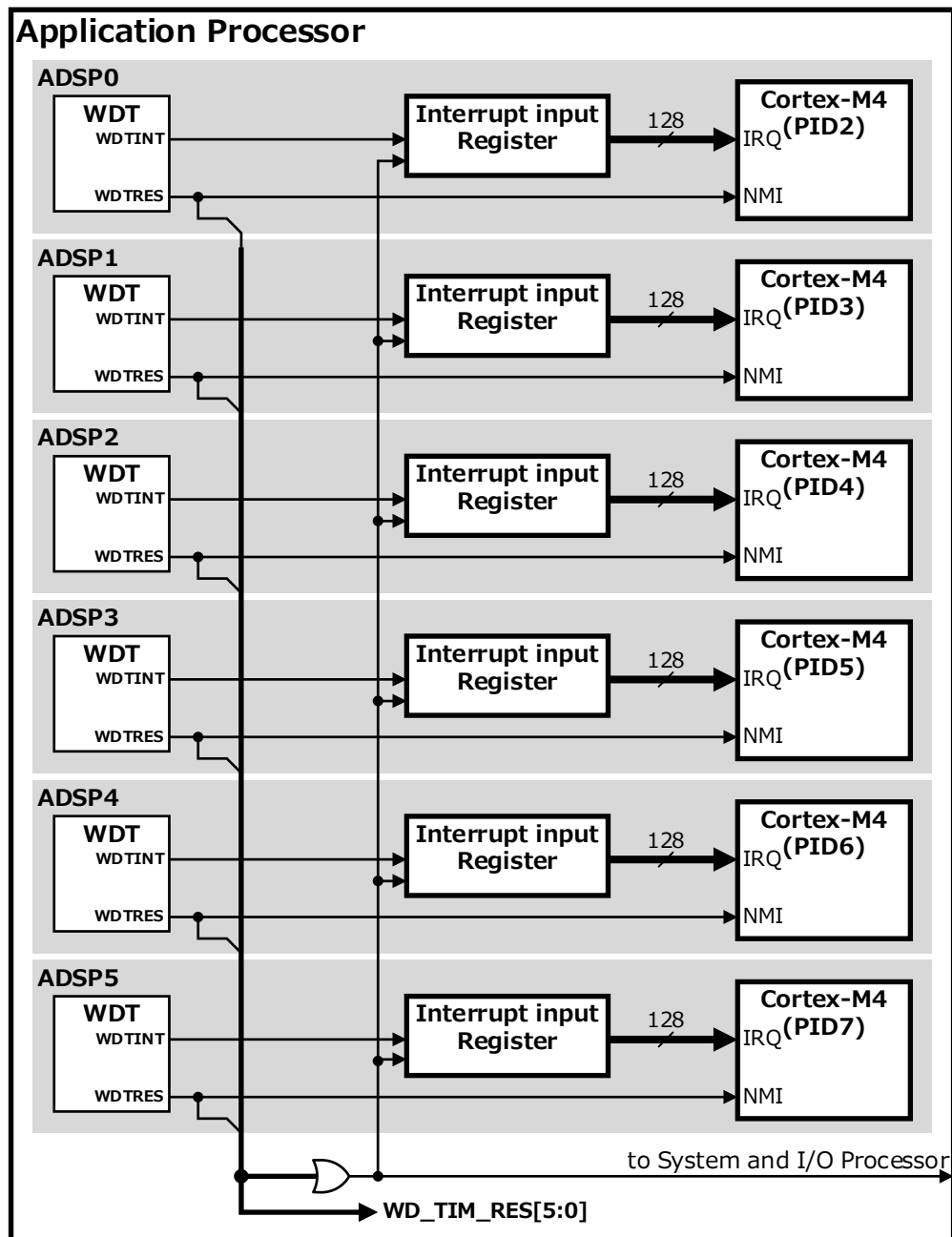


Figure APP-105 WDTRES Connection

All the WDTRES signal status of the ADSP can be confirmed by reading the registers.

Table APP-755 WDTRES Register List

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E002048	WD_TIM_RES	Reserved	RO	[31:6]	0	Reserved
		wd_tim_res_5	RO	[5]	0	Reset status of Watchdog Timer of ADSP5
		wd_tim_res_4	RO	[4]	0	Reset status of Watchdog Timer of ADSP4
		wd_tim_res_3	RO	[3]	0	Reset status of Watchdog Timer of ADSP3
		wd_tim_res_2	RO	[2]	0	Reset status of Watchdog Timer of ADSP2
		wd_tim_res_1	RO	[1]	0	Reset status of Watchdog Timer of ADSP1
		wd_tim_res_0	RO	[0]	0	Reset status of Watchdog Timer of ADSP0

3.13.4.9 SLEEPING Signal Monitor

You can confirm whether each ADSP is in stopped state (Sleep-now or Sleep-on-exit mode) or not by reading registers shown below.

Table APP-756 SLEEPING Signal Register List

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E002044	DSP_SLEEPING	Reserved	RO	[31:6]	0	Reserved
		dsp_sleeping_5	RO	[5]	0	Stopped state of ADSP5
		dsp_sleeping_4	RO	[4]	0	Stopped state of ADSP4
		dsp_sleeping_3	RO	[3]	0	Stopped state of ADSP3
		dsp_sleeping_2	RO	[2]	0	Stopped state of ADSP2
		dsp_sleeping_1	RO	[1]	0	Stopped state of ADSP1
		dsp_sleeping_0	RO	[0]	0	Stopped state of ADSP0

3.13.4.10 Debug Function

For debugging of each ADSP, Serial Wire Debug (two-wire protocol) can be used. It supports the following functions.

Table APP-757 Debug Function List

Function Name	Description
Multi-Core-Debug	Embedded multi-core debug function is supported.
System-Debug	System debug function is supported. Without halting the ADSP, debug access to the memories is possible.
Debugger	AS Integrated Development Environment of Embedded multi-core, YDC advice LUNA II (customized for CXD5602) environment can be used. Arm® DS-5 environment and DSTREAM as debug adaptor are supported. (The number of processors which can be debugged simultaneously is limited.)
FPB	Eight-breakpoint function is equipped including FPB (4K) in the configuration of Cortex®-M4 processor with FPU. FPB unit contains the following components: • Two literal comparators Two literal comparators for matching against literal loads from Code space, and remapping to a corresponding area in System space. • Six instruction comparators Six instruction comparators for matching against instruction fetches from Code space, and remapping to a corresponding area in System space. Alternatively, you can configure the comparators individually to return a Breakpoint Instruction (BKPT) to the processor core on a match, to provide hardware breakpoint capability.
DWT	Four-watchpoint function is supported including a reduced DWT (7K) to the configuration of Cortex®-M4 processor with FPU.
ITM	Instrumentation Trace Macrocell (ITM) function in Cortex®-M4 processor with FPU is supported.
TRACE	Data tracing and software tracing functions using ITM/DWT features of Cortex®-M4 processor with FPU are supported. Clock synchronized signals are output from Tracedata.
AUTH	Debug I/F Authentication function is supported.

3.13.4.11 I/D Multiplexor

Master ports of the ICode and DCode of each ADSP are connected to a master port.

When the ICode and the DCode access the master port simultaneously, DCode has a higher priority than ICode.

3.13.4.12 Address Map

Figure APP-106 shows a map showing how to access resource of the APP_DSP via buses.

For external access of each ADSP, there are three AHP Lite master ports, which can be seen as the Application Processor View. ICode bus is used for instruction fetch of the code memory region (0x00000000 - 0x1FFFFFFFC), DCode bus is used for data and the debug access of the code memory region (0x00000000 - 0x1FFFFFFF), and System bus is used for instruction fetch, data, and the debug access of the address regions (0x20000000 - 0xDFFFFFFF and 0xE0100000 - 0xFFFFFFFF). Please note that 0x22000000 - 0x23FFFFFFF region and 0x42000000 - 0x43FFFFFFF region of the Application Processor View cannot be accessed.

The Application Processor View's three regions: 0x00000000 - 0x0FFFFFFF region, 0x20000000 - 0x2FFFFFFF region, and 0x40000000 - 0x4FFFFFFF region are mapped in 0x00000000 - 0x0FFFFFFF region. Then, using address converter, the 0x00000000 - 0x000FFFFF region can be remapped, being controlled by the program, as the APP Window, GNSS Window, and SYS Window.

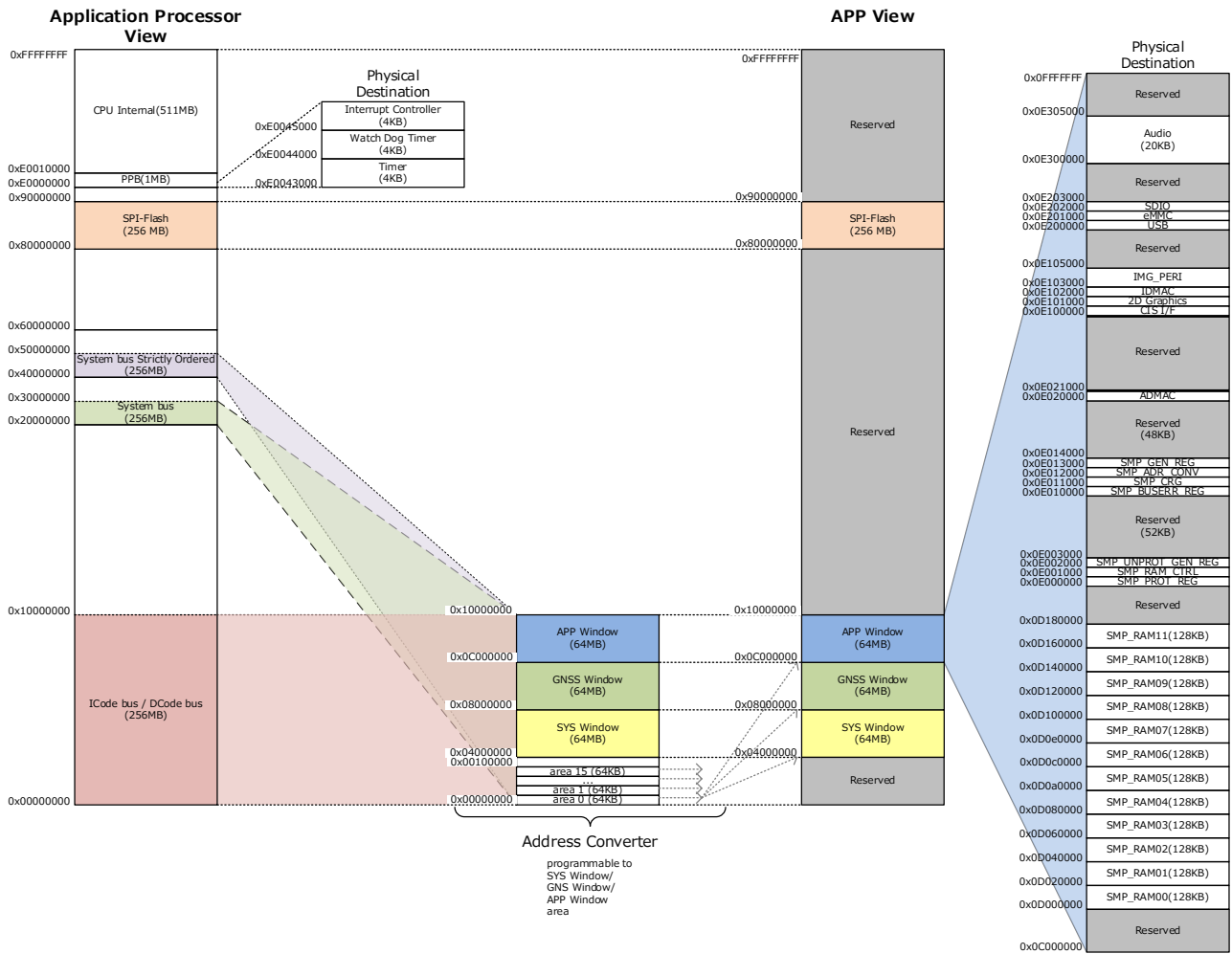


Figure APP-106 Address Map

3.13.4.13 Address Converter

Address converter offers the function that converts address signals from each ADSP into 96 MByte of region in total, when the address signals are within 1 MByte of region from 0x00000000 to 0x000FFFFFF. The remapped regions are from 0x04000000 to 0x05FFFFFFF, from 0x08000000 to 0x09FFFFFFF, and from 0x0C000000 to 0x0DFFFFFFF, which are 32 MByte individually.

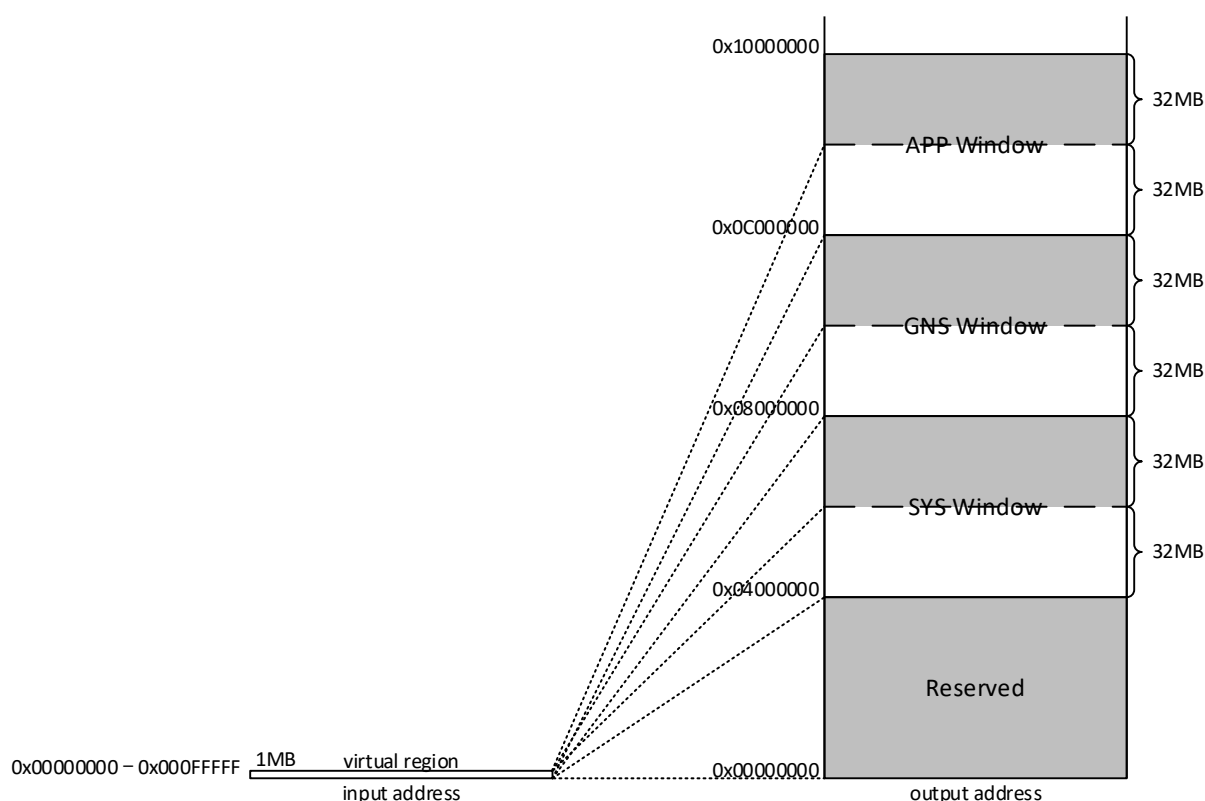


Figure APP-107 Input-Output Addresses of Address Converter

Address converter can be set on each ADSP, furthermore, on 16 areas of each 64 Kbyte individually. As Figure APP-108 indicates, address converter realizes the above conversion function that identifies areas by using input address bit [19:16] and replaces output address bits [27:26] and [24:16] with set values against the areas. As the conversion is performed by every 64 Kbyte, an input address less than 64 Kbyte corresponding to the input address bit [15:0] becomes to be an output address without conversion. In addition, address signals are transferred with no latency from input to output.

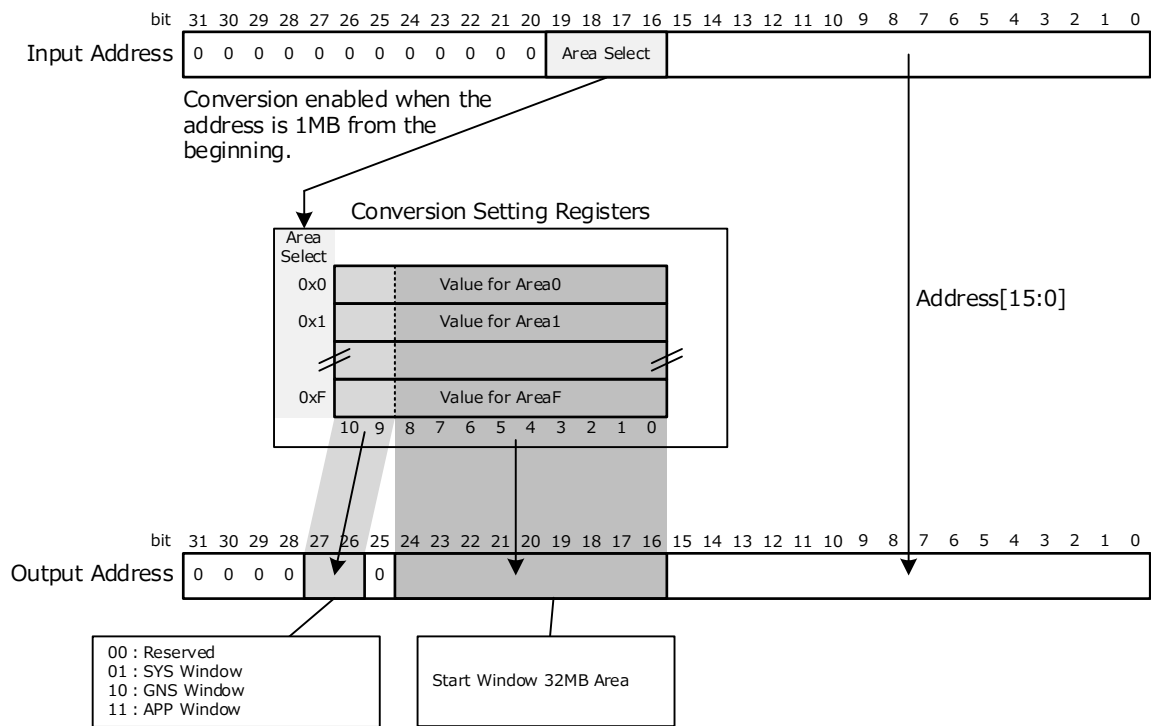


Figure APP-108 Address Conversion Operation Scheme

Timing control function of reflecting the address converter setting is not equipped. For this reason, set value change must be performed during the period that there are no bus transactions of the target ADSP between the address area before conversion and the address area after conversion. Any accesses to undefined addresses are prohibited.

Table APP-790 shows address conversion registers.

Table APP-758 Address Conversion Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E012004 +<N>*0x020	ACNV_P<N>_DST_0	AREA_1	RW	[26:16]	0x001	Destination address after conversion of ADSP<N> area 1 (64 – 128 KByte address area)
		AREA_0	RW	[10:0]	0x000	Destination address after conversion of ADSP<N> area 0 (0 – 64 KByte address area)
0x0E012008 +<N>*0x020	ACNV_P<N>_DST_1	AREA_3	RW	[26:16]	0x003	Destination address after conversion of ADSP<N> area 3 (192 - 256 KByte address area)
		AREA_2	RW	[10:0]	0x002	Destination address after conversion of ADSP<N> area 2 (128 - 192 KByte address area)
0x0E01200C +<N>*0x020	ACNV_P<N>_DST_2	AREA_5	RW	[26:16]	0x005	Destination address after conversion of ADSP<N> area 5 (320 - 384 KByte address area)
		AREA_4	RW	[10:0]	0x004	Destination address after conversion of ADSP<N> area 4 (256 - 320 KByte address area)
0x02012010 +<N>*0x020	ACNV_P<N>_DST_3	AREA_7	RW	[26:16]	0x007	Destination address after conversion of ADSP<N> area 7 (448 - 512 KByte address area)
		AREA_6	RW	[10:0]	0x006	Destination address after conversion of ADSP<N> area 6 (384 - 448 KByte address area)
0x0E012014 +<N>*0x020	ACNV_P<N>_DST_4	AREA_9	RW	[26:16]	0x009	Destination address after conversion of ADSP<N> area 9 (576 - 640 KByte address area)
		AREA_8	RW	[10:0]	0x008	Destination address after conversion of ADSP<N> area 8 (512 - 576 KByte address area)
0x0E012018 +<N>*0x020	ACNV_P<N>_DST_5	AREA_B	RW	[26:16]	0x00B	Destination address after conversion of ADSP<N> area B (704 - 768 KByte address area)

		AREA_A	RW	[10:0]	0x00A	Destination address after conversion of ADSP<N> area A (640 - 704 KByte address area)
0x0E01201C +<N>*0x020	ACNV_P<N>_DST_6	AREA_D	RW	[26:16]	0x00D	Destination address after conversion of ADSP<N> area D (832 - 896 KByte address area)
		AREA_C	RW	[10:0]	0x00C	Destination address after conversion of ADSP<N> area C (768 - 832 KByte address area)
0x0E012020 +<N>*0x020	ACNV_P<N>_DST_7	AREA_F	RW	[26:16]	0x00F	Destination address after conversion of ADSP<N> area F (960 - 1024 KByte address area)
		AREA_E	RW	[10:0]	0x00E	Destination address after conversion of ADSP<N> area E (896 - 960 KByte address area)

Note: about <N>

E.g., ADSP0 means that N = 0, ADSP1 means that N = 1, in the same way, ADSP5 means that N = 5.

Examples of Address Conversion

Below are setting examples showing conversion from 0x00000000 - 0x0001FFFF region into 0x0D000000 - 0x0D01FFFF region which is seen from ADSP0, and conversion from 0x00000000 - 0x0001FFFF region into 0x0D020000 - 0x0D03FFFF region which is seen from ADSP1.

ACNV_P0_DST_0 = 0x07010700

ACNV_P1_DST_0 = 0x07030702

Figure APP-109 and Figure APP-110 show these conversion schemes.

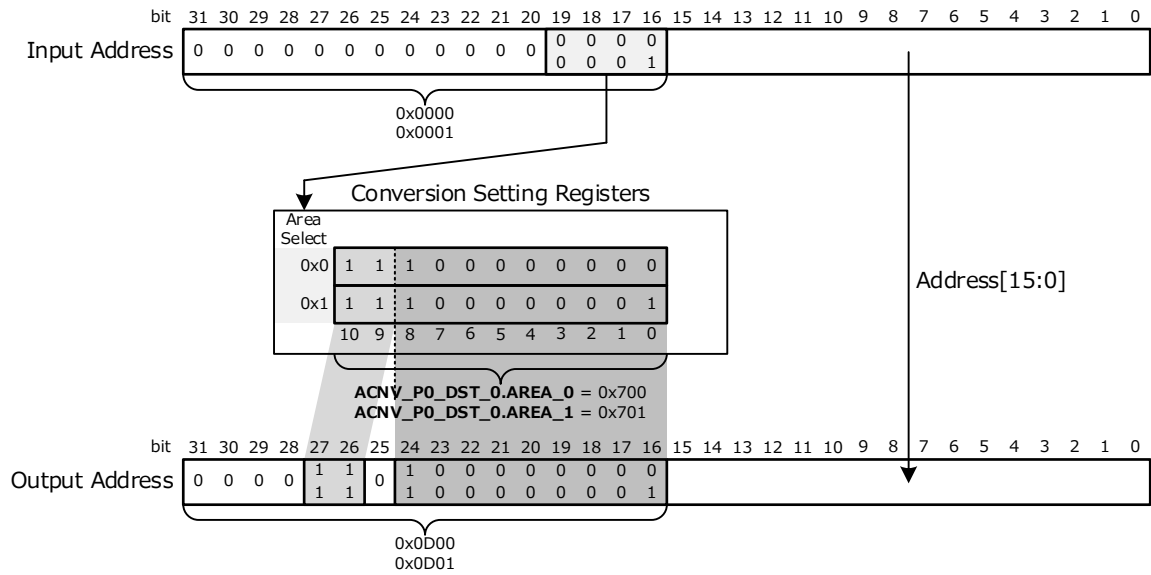


Figure APP-109 Example of Address Conversion: Conversion of Bit Assignment for ADSP0

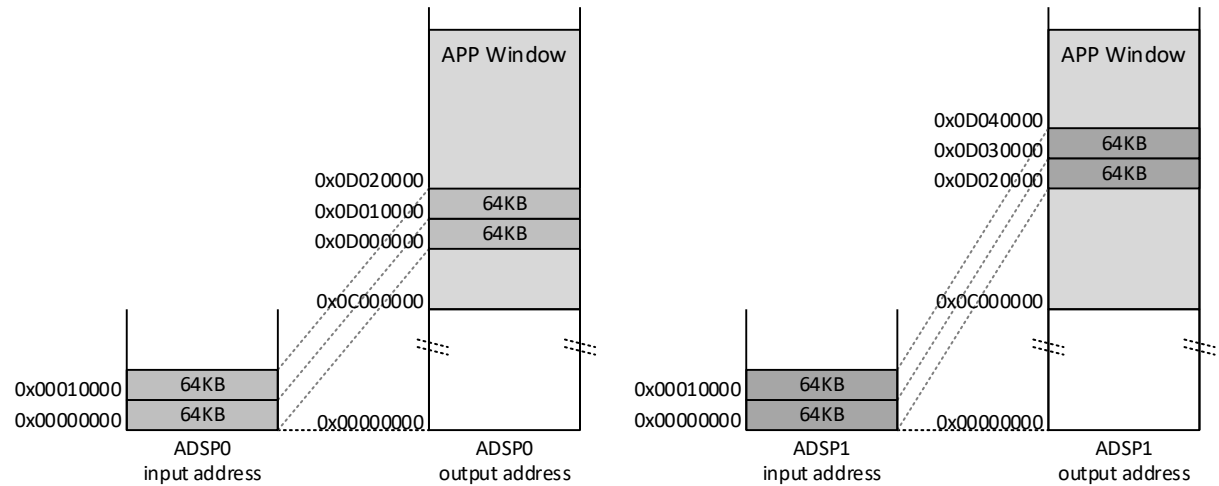


Figure APP-110 Example of Address Conversion: Conversion Address Map for ADSP0 and ADSP1

3.13.4.14 Bus Matrix

APP_DSP has two multi-layer AHB matrixes. APP MAIN Bus matrix uses a processor as a master, and has SRAM with protection features as a slave. APP SUB Bus matrix has a connection interface for three sub blocks: PWD_APP_AUD, APP_IMG, and APP_PER mainly used for PWD_APP, and has data of each functional block inside APP_DSP and control interface. Figure APP-104 shows the connection overview.

Only when simultaneous accesses to a single slave occurs, arbitration operates according to the multi-layer AHB matrix. The algorithm of the arbitration is round-robin.

3.13.4.15 Exclusive Load/Store

Monitoring and controlling of exclusive accesses to slaves are performed.

One monitoring of access per APP SRAM tile (12 in total) and one monitoring of access from APP MAIN Bus to APP SUB Bus are performed.

By setting the register, this function can be enabled or disabled.

When **BUS_SNOOP_DISABLE.bus_snoop_disable** = 1'b1, all accesses receive “success” response.

Switch **BUS_SNOOP_DISABLE** at the timing when **LDREX/STREX** is ensured not to be issued. In the case that it was switched while LDREX or STREX are in use, the snooping of the Bus will be finished.

When **BUS_SNOOP_DISABLE.bus_snoop_disable** = 1'b1, Bus Snooper is reset. Held status is cleared. (Only internal flag is cleared.)

Table APP-759 Exclusive Access Register

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x0E013000	BUS_SNOOP_DISABLE	bus_snoop_disable	RW	[0]	1	Exclusive Load/Store Disable register 1: Disable 0: Enable

3.13.4.15.1 Monitoring Exclusive Accesses to SRAM

The following shows the features of monitoring exclusive accesses to SRAM.

- In the case that there is an exclusive read (ExR), the address will be snooped.
- Only first address per APP SRAM tile can be snooped. Until the snooping of the first address is released, the second and subsequent exclusive reads (ExRs) are ignored. In addition, only one master can obtain the exclusive access right.
- The target address of monitoring must be Word address. When monitoring an exclusive access, the data monitor size is word even if the data access size is any of byte, halfword, or word.

- In the case that “failure” has been returned as a result of exclusive access, write to the slave has not been performed.

Success case of exclusive access

- The snooping is released after an exclusive write (ExW) is issued from the master obtaining exclusive access right to the target address to snoop. At this time, if exclusion process to the target address to snoop has been successful, “success” will be returned. (refer to Figure APP-111)
- An exclusive read access always receives “success” response. That is, “success” is returned even during one exclusive read access’s snooping, another exclusive read access has occurred. After the other exclusive read access’s occurrence, “success” is returned to the exclusive write access to the target address to snoop, issued from the master obtaining exclusive access right. (refer to Figure APP-112)

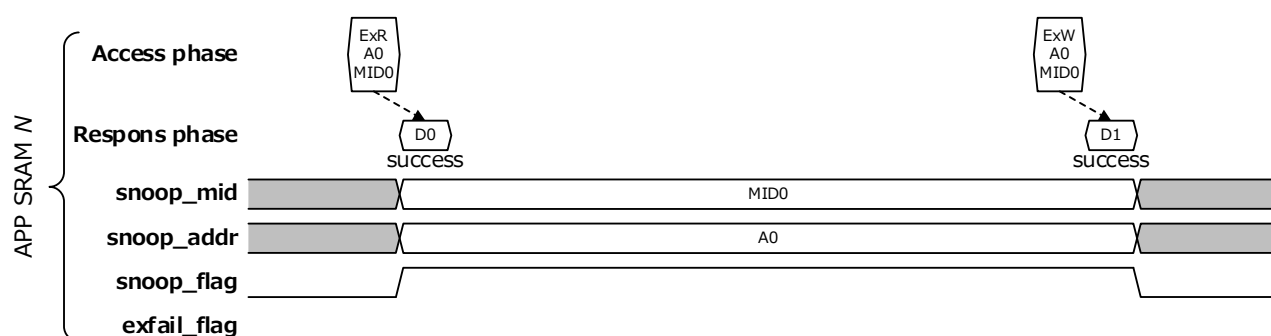


Figure APP-111 Success Case 1 of Exclusive Access

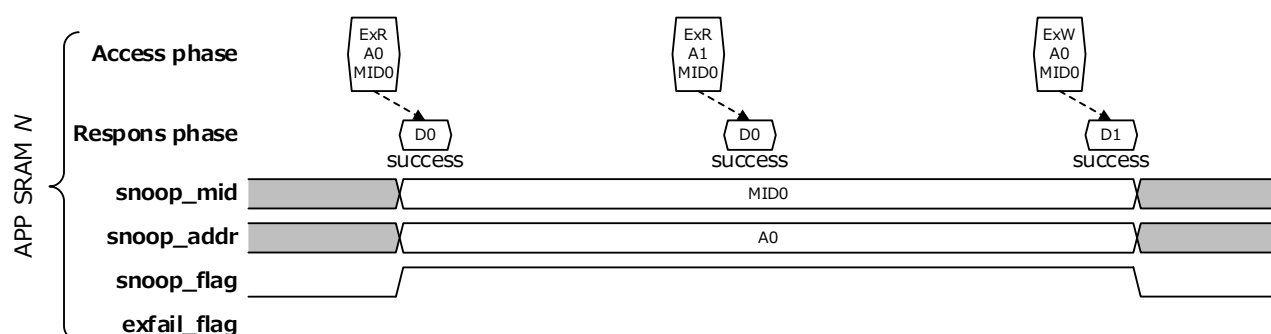


Figure APP-112 Success Case 2 of Exclusive Access

Failure case of exclusive access

- In the case that a usual write access (not an exclusive write access) occurs to a target address to snoop, exclusive access processing is failed and the exclusive write access is blocked.
“Failure” will be returned at the timing of an exclusive write access from the master with the exclusive access right. (refer to Figure APP-113)
- In the case that an exclusive write access (ExW) occurs from the master without the exclusive access right to

a target address, “failure” will be returned. (refer to Figure APP-114)

- In the case that an exclusive write access (ExW) occurs to an address that is not a target to snoop, “failure” will be returned at the timing of an exclusive write access from the master with the exclusive access right. (refer to Figure APP-115)
- For all failure cases, write to the slave is not performed.

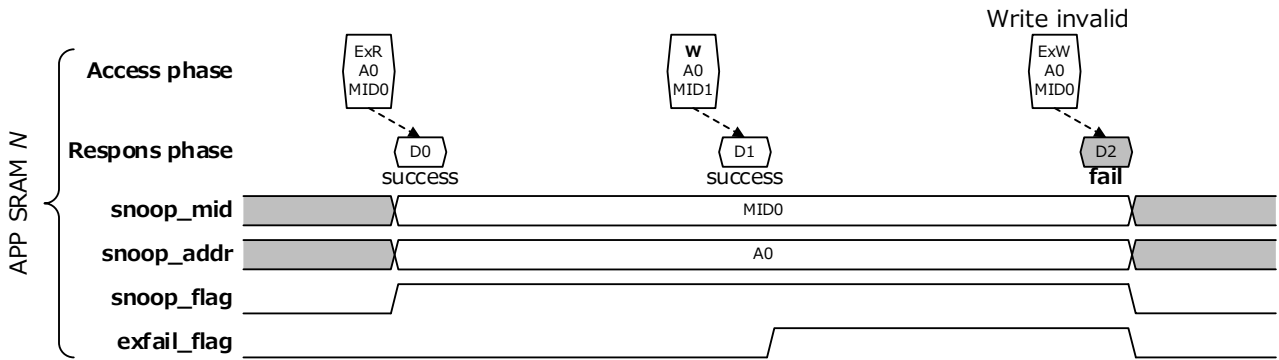


Figure APP-113 Failure Case 1 of Exclusive Access

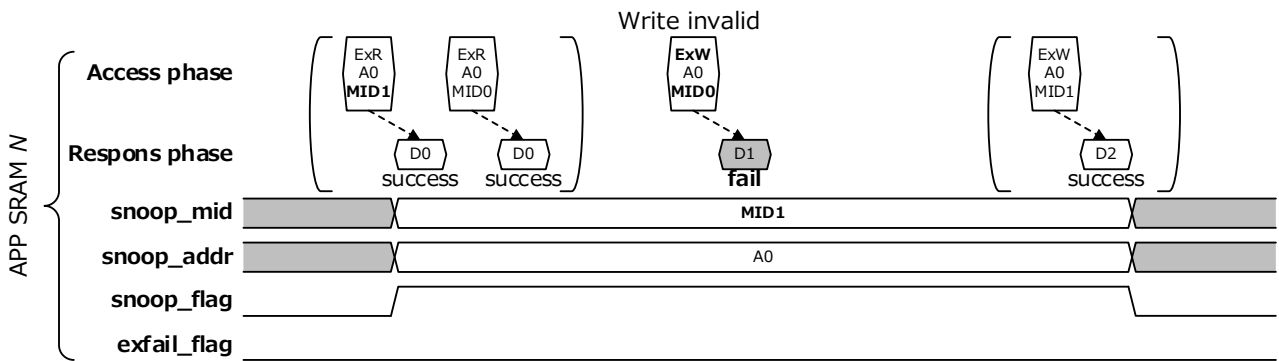


Figure APP-114 Failure Case 2 of Exclusive Access

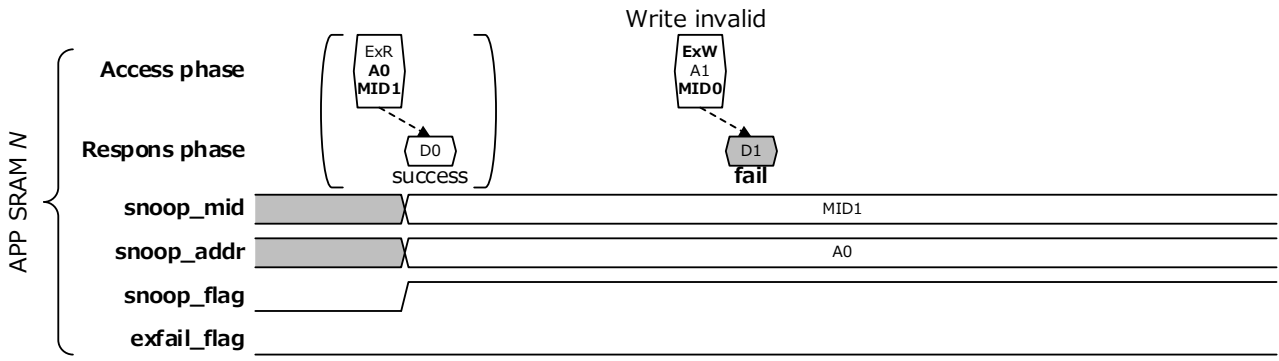


Figure APP-115 Failure Case 3 of Exclusive Access

3.13.4.15.2 Monitoring Exclusive Accesses to APP SUB Bus

The following shows the features of monitoring of exclusive accesses to APP SUB Bus.

- “Failure” will be returned to the exclusive write (ExW). However, in the case that **BUS_SNOOP_DISABLE.bus_snoop_disable=1'b1**, “success” will be returned. Even if for failure cases, write to the slave is performed.
- “
Success” will be returned to the exclusive read (ExR).

3.13.4.16 Start and Stop Sequence of ADSP

This section explains power supply, clock, and ADSP's recommended start and stop sequence including reset control.

Precaution:

Cortex[®]-M4 processor with FPU has multiple clocks and resets. In this section, when without specific description hereinafter, "clock" and "reset" means clock and reset of Cortex[®]-M4 processor with FPU core. Read-modify-write operation to registers is needed so that bits other than designated bits of the write register will not be changed.

Perform ADSP's start control in the following order.

step1	Turn ON the power domain PWD_APP or supply clocks if required.	For power supply control, refer to the PMU chapter.
step2	Turn ON the power domain PWD_APP if required.	Refer to 3.13.4.16.2 section.
step3	Start the ADSP.	Refer to 3.13.4.16.3 section.

Perform the ADSP's stop control in the following order.

step1	Stop the ADSP.	Refer to 3.13.4.16.6 section.
step2	Turn OFF the power domain PWD_APP_DSP if required.	Refer to 3.13.4.16.7 section.
step3	Stop the clock, turn OFF the power domain PWD_APP if required.	For power supply control, refer to the PMU chapter 3.4.

3.13.4.16.1 Start of Clock Supply for APP

Control the clock supply using System and I/O Processor.

- Precondition
The power supply of the power domain PWD_APP must be ON. (For power supply control, refer to the PMU chapter 3.4.)
- 1. Clock supply setting for APP
Control clock division ratio and clock source using the API.
- 2. Start of clock supply
APP_CKEN.APP=1 (CK_APP supply starts)
APP_CKEN.AHB=1 (CK_APP_AHB supply starts)
APP_CKEN.MCLK=1 (CK_APP_MCLK supply starts (only when AUDIO is used))

3.13.4.16.2 Power Supply ON for PWD_APP_DSP

For power supply control, refer to the PMU chapter 3.4.

3.13.4.16.3 ADSP Startup

Control the ADSP startup using System and I/O Processor or ADSP other than the target ADSP.

Note: about <N>

E.g., ADSP0 means that N = 0, ADSP1 means that N = 1, in the same way, ADSP5 means that N = 5.

- Precondition
The power supply of the power domain PWD_APP and PWD_APP_DSP must be ON. (For power supply control, refer to the PMU chapter 3.4.)
- 1. Clock division ratio setting
GEAR_AHB.gear_m_ahb= arbitrary (division ratio denominator write)
GEAR_AHB.gear_n_ahb= arbitrary (division ratio numerator write)
- 2. Clock supply (Initialization of internal circuit)
CK_GATE_AHB.ck_gate_dsp<N>=1
- 3. Clock stop
CK_GATE_AHB.ck_gate_dsp<N>=0
- 4. ADSP start preparation
Transfer the program codes to the APP SRAM, and do the address converter setting.
(For address converter, refer to 3.13.4.13 section.)
- 5. Reset release
RESET.xrs_dsp<N>=1
- 6. Clock supply
CK_GATE_AHB.ck_gate_dsp<N>=1

3.13.4.16.4 Clock Frequency Change

1. Clock division ratio setting
GEAR_AHB.gear_m_ahb= (division ratio denominator)
GEAR_AHB.gear_n_ahb= (division ratio numerator)

3.13.4.16.5 Reset Assert and Release

Control Reset Enable and Release using System and I/O Processor or ADSP other than the target ADSP processor.

Note: about <N>

E.g., ADSP0 means that N = 0, ADSP1 means that N = 1, in the same way, ADSP5 means that N = 5.

- Precondition
The ADSP must be in SLEEPING state so that uncompleted accesses will not remain in buses. (Refer to the PMU chapter 3.4 and 3.13.4.9 section.)
- 1. Reset assert
RESET.xrs_dsp<N>=0
- 2. Clock stop
CK_GATE_AHB.ck_gate_dsp<N>=0
- 3. Reset release
RESET.xrs_dsp<N>=1
- 4. Clock supply
CK_GATE_AHB.ck_gate_dsp<N>=1

3.13.4.16.6 ADSP Stop

Control ADSP stop using System and I/O Processor or ADSP other than the target ADSP.

Note: about <N>

E.g., ADSP0 means that N = 0, ADSP1 means that N = 1, in the same way, ADSP5 means that N = 5.

Precondition

The ADSP must be in SLEEPING state so that uncompleted accesses will not remain in buses. (Refer to the PMU chapter 3.4 and 3.13.4.9 section.)

1. Reset assert
RESET.xrs_dsp<N>=0
2. Clock stop
CK_GATE_AHB.ck_gate_dsp<N>=0

3.13.4.16.7 PWD_APP_DSP Power Supply OFF

For power supply control, refer to the PMU chapter 3.4.

3.14 SYSIOP Clock and Reset Control

3.14.1 Function Overview

The System and IOP Domain (referred to as “SYSIOP” hereinafter) is responsible for overall system control. Centered around the Arm® Cortex®-M0+, it equips IO Configuration, DMAC, RTC, a common communication I/F that supports I2C/SPI/UART, and the HOSTIFC, etc. for communication with the external host. These are connected together via the SYSTEM Bus.

The performance such as the transfer rate depends on the combination of the X'tal Oscillator clock frequency and voltage mode (High Performance mode/Low Power mode). The following describes a function overview using the X'tal Oscillator clock frequency operating at 26 MHz as an example.

The SYSIOP offers the following functions.

System and I/O Processor

This is the processor block (referred to as “SYSCPU” hereinafter) that is centered around the Arm® Cortex®-M0+. The following functions are equipped.

- Arm® Cortex®-M0+
- The communication unit that performs communication between the Application Processor and CPU, and between the GNSS DSP and CPU
- Interrupt input register
- Timer
 - AMBA® Design Kit (ADK) SP804
 - Two channel support
 - One Timer module for each processor (Total: Six Timers)
- Watchdog Timer
 - AMBA® Design Kit (ADK) SP805
 - One channel for each processor (Total: Six Watchdog Timers)

System and I/O Processor Memory

- 256 KByte SRAM
- operating frequency
 - High Performance mode: Up to 97.5 MHz
 - Low Power mode: Up to 32.5 MHz

SYSTEM Bus

A 32 bit multi-layer AHB bus matrix. Connects the blocks within the SYSIOP to each other and other Domains.

Equips an HW protection function that uses a master ID, and an access detection (error response) function to the power supply OFF area.

I/O Configuration

An I/O terminal control function. For details, refer to Section 3.1.

GPIO

Performs GPIO control of pins and selection/detection control of pins used for interrupts. The following functions are equipped.

- GPIO control
- Pin selection
- External interrupt selection
- Event detection control

For details, refer to Section 3.2.

DMAC

Equips the four following DMACs that are used according to the application.

- SYDMAC: memory to memory transfer and Crypto-engine
- SYSUBDMAC: Crypto-engine, SPI-FLASH Interface and Configurable I/O
- SDMAC: Sensor Engine
- HDMAC: Host Interface

RTC

The timer block that counts the time using the RTC clock. For details, see Section 3.6.

COMMIF

Has each of the interface circuits of the I2C/SPI/UART.

- I2C Interface for Configurable I/O
 - Communication speeds
 - High Performance mode: up to 400 Kbit/s
 - Low Power mode: up to 400 Kbit/s
- SPI Interface for Configurable I/O
 - Arm® PrimeCell® Synchronous Serial Port (PL022)
 - Communication speeds
 - High Performance mode: up to 9.750 Mbit/s
 - Low Power mode: up to 7.8 Mbit/s
- UART interfaces for Configurable I/O
 - PrimeCell® UART (PL011)
 - Communication speeds

- High Performance mode: up to 3 Mbit/s
- Low Power mode: up to 2 Mbit/s

SPI Flash Controller

The main memory interface that supports the Quad SPI FLASH. For details, refer to Section 3.10.

HOSTIFC

The I/F block for communication with the CXD5602's external host. In addition to supporting the I2C/UART/SPI communication I/F, sequential control is also possible for reduced power consumption. For details, refer to Section 0.

Debugger I/F

A debugger interface circuit. It has a user authentication function that uses a debug path.

3.14.2 Power Supply Control

The SYSIOP block is divided into the three power domains of PWD_CORE, PWD_SYSIOP, and PWD_SYSIOP_SUB. The power supply domains that correspond to each function block of the SYSIOP are as follows:

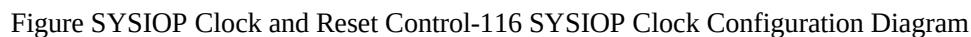
- PWD_CORE
 - 256 KByte SRAM in System Control and I/O Processor Memory
- PWD_SYSIOP
 - System and I/O Processor
 - DMAC (SYDMAC, HDMAC, SDMAC)
 - HOSTIFC
 - Debugger I/F
 - FREQDISC
 - RTC
- PWD_SYSIOP_SUB
 - COMMIF Block
 - SPI-FLASH Interface
 - 128 KByte ROM in System Control and I/O Processor Memory
 - Crypto Engine in System Control and I/O Domain
 - SYSUBDMAC

3.14.3 Clock and Reset Control

Using clock control, clock switching, frequency control by frequency division switching, and clock supply/stop can be performed. Using reset control, reset assert/release of each block can be performed. The API is used for the control.

3.14.3.1 SYSIOP Clock Configuration Diagram

Figure SYSIOP Clock and Reset Control-116 shows the SYSIOP clock configuration diagram. Within the figure, the SEL(number), DIV(number), and CG(SYS/SUB number) are linked to the numbers within Table SYSIOP Clock and Reset Control-802, Table SYSIOP Clock and Reset Control-807, and Table SYSIOP Clock and Reset Control-808. For areas where the register names are directly indicated in the figure, refer to the descriptions in each corresponding Section.



The following tables describe the maximum operating frequencies of the System and I/O Processor and the SYSTEM Bus – the main function blocks of the SYSIOP. Each has a different maximum operating frequency depending on the supported XOSC frequency and the SYSPLL oscillating frequency. The SYS SRAM within the SYSIOP has the same operating frequency as the System and I/O Processor. The element circuits (BackUp SRAM, DMAC, Crypto...) directly connected to the SYSTEM Bus or via a synchronous bridge basically have the same maximum frequencies as the SYSTEM Bus.

Table SYSIOP Clock and Reset Control-760 XOSC (26 MHz), High Performance Mode

—936/1010—

Table SYSIOP Clock and Reset Control-761 XOSC (26 MHz), Low Power Mode

Clock source		SYSPLL		XOSC	RCOSC	RTC
frequency	MHz	195.000	156.000	26.000	8.192	0.032768
System and I/O Processor	MHz	32.500	31.200	26.000	8.192	0.032768
System Bus	MHz	32.500	31.200	26.000	8.192	0.032768

3.14.3.3 Clock Switching Confirmation

3.14.3.3.1 Function Details

The clock source of the clock supplied to each block can be changed using the API. The selected clock can be confirmed by reading the register.

3.14.3.3.2 Register Descriptions

Table SYSIOP Clock and Reset Control-802 shows the clock switching status registers. Make sure to use RW registers as RO registers.

Table SYSIOP Clock and Reset Control-762 Clock Switching Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041004CC	CKSEL_SYSIOP	Reserved	RO	[31:22]	0	Reserved
		SEL_FD_PLL	RW	[21:20]	2'b00	Indicated as SEL(5) in Figure SYSIOP Clock and Reset Control-116 FREQDISC clock source switching 2'b00: SYSPLL clock not divided 2'b01: SYSPLL clock divided by 2 2'b10: SYSPLL clock divided by 4 2'b11: SYSPLL clock divided by 4
		Reserved	RO	[19:18]	0	Reserved
		SEL_FREQDIS	RW	[17:16]	2'b00	Indicated as SEL(4) in Figure SYSIOP Clock and Reset Control-116 FREQDISC clock source switching 2'b00: RCOSC 2'b01: XOSC 2'b10: The frequency divided clock selected by CKSEL_SYSIOP.SEL_FD_PLL 2'b11: Prohibited setting
		Reserved	RO	[15:14]	0	Reserved
		SEL_I2CS	RW	[13:12]	2'b00	Indicated as SEL(3) in Figure SYSIOP Clock and Reset Control-116 I2C3 clock source switching 2'b00: The clock selected by CKSEL_SYSIOP.SEL_HOST2 2'b01: The frequency divided clock selected by CKSEL_SCU.SEL_SCU_XTAL 2'b10: SYSPLL 2'b11: Prohibited setting
		Reserved	RO	[11:9]	0	Reserved

		SEL_UART0	RW	[8]	0	Indicated as SEL(2) in Figure SYSIOP Clock and Reset Control-116 UART0 clock source switching 0: The clock selected by CKSEL_SYSIOP.SEL_HOST2 1: Reserved
		Reserved	RO	[7:3]	0	Reserved
		SEL_HOST2	RW	[2]	0	Indicated as SEL(1) in Figure SYSIOP Clock and Reset Control-116 HOSTIFC clock source switching 0: The clock selected by CKSEL_SYSIOP.SEL_HOST 1: XOSC
		SEL_HOST	RW	[1:0]	2'b00	Indicated as SEL(0) in Figure SYSIOP Clock and Reset Control-116 HOSTIFC clock source switching 2'b00: RCOSC 2'b01: RCRTC (RCOSC frequency divided by 250) 2'b10: The clock selected by CKSEL_ROOT.SEL_RF_PLL_1_DIV 2'b11: RTC Clock
0x041004D0	CKSEL_SYSIOP_SUB	Reserved	RO	[31:1]	0	Reserved
		SEL_UART1	RW	[0]	0	Indicated as SEL(6) in Figure SYSIOP Clock and Reset Control-116 UART1 clock source switching 1: Reserved 0: The clock selected by CKDIV_COM.CK_COM

3.14.3.4 Clock Frequency Division Switching Confirmation

3.14.3.4.1 Function Details

Using the API, the frequency division ratio of the target clock can be changed. You can confirm the currently selected frequency division ratio from the register.

Clock Frequency Division for the System and I/O Processor, AHB, and APB

The clock (ck_cpu_bus_gear_1) for the System and I/O Processor, the AHB clock (ck_ahb_gear), and the APB clock (ck_apb_gear) are frequency divided clocks of the ck_cpu_bus. The frequency division of the ck_cpu_bus is described by the following equations.

Frequency division of ck_cpu_bus

- ck_cpu_bus_gear_1= frequency division (A)
- ck_ahb_gear = frequency division (A) x frequency division (B)
- ck_apb_gear = frequency division (A) x frequency division (B) x frequency division (C)

Note:

Refer to Table SYSIOP Clock and Reset Control-803 for frequency division (A), Table SYSIOP Clock and Reset Control-804 for frequency division (B), and Table SYSIOP Clock and Reset Control-805 for frequency division (C).

Table SYSIOP Clock and Reset Control-763 System and I/O Processor Frequency Division Setting

CKDIV_CPU_DSP_BUS.CK_M0	Frequency Division(A)
0	1
1	2
2	3
3	4
...	Register value + 1
28	29
29	30
30	31
31	32

Table SYSIOP Clock and Reset Control-764 AHB Clock Frequency Division Setting

CKDIV_CPU_DSP_BUS.CK_AHB	Frequency Division(B)
0	1
1	2
2	4
3	8
4	16
5	Prohibited setting
6	
7	

Table SYSIOP Clock and Reset Control-765 APB Clock Frequency Division Setting

CKDIV_CPU_DSP_BUS.CK_APB	Frequency Division(C)
0	1
1	2
2	4

3	8

Clock Frequency Division for SPI Flash Controller

The frequency of the clock for the SPI Flash Controller is determined by the `ck_cpu_bus` frequency and the register setting value. The following equations show the frequency division of the clock for the SPI Flash Controller.

- Frequency division of the clock for the SPI Flash Controller based on the `ck_cpu_bus`
 - `ck_sfc_sfclk_gear` = frequency division(D)
 - `ck_sfc_hclk_low_gear` = frequency division(D) x 2

Note:

Refer to Table SYSIOP Clock and Reset Control-806 for the frequency division(D).

Table SYSIOP Clock and Reset Control-766 Frequency Division Setting of Clock for the SPI Flash Controller

CKDIV_CPU_DSP_BUS.SFC_HCLK_LOW	Frequency Division(D)
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	16
11	32
12	64
13	128
14	256
15	512

Caution upon Setting the Frequency Division

When the SPI Flash Controller is not used, set `CKDIV_CPU_DSP_BUS.SFC_HCLK_LOW` to “0”.

3.14.3.4.2 Register Descriptions

Table SYSIOP Clock and Reset Control-807 shows the frequency division setting status registers of each clock. Make sure to use the RW registers as RO registers.

Table SYSIOP Clock and Reset Control-767 Frequency Division Setting Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x041004D8	CKDIV_CPU_DSP_BUS	SFC_HCLK_LOW	RW	[31:28]	0	Indicated as DIV(3) in Figure SYSIOP Clock and Reset Control-116 Frequency division setting (ratio against System and I/O Processor clock) of ck_sfc_sfclk_gear 0: divided by 1 1: divided by 2 2: divided by 3 3: divided by 4 4: divided by 5 5: divided by 6 6: divided by 7 7: divided by 8 8: divided by 9 9: divided by 10 10: divided by 16 11: divided by 32 12: divided by 64 13: divided by 128 14: divided by 256 15: divided by 512 CK_SFC_HCLK_LOW is always the CK_SFC_SFCLK frequency divided by 2. E.g. 0: CK_SFC_SFCLK (divided by 1) CK_SFC_HCLK_LOW(divided by 2) 3 : CK_SFC_SFCLK(divided by 4) CK_SFC_HCLK_LOW(divided by 8)
		Reserved	RO	[27:26]	0	Reserved

		CK_APB	RW	[25:24]	2'b00	Indicated as DIV(2) in Figure SYSIOP Clock and Reset Control-116 Frequency division setting (ratio against AHB clock) of APB clock 0: divided by 1 1: divided by 2 2: divided by 4 4: divided by 8
		Reserved	RO	[23:19]	0	Reserved
		CK_AHB	RW	[18:16]	0	Indicated as DIV(1) in Figure SYSIOP Clock and Reset Control-116 Frequency division setting (ratio against CPU clock) of AHB clock 0: divided by 1 1: divided by 2 2: divided by 4 3: divided by 8 4: divided by 6 5, 6, 7: Prohibited settings
		Reserved	RO	[15:5]	0	Reserved
		CK_M0	RW	[4:0]	0	Indicated as DIV(0) in Figure SYSIOP Clock and Reset Control-116 Frequency division setting (ratio against ck_cpu_bus) of System and I/O Processor 0: divided by 1 1: divided by 2 ... 30: divided by 31 31: divided by 32
0x041004DC	CKDIV_COM	Reserved	RO	[31:5]	0	Reserved

		CK_COM	RW	[4:0]	0	Indicated as DIV(4) in Figure SYSIOP Clock and Reset Control-116 Frequency division setting (ratio against ck_cpu_bus) of SYSIOP_SUB communication system 0: divided by 1 1: divided by 2 2: divided by 3 ... 29: divided by 30 30: divided by 31 31: divided by 32
0x041004E0	CKDIV_HOS TIFC	Reserved	RO	[31:5]	0	Reserved
		CK_HOS TIFC	RW	[4:0]	0	Indicated as DIV(5) in Figure SYSIOP Clock and Reset Control-116 HOSTIFC frequency switching setting 0: divided by 1 1: divided by 2 ... 30: divided by 31 31: divided by 32
0x04100518	GEAR_STAT	Reserved	RO	[31:3]	0	Reserved
		SFC_STA T	RO	[2]	0	Indicated as DIV(3) in Figure SYSIOP Clock and Reset Control-116 Update status of CKDIV_CPU_DSP_BUS.SFC_HCLK_LOW setting value 0: Update completed 1: Update in progress
		AHB_STA T	RO	[1]	0	Indicated as DIV(1) in Figure SYSIOP Clock and Reset Control-116 Update status of CKDIV_CPU_DSP_BUS.CK_AHB setting value 0: Update completed 1: Update in progress

		CPU_ST AT	RO	[0]	0	Indicated as DIV(0) in Figure SYSIOP Clock and Reset Control-116 Update status of CKDIV_CPU_DSP_BUS.CK_M0 setting value 0: Update completed 1: Update in progress

3.14.3.5 Clock Enable Confirmation

3.14.3.5.1 Function Details

Using the API, supply/stop control of the clocks supplied to each block can be performed.

3.14.3.5.2 Register Descriptions

Table SYSIOP Clock and Reset Control-808 shows the clock enable status registers. Make sure to use the RW registers as RO registers.

Table SYSIOP Clock and Reset Control-768 Clock Enable Status Registers

Address	Register Name	Bit Field Name	Type	Bit	Initial Value	Description
0x04100714	SYSIOP_CKEN	Reserved	RW	[31:18]	0	Reserved
		HOSSPI	RW	[17]	0	Indicated as CG(SYS17) in Figure SYSIOP Clock and Reset Control-116 Clock enable for SPI2
		HOSI2C	RW	[16]	0	Indicated as CG(SYS16) in Figure SYSIOP Clock and Reset Control-116 Clock enable for I2C3
		HOSTIFC_SEQ	RW	[15]	0	Indicated as CG(SYS15) in Figure SYSIOP Clock and Reset Control-116 Clock enable for HOSTIFC processor
		BRG_SCU	RW	[14]	0	Indicated as CG(SYS14) in Figure SYSIOP Clock and Reset Control-116 Clock enable for AHB-APB bridge between PWD_SYSIOP and PWD_SCU
		SYSIOP_RTC	RW	[13]	1	Indicated as CG(SYS13) in Figure SYSIOP Clock and Reset Control-116 Clock enable for RTC1 and APB
		RCOSC_OUT	RW	[12]	0	Indicated as CG(SYS12) in Figure SYSIOP Clock and Reset Control-116 Clock enable for reference clock (RCOSC) of FREQDISC

		AP_CLK	RW	[11]	0	Indicated as CG(SYS11) in Figure SYSIOP Clock and Reset Control-116 Clock enable for reference clock (AP_CLK) of FREQDISC
		RTC_ORG	RW	[10]	0	Indicated as CG(SYS10) in Figure SYSIOP Clock and Reset Control-116 Clock enable for reference clock (RTC Clock) of FREQDISC
		FREQDIS	RW	[9]	0	Indicated as CG(SYS09) in Figure SYSIOP Clock and Reset Control-116 Clock enable for measurement target clock of FREQDISC
		APB	RW	[8]	1	Indicated as CG(SYS08) in Figure SYSIOP Clock and Reset Control-116 Clock enable for the APB within PWD_SYSIOP
		AHB_DMAC2	RW	[7]	0	Indicated as CG(SYS07) in Figure SYSIOP Clock and Reset Control-116 Clock enable for SYDMAC
		AHB_DMAC1	RW	[6]	0	Indicated as CG(SYS06) in Figure SYSIOP Clock and Reset Control-116 Clock enable for HDMAC
		AHB_DMAC0	RW	[5]	0	Indicated as CG(SYS05) in Figure SYSIOP Clock and Reset Control-116 Clock enable for SDMAC
		BRG_HOST	RW	[4]	0	Indicated as CG(SYS04) in Figure SYSIOP Clock and Reset Control-116 Clock enable for the AHBAPB bridge that connects the MainAHB Bus and APB module of the HOSTIF

		I2CS	RW	[3]	0	Indicated as CG(SYS03) in Figure SYSIOP Clock and Reset Control-116 Clock enable for HOSTIFC I2C3 communication
		PCLK_HOSTIFC	RW	[2]	0	Indicated as CG(SYS02) in Figure SYSIOP Clock and Reset Control-116 Clock enable for the APB of SPI2 and I2C3
		PCLK_UART0	RW	[1]	0	Indicated as CG(SYS01) in Figure SYSIOP Clock and Reset Control-116 UART0 APB clock enable
		UART0	RW	[0]	0	Indicated as CG(SYS00) in Figure SYSIOP Clock and Reset Control-116 UART0 communication clock enable
0x04103420	SYSIOP_SUB_C KEN	Reserved	RO	[31:17]	0	Reserved
		COM_UART_PCLK	RW	[16]	0	Indicated as CG(SUB10) in Figure SYSIOP Clock and Reset Control-116 Clock enable for APB of UART1
		Reserved	RO	[15:10]	0	Reserved
		SFC_HCLK_LOW	RW	[9]	1	Indicated as CG(SUB09) in Figure SYSIOP Clock and Reset Control-116 Clock enable for AHB of SPI Flash Controller
		SFC_SFCLK	RW	[8]	1	Indicated as CG(SUB08) in Figure SYSIOP Clock and Reset Control-116 Clock enable for clock generation of SPI Flash Controller

		SFC_HCLK	RW	[7]	1	Indicated as CG(SUB07) in Figure SYSIOP Clock and Reset Control-116 Clock enable for AHB synchronous bridge between SYSTEM Bus and SPI Flash Controller
		Reserved	RW	[6]	0	Reserved
		I2CM_SUB	RW	[5]	0	Indicated as CG(SUB05) in Figure SYSIOP Clock and Reset Control-116 Clock enable for I2C2
		SPIM	RW	[4]	0	Indicated as CG(SUB04) in Figure SYSIOP Clock and Reset Control-116 Clock enable for SPI0
		UART1	RW	[3]	0	Indicated as CG(SUB03) in Figure SYSIOP Clock and Reset Control-116 Clock enable for UART1
		AHB_DMAC3	RW	[2]	0	Indicated as CG(SUB02) in Figure SYSIOP Clock and Reset Control-116 Clock enable for SYSUBDMAC
		COM_BRG	RW	[1]	0	Indicated as CG(SUB01) in Figure SYSIOP Clock and Reset Control-116 Clock enable for AHB asynchronous bridge master of I2C2, UART1, and SPI0
		AHB_BRG_COM IF	RW	[0]	0	Indicated as CG(SUB00) in Figure SYSIOP Clock and Reset Control-116 Clock enable for AHB asynchronous bridge slave of I2C2, UART1, and SPI0

3.14.3.6 Reset and Control

3.14.3.6.1 SYSIOP Reset Configuration Diagram

Figure SYSIOP Clock and Reset Control-117 SYSIOP Reset Configuration Diagram shows the reset configuration diagram of SYSIOP.

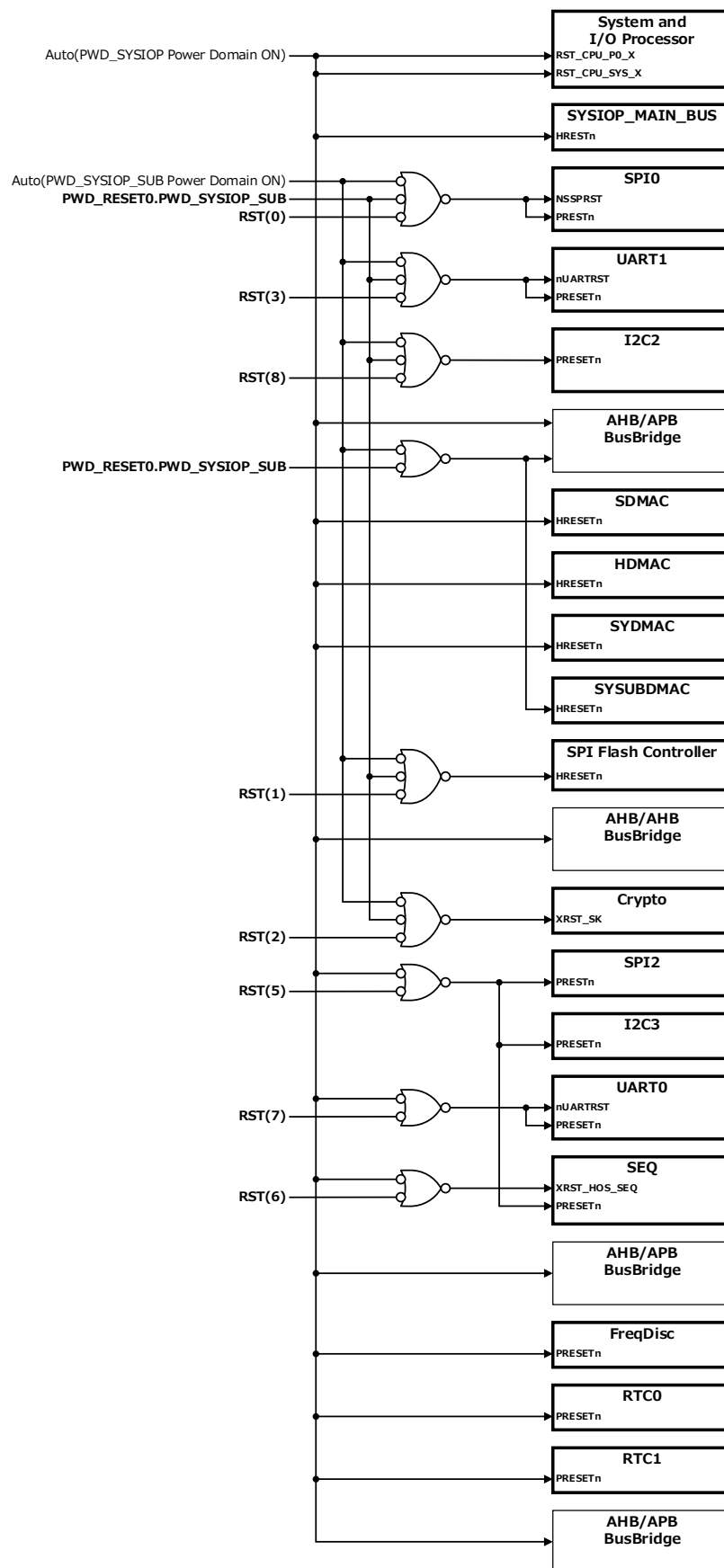


Figure SYSIOP Clock and Reset Control-117 SYSIOP Reset Configuration Diagram

3.14.3.6.2 Register Descriptions

The reset of each block can be controlled using the registers. Since the control flow varies according to the function block, refer to each block's Section. Table SYSIOP Clock and Reset Control-809 shows the reset control registers.

Table SYSIOP Clock and Reset Control-769 Reset Control Registers

Address	Register	Bit Field Name	Type	Bit	Initial Value	Description
0x04100700	SWRESET_BUS	Reserved	RO	[31:17]	0	Reserved
		XRST_PMU_I2CM	RW	[16]	1	Indicated as RST(9) in Figure SYSIOP Clock and Reset Control-117 Reset for I2C4 0 Reset is performed 1: Reset release
		Reserved	RO	[15:12]	0	Reserved
		XRST_I2CM_SUB	RW	[11]	0	Indicated as RST(8) in Figure SYSIOP Clock and Reset Control-117 Reset for I2C2
		XRST_UART0	RW	[10]	0	Indicated as RST(7) in Figure SYSIOP Clock and Reset Control-117 Reset for UART0
		XRST_HOSTIFC_ISOP	RW	[9]	0	Indicated as RST(6) in Figure SYSIOP Clock and Reset Control-117 Reset for HOSTIFC Sequencer
		XRST_HOSTIFC	RW	[8]	0	Indicated as RST(5) in Figure SYSIOP Clock and Reset Control-117 Reset for HOSTIFC
		Reserved	RO	[7:6]	0	Reserved
		XRST_UART1	RW	[5]	0	Indicated as RST(3) in Figure SYSIOP Clock and Reset Control-117 Reset for UART1
		Reserved	RO	[4:3]	0	Reserved
		XRST_SAKE	RW	[2]	0	Indicated as RST(2) in Figure SYSIOP Clock and Reset Control-117 Reset for Crypto(Clelia)

		XRST_SFC	RW	[1]	1	Indicated as RST(1) in Figure SYSIOP Clock and Reset Control-117 Reset for SPI Flash Controller
		XRST_SPIM	RW	[0]	0	Indicated as RST(0) in Figure SYSIOP Clock and Reset Control-117 Reset for SPI0

3.15 Audio Codec

The Audio Codec, when combined with the CXD5247, realizes Audio Codec functions.

The following is an overview of its functions.

- I2S Bus Interface supports:
 - Two I2S-bus for audio-codec interface with DMA-based operation
 - 16/24-bit per channel data transfers
 - I2S, Left-justified data format
 - Various bit clock frequency and codec clock frequency support
 - ✧ Master clock:
 - High performance mode: 256fs, 128fs, 64fs of bit clock frequency
 - Low power mode: 128fs, 64fs of bit clock frequency
 - ✧ Slave clock:
 - High performance mode: 256fs, 128fs, 64fs of bit clock frequency
 - Low power mode: 128fs, 64fs of bit clock frequency
 - ✧ Sampling rate
 - High performance mode
 - Master mode : 192kHz, 96kHz, 48kHz
 - Slave mode: 192kHz, 96kHz, 48kHz, 44.1kHz, 16kHz, 8kHz
 - Low power mode
 - Master mode : 96kHz, 48kHz
 - Slave mode: 96kHz, 48kHz, 44.1kHz, 16kHz, 8kHz
 - ✧ 2ch channels each I2S interface
 - Unique Audio Data Format (Pulse Density Modulation) between CXD5602GG and CXD5247GF

3.16 SDIO

- SD Host Controller Interface
 - SD Memory Card Protocol version 3.0 compatible
 - 8K-Byte(32bit x 512word) x2 FIFOs for Tx/Rx
 - Communication speeds
 - ✧ High Performance mode: up to 39.000MHz
 - ✧ Low Power mode: up to 24.552MHz

3.17 eMMC

- eMMC Interface
 - eMMC 4.41 Protocol compatible
 - ✧ only SDR mode
 - 1K-Byte(32bit x 256word) x2 FIFOs for Tx/Rx
 - Communication speeds
 - ✧ High Performance mode: up to 39.000MHz
 - ✧ Low Power mode: up to 24.552MHz

3.18 USB

- USB 2.0 Device
 - Complies with USB2.0 Specification High-speed up to 480 Mbps
 - ✧ Not supported at Low Power mode
 - On-chip USB PHY transceiver
 - Supports MSC, MTP, CDC, PTP, ACM and HID class
 - Multi-function
 - ✧ Interface: #0/#1/#2

3.19 CIS I/F

- 8-bit parallel Camera Interface input
 - 8-bit ITU-R BT 601 / 656 Mode
 - Compressed data like JPEG support
 - Supports Y/C, JPEG and JPEG+Y/C Interleave formats
 - Programmable polarity of video sync signal
 - Capture frame control support
 - Input image size
 - ✧ JPEG Only: up to 5M pixels
 - ✧ Y/C Only: up to 480x360
 - ✧ JPEG+Y/C: 2M + WQVGA (JPEG High Quality mode)
5M + WQVGA (JPEG Normal Quality mode)
 - Parallel Input rate: up to 54MHz

3.20 2D Graphics

- 2D Graphics accelerator
 - Bit Block Transfer
 - Rotator
 - ✧ Supported image format: YCbCr422, RGB565
 - ✧ Supported rotate degree: 0, 90, 180, 270 degrees
 - ✧ Color space Conversion (YCbCr422<->RGB565)
 - 3-operand raster operation (ROP3)
 - Alpha blending
 - Scaling
 - ✧ Horizontal direction: x1/64 to x64, Vertical direction: x1/64 to x64
Maximum source input 2880x2160, maximum destination output 768x1024
 - ✧ YCbCr 422 16 bpp format

3.21 ADC

3.21.1 ADC Overview

Analog input function comprises the SCU_ADCIF module including a logic to control LPADC (4ch) and HPADC (2ch), and the SCU_ANALOG module including the ADC analog circuits and the peripheral circuits.

The ADCIF module distributes 10 bit A/D conversion data from the LPADC to four time-sharing lines and stores them in the FIFO. In the meantime, the ADCIF module applies a decimation filter comprising the third order CIC filter to two 10 bit A/D conversion data, which are from the individual two HPADCs separately. These data are stored in the FIFO as 16 bit data. Regarding conversion data from the HPADC, two data-writing modes can be selected. One is a mode called vector mode (dual axis) that packs two A/D conversion data, and then writes them in the FIFO. The other is a mode that writes two A/D conversion data in the FIFO separately. These FIFOs which are used only for the ADC in the ADCIF module are referred to as SCU_ADCIF_FIFOs in this manual. Four channels of 16 rows of SCU_ADCIF_FIFOs are prepared for the LPADC, and two channels of 32 rows are prepared for the HPADC. Each channel has an interface for DMA REQ/ACK signals to perform DMA processing, and for interrupt signals to perform Watermark Level detection.

Furthermore, the ADCIF module has a register block to control analog circuits, and the APB interface to exchange data with the CPU and the SCU internal sequencer.

For data storage at the SCU and the FIFO control inside the SCU, refer to Chapter of the SCU (3.9).

The ADCIF module has two ports for GNSS, one is 10 bit A/D conversion data, and the other is the enable signal, to directly output the values of a selected channel in the LPADC.

3.21.1.1 LPADC (Low Power ADC) Sampling Frequency

Table ADC-810 describes sampling frequencies supported by the LPADC. The maximum sampling rate is dependent on the number of active channels.

Table ADC-770 Sampling Rate Range Supported by the LPADC

Clock Source of CK_U32KL	Clock Frequency (Input to SCU)	Supported Sampling Rate Range vs number of active channels		
		1 channel	2 channels	4 channels
RCOSC	8.192 MHz	1 Hz to 32 kHz	1 Hz to 512 Hz	1 Hz to 256 Hz
RTC	32.768 kHz	1 Hz to 32 kHz	1 Hz to 512 Hz	1 Hz to 256 Hz

3.21.1.2 HPADC (High Performance ADC) Sampling Frequency

Table ADC-811 describes sampling frequencies supported by the HPADC

Table ADC-771 Sampling Rate Range Supported by the HPADC

Clock Source	Clock Frequency (Input to SCU)	Supported Sampling Rate Range	Over Sampling Frequency
RCOSC	8.192 MHz	16 kHz to 32 kHz	2.048 MHz
	1 Hz to 32.768 kHz	1 Hz to 32.768 kHz	None (actual rate conversion)
RTC	1 Hz to 32.768 kHz	1 Hz to 32.768 kHz	None (actual rate conversion)
XOSC	13 MHz	16.927 kHz to 33.854 kHz	2.167 MHz

3.21.2 ADC Block Diagram

Figure 3.26-1 describes the block diagram of the ADCIF module and around ADC macro circuits.

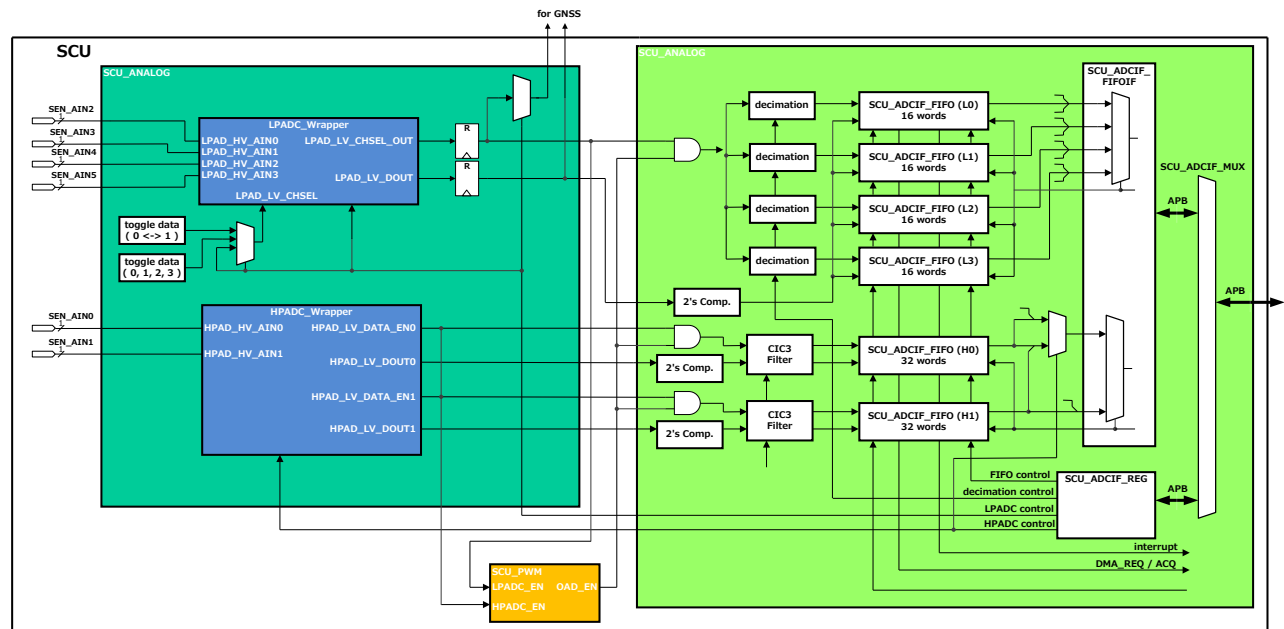


Figure ADC-118 Block Diagram ADCIF module and around ADC macro circuits

3.21.3 Memory Map

Figure ADC-119 describes a memory map inside the ADCIF.

For the memory map seen from the higher layers, refer to Chapter of the SCU (3.9).

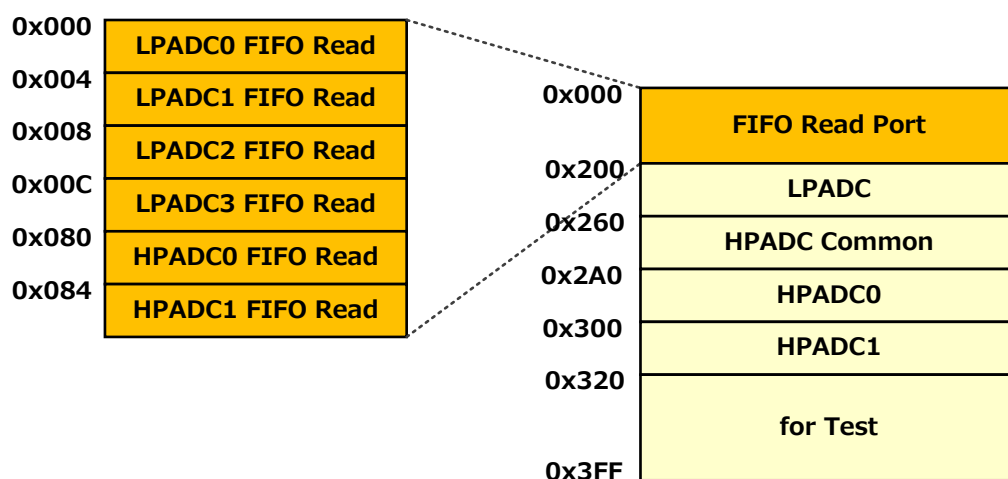


Figure ADC-119 Memory Map inside the ADCIF

3.21.4 Power Supply Control

The LPADC and the HPADC belong to power domain called PWD_SCU. Inside PWD_SCU, as lower level power supply domains, there are module areas for power supply control shown below. Power supply control registers for such areas are held in the TOPREG.

Table ADC-772 Power Supply Information

Target for Power Supply Control	Address Offset	Bit	Bit Name (TOPREG)	Description
LPADC	0x0004	[29]	WEN_LPADC	LPADC Power supply control Write Enable 0: Disable 1: Enable
		[13]	LPADC	LPADC Power supply control 0: OFF 1: ON
HPADC		[28]	WEN_HPADC	HPADC Power supply control Write Enable 0: Disable 1: Enable
		[12]	HPADC	HPADC Power supply control 0: OFF 1: ON

For control details, refer to Section of the SCU Control Sequence described in Chapter of the SCU (3.9).

3.21.5 Clock Control

3.21.5.1 Clock Summary

Table ADC-773 Clock Summary

Clock Name	Maximum Frequency (HV)	Maximum Frequency (LV)	Usage
CK_SCU_SCU	13 MHz	13 MHz	SCU Main ^(1*)
CK_SCU_SCU_SC	13 MHz	13 MHz	Controls SCU Main CPU only ^(1*)
CK_SCU_XOSC	13 MHz	13 MHz	For HPADC
CK_SCU_RC8M	8 MHz	8 MHz	For HPADC
CK_SCU_U32KL	32 kHz	32 kHz	For LPADC
CK_SCU_U32KH	32 kHz	32 kHz	For HPADC

^(1*) For CK_SCU_SCU and CK_SCU_SCU_SC, refer to Section of the Clock Control described in Chapter of the SCU (3.9).

The following describes the schematic diagram of the clock control.

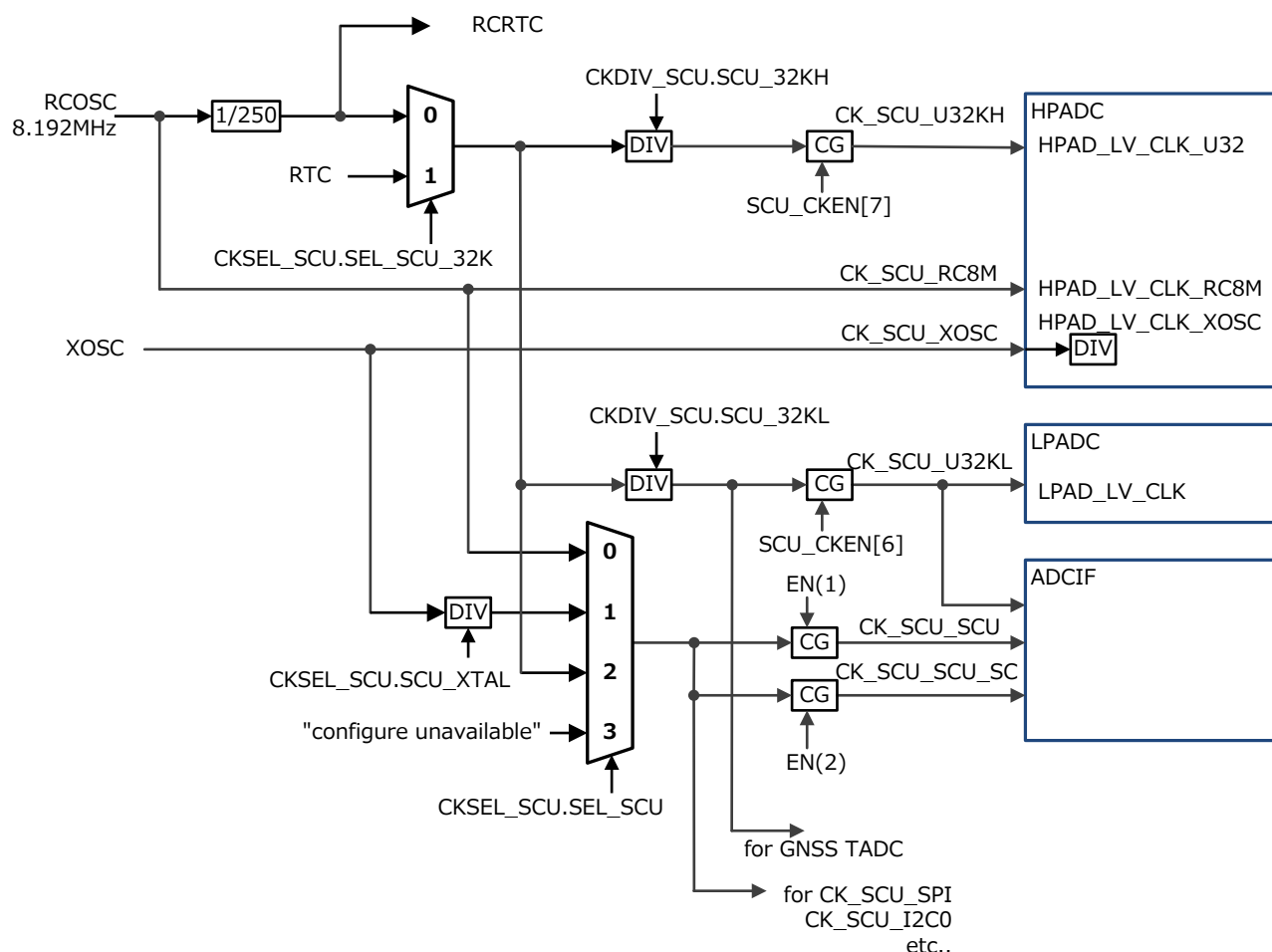


Figure ADC-120 Schematic Diagram of the Clock Control

Clocks supplied to the HPADC and the LPADC are controlled by the following register.

Table ADC-774 Clock Control Register List

Control from	Block Name	Register Name	Offset	Comment
CPU	TOPREG	SCU_CKEN	0x071c	TOPREG control area

For EN(1) and EN(2) in Figure ADC-120, and the summary of clock source selection, refer to Section of the Clock Control described in Chapter of the SCU (3.9).

3.21.5.2 Clock for the LPADC

- CK_SCU_U32KL

This is a clock to determine the sampling frequency of the LPADC.

CK_SCU_U32KL is generated in the CRG (Clock Reset Generator), and it is divided CK_SCU_32K (low speed logic system clock) by 2^n ($n = 0$ to 15). For the range of the available sampling frequencies, refer to Table ADC-810.

The API enables to select clock sources and to control selecting division ratio of CK_SCU_U32KL.

3.21.5.3 Clock for the HPADC

- CK_SCU_XOSC
- CK_SCU_RC8M
- CK_SCU_U32KH

One of the above three clocks is used for the sampling frequency of the HPADC.

CK_U32KH is made, in the CRG outside the SCU, by dividing CK_SCU_32K (low speed logic system clock) by 2^n ($n = 0$ to 15). The frequency division can be set independently from CK_SCU_U32KL of the clock for the LPADC.

CK_SCU_XOSC is the oscillation clock of the crystal oscillator which is connected outside the LSI.

The oscillation clock of the RCOSC is input to CK_SCU_RC8M.

The API enables to select clock sources and to control selecting division ratio of CK_SCU_U32KH.

The ADCIF register actually controls to select which clock should be used for sampling frequency of the HPADC. In addition, the frequency division of CK_SCU_XOSC and CK_SCU_RC8M can be set in the HPADC, and the setting is controlled by the ADCIF register in the SCU as well.

The following describes the summary of input clock selection.

Table ADC-775 Input Clock Selection

Clock Source	Divider Circuit	Clock Port	Remarks
RCRTC (RCOSC divided by 250)	Select one number from 1, 2, 4, ...,32768 to divide frequency	CK_SCU_32KL	For LPADC
	Select one number from 1, 2, 4, ...,32768 to divide frequency	CK_SCU_32KH	For HPADC
RCOSC	None	CK_SCU_RC8M	For HPADC
XOSC	None	CK_SCU_XOSC	For HPADC

3.21.5.4 Clock Control of the ADCIF

In the case that the HPADC in the SCU is not operated by the RCOSC while the RCOSC is ON, the power consumption of the clock in the ADCIF can be reduced by writing “1” in RCOSC_CTRL1. IRO_LV_SENSCLK_XEN, which is in 0x0590 region of the ADCIF.

3.21.5.5 CPU's Clock Control to SCU

When you import the data for the ADC by using a sequencer inside the SCU, you must pay attention to the clock supply to the SCU.

For details, refer to Section 3.9.4.6, Clock Control from Internal Sequencers described in Chapter of the CPU.

3.21.6 Reset Control

The following describes main reset control of the LPADC and the HPADC.

For Peripheral Name information, refer to Table Memory Mapping-2 of the section 2.6.2, Memory Map of each block.

Table ADC-776 Main Reset Control

Target	Peripheral Name	Address	bit	Name	Set Value	Remarks
LPADC	PMU, CRG, GPIO, I/O Config	0x0704	[4]	XRST_SCU_LPADC	1'b1	0: Reset
HPADC	PMU, CRG, GPIO, I/O Config	0x0704	[2]	XRST_SCU_HPADC	1'b1	1: Reset release

3.21.7 Interrupt

The ADCIF is equipped in the SCU. For the details of the interrupt, refer to the chapter 3.3, Interrupt.

3.21.8 FIFO writing Process

The following describes the data flow.

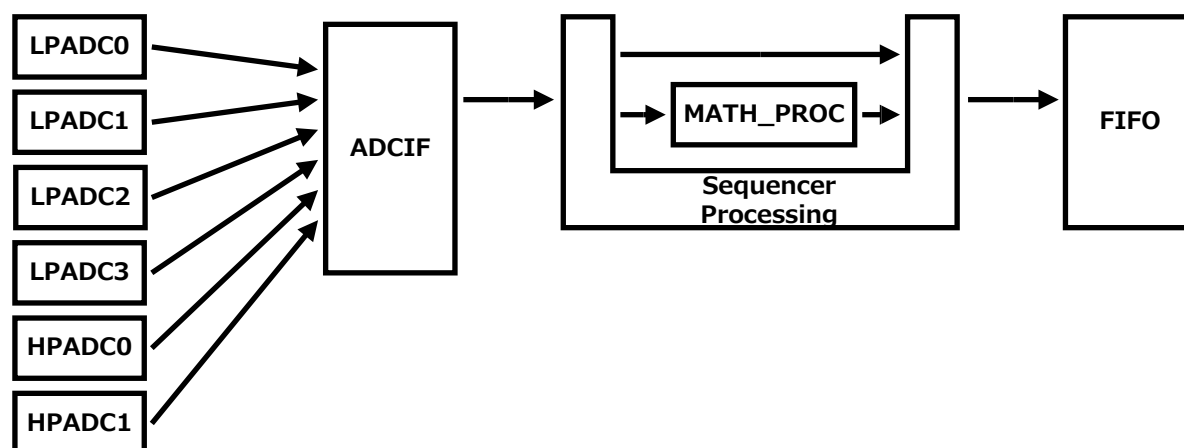


Figure ADC-121 Data Flow of the ADC

After being started, the ADC refers the status of the NOT_EMPTY interrupt from the ADCIF, then begins to move. When the status is NOT_EMPTY, the ADC reads out the data and transfer them to the Write FIFO in the SCU.

When the end of operation is notified (when a parameter `ADC_PROPERTY.*_ENABLE` in the `SCU_RAM` is changed from “1” to “0”), the ADC reads out the corresponding data of `SCU_ADCIF_FIFO` until the FIFO becomes EMPTY, then discards them. The function is prepared so that unnecessary data cannot be read out even if the ADC is rebooted without resetting the `SCU_ADCIF_FIFO`.

The sample of the HPADC is processed every eight samples at a time. Accordingly, the time stamp per sample cannot be recorded correctly. The fluctuation of the time stamp when eight samples are processed at a time can be minimized by making the number of the DMA's Watermark multiple of the eight samples. However, the following fluctuation will occur if the samples are written during time stamp's reading out even when making the number of the DMA's Watermark multiple of the eight samples.

$$(\text{The remaining number of the 8-FIFO data} \% 8) \times (\text{INTERVAL}[\text{sec}] - 165/\text{scu\_clock\_freq}[\text{Hz}])$$

In this formula, INTERVAL means sample's interval (second).

3.21.9 Gain Control

3.21.9.1 Gain Control of the LPADC

The LPADC has a fixed voltage range, there is no gain control. Input the data with appropriate signal level based on the LSI's specifications, and perform appropriate signal processing after importing the data.

3.21.9.2 Gain Control of the HPADC

Gain control of the HPADC is performed in registers `LV_LPFn_ATT_SEL`, `LV_LPFn_GAIN1ST`, and `LV_LPFn_GAIN2ND` (n = 0,1).

Table ADC-777 Gain Control of the HPADC

Function Name	Control Register Name (n = 0, 1)		
LPF Gain setting	<code>LV_LPFn_ATT_SEL</code>	<code>LV_LPFn_GAIN1ST</code>	<code>LV_LPFn_GAIN2ND</code>
-6dB	2'b10	4'b0000	4'b0000
0dB	2'b00	4'b0000	4'b0000
6dB	2'b00	4'b0100	4'b0000
12dB	2'b00	4'b1100	4'b0000
14dB	2'b00	4'b0100	4'b1000

The combinations of setting other than the setting listed in Table ADC-817 are prohibited. Use the designated combinations of setting.

The following describes gain control overview.

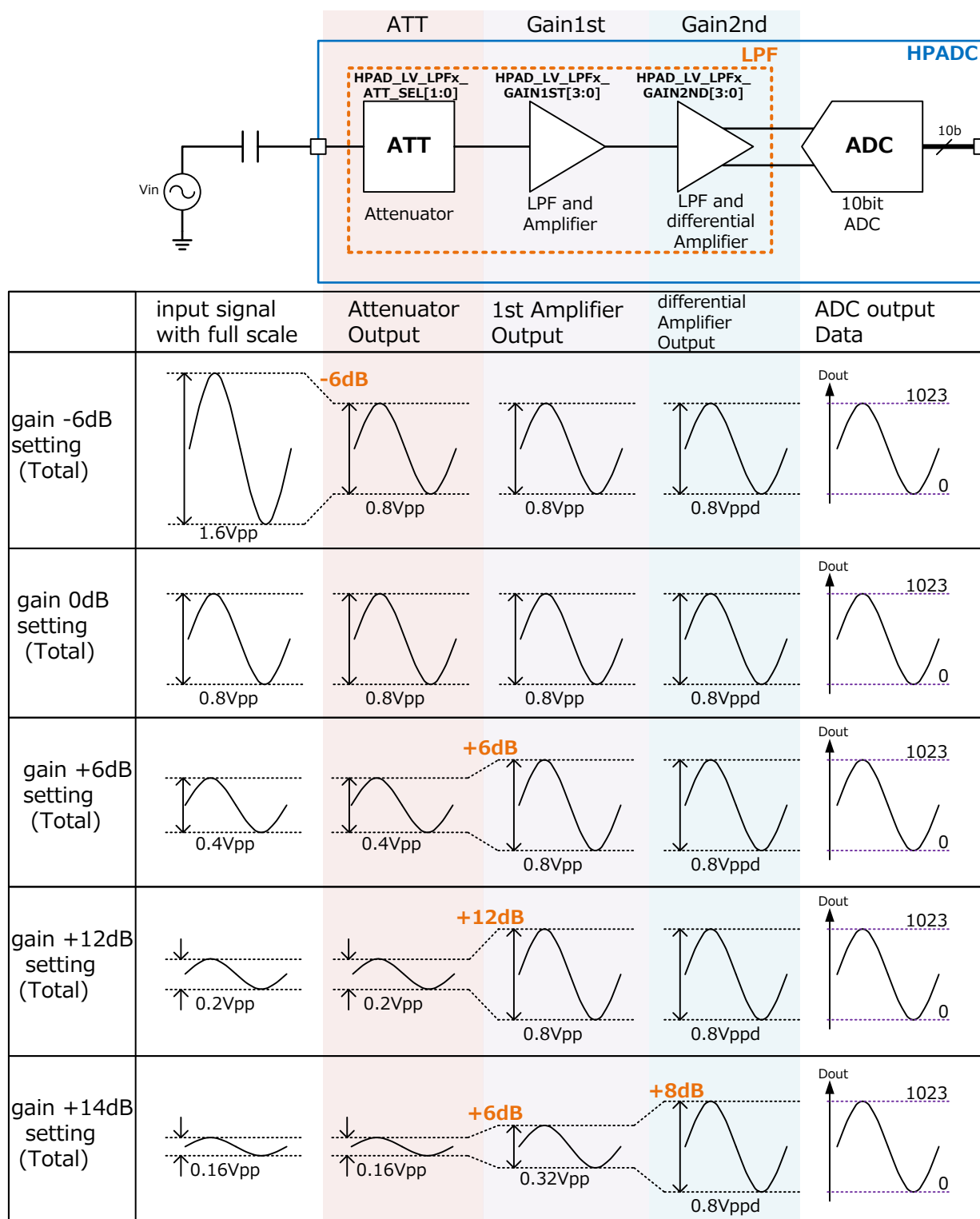


Figure ADC-122 HPADC Gain Control Overview

3.21.10 Performance Estimation

The following describes the performance estimation of the maximum sampling frequency.

Table ADC-778 ADC Sampling Frequency Estimation

SCU Main Clock(Hz)	Resource/Mode	With Sensor Operation (Hz)	Without Sensor Operation (Hz)	Remarks
32,768	LPADC/1CH	25	27	
	LPADC/2CH	15	17	
	LPADC/4CH	8	9	
	HPADC	90	100	
8,192,000	LPADC/1CH	5,500	6,500	
	LPADC/2CH	512	512	ADC HW performance bottleneck
	LPADC/4CH	256	256	ADC HW performance bottleneck
	HPADC	22,000	26,000	
13,000,000	LPADC/1CH	9,500	11,000	
	LPADC/2CH	512	512	ADC HW performance bottleneck
	LPADC/4CH	256	256	ADC HW performance bottleneck
	HPADC	37,000	41,000	

- The following describes the sensor conditions with sensor operation.
 - Six byte read transfer per event for each sensor (three axes are assumed)
 - The total of the sampling frequencies of all SPI sensors is 820 Hz (1 Hz when the clock is 32 kHz)
 - The total of the sampling frequencies of all I2C sensors is 180 Hz (1 Hz when the clock is 32 kHz)
 - The SPI's transfer rate is about 4 Mbps, and the I2C's transfer rate is about 400 Kbps (The SPI's is about 16Kbps, and the I2C's is about 1.4 Kbps, when the clock is 32 kHz)

Caution: When you use the XOSC for sampling clock of the ADC, set the decimation filter so that the frequencies are less than the supported frequencies shown above.

In the meantime, the following describes the worst cases of the sensors estimated on the typical HPADC/LPADC scenario.

Table ADC-779 ADC Sensor Sampling Frequency Estimation

SCU Clock(Hz)	HPADC(Hz)	LPADC(Hz)	SPI Sensor (Hz)	I2C Sensor (Hz)
32,768	0	0	16	0
8,192,000	16,384	250	1,500	500
13,000,000	16,384	250	3,500	1,000

The following describes the sensor conditions with sensor operation.

- Six byte read transfer per event for each sensor (three axes are assumed)
The SPI's transfer rate is about 4 Mbps, the I2C's transfer rate is about 400 Kbps (The SPI's is about 16 Kbps, the I2C's is about 1.4 Kbps when the clock is 32 kHz.)

3.21.11 Synchronization Function with PWM

3.21.11.1 PWM Output Based on ADC

The PWM output can be performed based on the AD data confirmation signals (synchronization signals) from the ADC (LPADC/HPADC). For details, refer to Section 3.9.11, PWM Control described in Chapter of the SCU.

3.21.11.2 ADC Data Import Based on the PWM Output

Based on the rise of the PWM output, timing of importing the ADC data in the SCU can be controlled. For details, refer to Section of PWM Control described in Chapter of the SCU (3.9).

3.21.12 ADC Control Register Details

3.21.12.1 SCU_ADCIF_REG

The following describes the 32 bit address offset. Add this address to the offset addresses in the table shown below to calculate the address from the CPU.

Offset:0x0018dc00 (Mirror:0x0418dc00)

Table ADC-780 SCU_ADCIF_REG Register List

Offset (Transaction Port)	Address	Name	Type	Size (bits)	Description	Reset Value
0x200		LPADC_A0	RW	32	LPADC enable control	0x00000000
0x204		LPADC_A1	RW	32	LPADC channel switching control	0x00000000
0x210		LPADC_D0	RW	32	LPADC software reset	0x00000000
0x214		LPADC_D1	RW	32	LPADC basic setting	0x00000008
0x218		LPADC_D2	RW	32	Permission/prohibition of the LPADC ADC data acceptance	0x00000000
0x21C		LPADC_D4	RW	32	LPADC basic setting	0x00000008
0x220		LPADC_D5	RW	32	LPADC basic setting	0x00000008
0x224		LPADC_D6	RW	32	LPADC basic setting	0x00000008
0x240		HPADC_AC0	RW	32	HPADC common clock control	0x00000000
0x244		HPADC_AC1	RW	32	HPADC common enable control	0x00000000
0x250		HPADC_DC	RW	32	Permission/prohibition of handling two element vector	0x00000000
0x280		HPADC0_A0	RW	32	HPADC0 clock selection	0x00000000
0x284		HPADC0_A1	RW	32	HPADC0 enable control	0x00000000
0x288		HPADC0_A2	RW	32	HPADC0 clock enable control	0x00000000
0x28C		HPADC0_A3	RW	32	HPADC0 LPF control	0x00000100
0x290		HPADC0_D0	RW	32	HPADC0 software reset	0x00000000
0x294		HPADC0_D1	RW	32	HPADC0 basic setting	0x00000010
0x298		HPADC0_D2	RW	32	Permission/prohibition of the HPADC0 ADC data acceptance	0x00000000
0x2C0		HPADC1_A0	RW	32	HPADC1 clock selection	0x00000000
0x2C4		HPADC1_A1	RW	32	HPADC1 enable control	0x00000000
0x2C8		HPADC1_A2	RW	32	HPADC1 clock enable control	0x00000000
0x2CC		HPADC1_A3	RW	32	HPADC1 LPF control	0x00000100
0x2D0		HPADC1_D0	RW	32	HPADC1 software reset	0x00000000
0x2D4		HPADC1_D1	RW	32	HPADC1 basic setting	0x00000010
0x2D8		HPADC1_D2	RW	32	Permission/prohibition of the HPADC1 ADC data acceptance	0x00000000
0x3D0		ADCIF_DCT	RO	32	SCU_ADCIF register map revision code	0xADC1F000
0x3D4		SCU_ADCIF_C KPOWER	RW	32		0x00000001

3.21.12.1.1 {0x200} LPADC_A0 Details

LPADC Enable Control

Table ADC-781

Local Address: 0x200																Register Type: RW (read/write) Reset Value: 0x00000000																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Reserved																														LV_ADC_EN				
Bits		Name				Type	Reset Value				Description																							
31..1		Reserved				RO	0x00000000				Reserved																							
0		LV_ADC_EN				RW	0x0				Permission/prohibition of the LPADC operation Switching between standby and move 1'b0: standby 1'b1: active (default)																							

3.21.12.1.2 {0x204} LPADC_A1 Details

LPADC Channel Switching Control

Table ADC-782

Local Address: 0x204																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																LV_CH_SEL_INV		Reserved						LV_CH_SEL_MODE							
Bits				Name				Type		Reset Value				Description																	
31..10				Reserved				RO		0x000000				Reserved																	
9..8				LV_CH_SEL_INV				RW		0x0				ADCH selector for GNSS (sets only a CH which are in operation shown below) 2'b00 CH0 2'b01 CH1 2'b10 CH2 2'b11 CH3																	
7..3				Reserved				RO		0x00				Reserved																	
2..0				LV_CH_SEL_MODE				RW		0x0				LPADC channel switching mode 3'b000 CH0 3'b001 CH1 3'b010 CH2 3'b011 CH3 3'b100 CH0 => CH1 3'b101 CH0 => CH1=> CH2=> CH3																	

3.21.12.1.3 {0x210} LPADC_D0 Details

LPADC Software Reset

Table ADC-783

Local Address: 0x210																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														SW_RESET	
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		SW_RESET				RW	0x0				LPADC software reset common to each LPADC																				

3.21.12.1.4 {0x214} LPADC_D1 Details

LPADC Basic Setting

Table ADC-784

Local Address: 0x214																				Register Type: RW (read/write)											
																				Reset Value: 0x00000008											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								SAMP_RATIO2								SAMP_RATIO				Reserved		DMA_HS_EN		Reserved		FIFO_WATERMARK					
Bits	Name							Type	Reset Value							Description															
31..21	Reserved							RO	0x000							Reserved															
20..12	SAMP_RATIO2							RW	0x000							Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized															
11..8	SAMP_RATIO							RW	0x0							LPADC sampling ratio selection (0: No frequency division, 1: 1/2, ..., 15: 1/32768)															
7..6	Reserved							RO	0x0							Reserved															

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using LPADC DMA signals
4	Reserved	RO	0x0	Reserved
3..0	FIFO_WATERMARK	RW	0x8	LPADC FIFO Watermark Determination of the DMA traffic

3.21.12.1.5 {0x218} LPADC_D2 Details

Permission/Prohibition of the LPADC ADC Data Acceptance

Table ADC-785

Local Address: 0x218																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										FIFO_EN					
Bits		Name				Type	Reset Value				Description																				
31..4		Reserved				RO	0x00000000				Reserved																				
3..0		FIFO_EN				RW	0x0				Permission/prohibition of the LPADC FIFO operation																				

3.21.12.1.6 {0x21C} LPADC_D4 Details

LPADC Basic Setting

Table ADC-786

Local Address: 0x21C																				Register Type: RW (read/write)											
																				Reset Value: 0x00000008											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								SAMP_RATIO2								SAMP_RATIO				Reserved		DMA_HS_EN		Reserved		FIFO_WATERMARK					
Bits	Name							Type	Reset Value							Description															
31..21	Reserved							RO	0x000							Reserved															
20..12	SAMP_RATIO2							RW	0x000							Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized															
11..8	SAMP_RATIO							RW	0x0							HPADC sampling ratio selection (0: No frequency division, 1: 1/2, -, 15: 1/32768)															
7..6	Reserved							RO	0x0							Reserved															

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using LPADC DMA signals
4	Reserved	RO	0x0	Reserved
3..0	FIFO_WATERMARK	RW	0x8	LPADC FIFO Watermark Determination of the DMA traffic

3.21.12.1.7 {0x220} LPADC_D5 Details

LPADC Basic Setting

Table ADC-787

Local Address: 0x220																				Register Type: RW (read/write)											
																				Reset Value: 0x00000008											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								SAMP_RATIO2								SAMP_RATIO				Reserved		DMA_HS_EN		Reserved		FIFO_WATERMARK					
Bits	Name							Type	Reset Value			Description																			
31..21	Reserved							RO	0x000			Reserved																			
20..12	SAMP_RATIO2							RW	0x000			Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized																			
11..8	SAMP_RATIO							RW	0x0			HPADC sampling ratio selection (0: No frequency division, 1: 1/2, -, 15: 1/32768)																			
7..6	Reserved							RO	0x0			Reserved																			

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using LPADC DMA signals
4	Reserved	RO	0x0	Reserved
3..0	FIFO_WATERMARK	RW	0x8	LPADC FIFO Watermark Determination of the DMA traffic

3.21.12.1.8 {0x224} LPADC_D6 Details

LPADC Basic Setting

Table ADC-788

Local Address: 0x224																				Register Type: RW (read/write)											
																				Reset Value: 0x00000008											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6		5 4		3 2		1 0	
Reserved								SAMP_RATIO2								SAMP_RATIO				Reserved		DMA_HS_EN		Reserved		FIFO_WATERMARK					
Bits	Name							Type	Reset Value							Description															
31..21	Reserved							RO	0x000							Reserved															
20..12	SAMP_RATIO2							RW	0x000							Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized															
11..8	SAMP_RATIO							RW	0x0							HPADC sampling ratio selection (0: No frequency division, 1: 1/2, -, 15: 1/32768)															
7..6	Reserved							RO	0x0							Reserved															

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using LPADC DMA signals
4	Reserved	RO	0x0	Reserved
3..0	FIFO_WATERMARK	RW	0x8	LPADC FIFO Watermark Determination of the DMA traffic

3.21.12.1.9 {0x240} HPADC_AC0 Details

Clock Control Common to the HPADC

Table ADC-789

Local Address: 0x240																Register Type: RW (read/write) Reset Value: 0x00000000															
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved																LV_CLK_XOSC_DIV				Reserved				LV_CLK_OSC_SEL							
Bits	Name			Type	Reset Value			Description																							
31..6	Reserved			RO	0x0000000			Reserved																							
5..4	LV_CLK_XOSC_DIV			RW	0x0			Division ratio setting port when using the XOSC clock 0: clock divided by 2, 1: clock divided by 3 2: clock divided by 4 3: clock divided by 6																							
3..1	Reserved			RO	0x0			Reserved																							
0	LV_CLK_OSC_SEL			RW	0x0			Clock selection port when performing high speed sampling 0: XOSC 1: RCOSC																							

3.21.12.1.10 {0x244} HPADC_AC1 Details

Enable Control Common to the HPADC

Table ADC-790

Local Address: 0x244																Register Type: RW (read/write) Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved																																LV_BGR_EN
Bits		Name				Type	Reset Value				Description																					
31..1		Reserved				RO	0x00000000				Reserved																					
0		LV_BGR_EN				RW	0x0				LV BGR Circuit Enable Switching between standby and move 1'b0: standby 1'b1: active (default)																					

3.21.12.1.11 {0x250} HPADC_DC Details

Permission/Prohibition of Handling Two Element Vector

Table ADC-791

Local Address: 0x250														Register Type: RW (read/write) Reset Value: 0x00000000																			
31 30 29 28 27 26 25 24							23 22 21 20 19 18 17 16							15 14 13 12 11 10 9 8							7 6 5 4 3 2 1 0												
Reserved																												VECTOR_SEL					
Bits				Name				Type		Reset Value				Description																			
31..1				Reserved				RO		0x00000000				Reserved																			
0				VECTOR_SEL				RW		0x0				Permission/prohibition of handling two element vector																			

3.21.12.1.12 {0x280} HPADC0_A0 Details

HPADC0 Clock Selection

Table ADC-792

Local Address: 0x280														Register Type: RW (read/write) Reset Value: 0x00000000																	
31 30 29 28 27 26 25 24							23 22 21 20 19 18 17 16							15 14 13 12 11 10 9 8							7 6 5 4 3 2 1 0										
Reserved																															LV_CLK_U32_SEL0
Bits	Name			Type	Reset Value			Description																							
31..1	Reserved			RO	0x00000000			Reserved																							
0	LV_CLK_U32_SEL0			RW	0x0			Clock selection port 0: high speed clock 1: low speed clock																							

3.21.12.1.13 {0x284} HPADC0_A1 Details

HPADC0 Enable Control

Table ADC-793

Local Address: 0x284																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										LV_ADC0_REF_EN		LV_LPF0_EN		LV_ADC0_EN	
Bits	Name					Type	Reset Value					Description																			
31..3	Reserved					RO	0x00000000					Reserved																			
2	LV_ADC0_REF_EN					RW	0x0					ADC0 REF circuit enable port Setting for the ADC reference and operation mode (0,0) standby (0,1) external enable (1,0) active (default) (1,1) active																			
1	LV_LPF0_EN					RW	0x0					LPF0 enable control port (0,0) standby (0,1) standby (1,0) active (default) (1,1) prohibited setting																			
0	LV_ADC0_EN					RW	0x0					Permission/Prohibition of the HPADC0 operation 1'b0: standby 1'b1: active (default)																			

3.21.12.1.14 {0x288} HPADC0_A2 Details

HPADC0 Clock Enable Control

Table ADC-794

Local Address: 0x288																Register Type: RW (read/write)															
																Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															LV_CLKOUT0_EN
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		LV_CLKOUT0_EN				RW	0x0				ADC0 clock output enable port																				

3.21.12.1.15 {0x28C} HPADC0_A3 Details

HPADC0 ADC and LPF Control

Table ADC-795

Local Address: 0x28C																		Register Type: RW (read/write)																																																																																					
																		Reset Value: 0x00000100																																																																																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																																																								
Reserved								LV_LPF0_ATT_SEL								Reserved								LV_LPF0_MODE								LV_LPF0_GAIN2ND								LV_LPF0_GAIN1ST								LV_LPF0_FC								Reserved								LV_LPF0_XSTARTUP								LV_ADC0_REFCTRL								Reserved								LV_ADC0_REFLP_EN								LV_ADC0_PREAMPLP_EN							
Bits	Name										Type	Reset Value						Description																																																																																					
31..26	Reserved										RO	0x00						Reserved																																																																																					
25..24	LV_LPF0_ATT_SEL										RW	0x0						Attenuator gain switching at LPF input part Refer to Section 3.21.9.1 2'b00: x1 (default) 2'b01: x0.75 2'b10: x0.5 2'b11: x0.25 (prohibited setting)																																																																																					
23	Reserved										RO	0x0						Reserved																																																																																					
22..20	LV_LPF0_MODE										RW	0x0						Switching port of the LPF current setting Bias current value switching 3'b000: 0.4uA (default) 3'b001: 0.5uA 3'b010: 0.6uA 3'b011: 0.7uA 3'b100: 0.8uA 3'b101: 0.1uA 3'b110: 0.2uA 3'b111: 0.3uA																																																																																					

19..16	LV_LPF0_GAIN2ND	RW	0x0	LPF gain switching function (differential amplifier) Refer to Section 3.21.9.1. 4'b0000: x1 (default) 4'b0001: x1.08 4'b0010: x1.18 4'b0011: x1.29 4'b0100: x1.43 4'b0101: x1.6 4'b0110: x1.82 4'b0111: x2.1 4'b1000: x2.5 4'b1001: x3.08 4'b1010: x4 4'b1011: x0.83 4'b1100: x0.71 4'b1101: x0.63 4'b1110: x0.56 4'b1111: x0.5
15..12	LV_LPF0_GAIN1ST	RW	0x0	LPF gain switching function (first stage amplifier) Refer to Section 3.21.9.1. 4'b0000: x1 (default) 4'b0001: x1.25 4'b0010: x1.5 : 4'b1110: x4.5 4'b1111: x4.75
11..10	LV_LPF0_FC	RW	0x0	LPF frequency band switching function 2'b00: 75 kHz (default) 2'b01: 150 kHz 2'b10: 37.5 kHz 2'b11: No LPF, Amplifier only
9	Reserved	RO	0x0	Reserved
8	LV_LPF0_XSTARTUP	RW	0x1	LPF0 input common startup function 1'b0: startup enable 1'b1: startup disable (default)

7..4	LV_ADC0_REFCTRL	RW	0x0	REF voltage regulator port Reference gm adjustment 4'b0000: ADC0 X1, ADC1 X1 (default) 4'b0001: X2, X1 4'b0010: X3, X1 4'b0011: X4, X2 4'b0100: X1, X2 4'b0101: X2, X2 4'b0110: X3, X2 4'b0111: X4, X2 4'b1000: X3, X1 4'b1001: X3, X2 4'b1010: X3, X3 4'b1011: X3, X4 4'b1100: X1, X4 4'b1101: X2, X4 4'b1110: X3, X4 4'b1111: X4, X4
3..2	Reserved	RO	0x0	Reserved
1	LV_ADC0_REFLP_EN	RW	0x0	Low power mode signal of the voltage reference circuit (0,0) Standby (0,1) Standby (1,0) active (default) (1,1) Prohibited setting
0	LV_ADC0_PREAMPLP_EN	RW	0x0	ADC0 PreAMP low power mode signal Control used when monitoring the ADC sampling clock via the ATB 1'b0: off (default) 1'b1: on

3.21.12.1.16 {0x290} HPADC0_D0 Details

HPADC0 Software Reset

Table ADC-796

Local Address: 0x290																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															SW_RESET
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		SW_RESET				RW	0x0				HPADC0 software reset																				

3.21.12.1.17 {0x294} HPADC0_D1 Details

HPADC0 Basic Setting

Table ADC-797

Local Address: 0x294																				Register Type: RW (read/write)									
																				Reset Value: 0x00000010									
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8				7 6		5 4		3 2		1 0			
Reserved								DECI_RATIO2								Reserved		DECI_RATIO		Reserved		DMA_HS_EN		FIFO_WATERMARK					
Bits	Name							Type	Reset Value			Description																	
31..21	Reserved							RO	0x000			Reserved																	
20..12	DECI_RATIO2							RW	0x000			Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized																	
11	Reserved							RO	0x0			Reserved																	
10..8	DECI_RATIO							RW	0x0			HPADC0 decimation ratio selection (0: No frequency division, 1: 1/2, ..., 7: 1/128)																	
7..6	Reserved							RO	0x0			Reserved																	

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using HPADC0 DMA signals
4..0	FIFO_WATERMARK	RW	0x10	HPADC0 FIFO Watermark

3.21.12.1.18 {0x298} HPADC0_D2 Details

Permission/Prohibition of the HPADC0 ADC Data Acceptance

Table ADC-798

Local Address: 0x298																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															DECIFIFO_EN
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		DECIFIFO_EN				RW	0x0				Permission/prohibition of the HPADC0 Decimation and FIFO operation																				

HPADC1 Clock Selection

Table ADC-799

Local Address: 0x2C0																Register Type: RW (read/write)																
																Reset Value: 0x00000000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved																																LV_CLK_U32_SEL1
Bits		Name				Type	Reset Value				Description																					
31..1		Reserved				RO	0x00000000				Reserved																					
0		LV_CLK_U32_SEL1				RW	0x0				Clock selection port 0: high speed clock, 1: low speed clock																					

3.21.12.1.20 {0x2C4} HPADC1_A1 Details

HPADC1 Enable Control

Table ADC-800

Local Address: 0x2C4																						Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																												LV_ADC1_REF_EN	LV_LPF1_EN	LV_ADC1_EN							
Bits		Name				Type	Reset Value				Description																										
31..3		Reserved				RO	0x00000000				Reserved																										
2		LV_ADC1_REF_EN				RW	0x0				ADC1 REF circuit enable port ADC reference operation mode setting (0,0) standby (0,1) external enable (1,0) active (default) (1,1) active																										
1		LV_LPF1_EN				RW	0x0				LPF1 enable control port (0,0) standby (0,1) standby (1,0) active (default) (1,1) prohibited setting																										
0		LV_ADC1_EN				RW	0x0				Permission/prohibition of the HPADC1 operation 1'b0: standby 1'b1: active (default)																										

3.21.12.1.21 {0x2C8} HPADC1_A2 Details

HPADC1 Clock Enable Control

Table ADC-801

Local Address: 0x2C8																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															LV_CLKOUT1_EN
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		LV_CLKOUT1_EN				RW	0x0				ADC1 clock output enable port																				

3.21.12.1.22 {0x2CC} HPADC1_A3 Details

HPADC1 LPF Control

Table ADC-802

Local Address: 0x2CC																		Register Type: RW (read/write)																																																													
																		Reset Value: 0x00000100																																																													
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0																																																							
Reserved								LV_LPF1_ATT_SEL				Reserved				LV_LPF1_MODE				LV_LPF1_GAIN2ND				LV_LPF1_GAIN1ST				LV_LPF1_FC				Reserved				LV_LPF1_XSTARTUP				LV_ADC1_REFCTRL				Reserved				LV_ADC1_REFLP_EN				LV_ADC1_PREAMPLP_EN																											
Bits		Name						Type		Reset Value						Description																																																															
31..26		Reserved						RO		0x00						Reserved																																																															
25..24		LV_LPF1_ATT_SEL						RW		0x0						Attenuator gain switching at LPF input part Refer to Section 3.21.9.1 2'b00: x1 (default) 2'b01: x0.75 2'b10: x0.5 2'b11: x0.25 (prohibited setting)																																																															
23		Reserved						RO		0x0						Reserved																																																															
22..20		LV_LPF1_MODE						RW		0x0						Switching port of the LPF current setting Bias current value switching 3'b000: 0.4uA (default) 3'b001: 0.5uA 3'b010: 0.6uA 3'b011: 0.7uA 3'b100: 0.8uA 3'b101: 0.1uA 3'b110: 0.2uA 3'b111: 0.3uA																																																															

19..16	LV_LPF1_GAIN2ND	RW	0x0	LPF gain switching function (differential amplifier) Refer to Section 3.21.9.1. 4'b0000: x1 (default) 4'b0001: x1.08 4'b0010: x1.18 4'b0011: x1.29 4'b0100: x1.43 4'b0101: x1.6 4'b0110: x1.82 4'b0111: x2.1 4'b1000: x2.5 4'b1001: x3.08 4'b1010: x4 4'b1011: x0.83 4'b1100: x0.71 4'b1101: x0.63 4'b1110: x0.56 4'b1111: x0.5
15..12	LV_LPF1_GAIN1ST	RW	0x0	LPF gain switching function (first stage amplifier) Refer to Section 3.21.9.1. 4'b0000: x1 (default) 4'b0001: x1.25 4'b0010: x1.5 : 4'b1110: x4.5 4'b1111: x4.75
11..10	LV_LPF1_FC	RW	0x0	LPF frequency band switching function 2'b00: 75 kHz (default) 2'b01: 150 kHz 2'b10: 37.5 kHz 2'b11: No LPF, Amplifier only
9	Reserved	RO	0x0	Reserved
8	LV_LPF1_XSTARTUP	RW	0x1	LPF input common startup function 1'b0: startup enable 1'b1: startup disable (default)

7..4	LV_ADC1_REFCTRL	RW	0x0	REF voltage regulator port <3> reference destination switching 1'b0: internal 0.7 V system power supply (default) 1'b1: external enable power supply via the ATB <2:0> BGR output voltage switching 3'b000: 700mV (default) 3'b001: 750mV 3'b010: 800mV 3'b011: 850mV 3'b100: 500mV 3'b101: 550mV 3'b110: 600mV 3'b111: 650mV
3..2	Reserved	RO	0x0	Reserved
1	LV_ADC1_REFLP_EN	RW	0x0	Low power mode signal of the REF circuit (0,0) standby (0,1) standby (1,0) active (default) (1,1) prohibited setting
0	LV_ADC1_PREAMPLP_EN	RW	0x0	ADC1 PreAMP low power mode signal Control used when monitoring the ADC sampling clock via the ATB 1'b0: off (default) 1'b1: on

3.21.12.1.23 {0x2D0} HPADC1_D0 Details

HPADC1 Software Reset

Table ADC-803

Local Address: 0x2D0																Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															SW_RESET
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		SW_RESET				RW	0x0				HPADC1 software reset																				

3.21.12.1.24 {0x2D4} HPADC1_D1 Details

HPADC1 Basic Setting

Table ADC-804

Local Address: 0x2D4																				Register Type: RW (read/write)											
																				Reset Value: 0x00000010											
31 30 29 28 27 26 25 24								23 22 21 20 19 18 17 16								15 14 13 12 11 10 9 8								7 6 5 4 3 2 1 0							
Reserved								DECI_RATIO2								Reserved		DECI_RATIO		Reserved		DMA_HS_EN		FIFO_WATERMARK							
Bits	Name							Type	Reset Value							Description															
31..21	Reserved							RO	0x000							Reserved															
20..12	DECI_RATIO2							RW	0x000							Bit0 Synchronization signal from the PWM0 is enabled Bit1 Synchronization signal from the PWM1 is enabled Bit2 Synchronization signal from the PWM2 is enabled Bit3 Synchronization signal from the PWM3 is enabled Bit4 Synchronization signal from the PWM4 is enabled Bit5 Synchronization signal from the PWM5 is enabled Bit6 Synchronization signal from the PWM6 is enabled Bit7 Synchronization signal from the PWM7 is enabled Bit8 0: not synchronized															
11	Reserved							RO	0x0							Reserved															
10..8	DECI_RATIO							RW	0x0							HPADC1 decimation ratio selection (0: No frequency division, 1: 1/2, ..., 7: 1/128)															
7..6	Reserved							RO	0x0							Reserved															

5	DMA_HS_EN	RW	0x0	Permission/prohibition of using HPADC1 DMA signals
4..0	FIFO_WATERMARK	RW	0x10	HPADC1 FIFO Watermark

3.21.12.1.25 {0x2D8} HPADC1_D2 Details

Permission/Prohibition of the HPADC1 ADC Data Acceptance

Table ADC-805

Local Address: 0x2D8																						Register Type: RW (read/write) Reset Value: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Reserved																																DECIFIFO_EN					
Bits		Name				Type	Reset Value				Description																										
31..1		Reserved				RO	0x00000000				Reserved																										
0		DECIFIFO_EN				RW	0x0				Permission/prohibition of the HPADC1 Decimation and the FIFO operation																										

3.21.12.1.26 {0x3D0} ADCIF_DCT Details

SCU_ADCIF Register Map Revision Code

Table ADC-806

Local Address: 0x3D0																Register Type: RO (read only) Reset Value: 0xADC1F000																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
REV_CODE																																
Bits		Name						Type	Reset Value						Description																	
31..0		REV_CODE						RO	0xADC1F000						Revision code of the SCU_ADCIF register map (revision of the last three digits)																	

3.21.12.1.27 {0x3D4} SCU_ADCIF_CKPOWER Details

Table ADC-807

Local Address: 0x3D4																Register Type: RW (read/write) Reset Value: 0x00000001															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															CK_POWEREN
Bits		Name				Type	Reset Value				Description																				
31..1		Reserved				RO	0x00000000				Reserved																				
0		CK_POWEREN				RW	0x1				Default clock supply																				

3.21.12.2 SCU_RAM Parameter

For parameters in the SCU_RAM, refer to Chapter of the SCU.

3.21.13 ADC Control Sequence

For the ADC startup and the details of the data transfer, refer to Section 3.9.13 SCU Control Sequence described in Chapter of the SCU.

In addition, for SCU sequencer to which the LPADC and the HPADC can connect, refer to Section of Connectable Sequencer described in Chapter of the SCU (3.9).

3.21.13.1 Setting for transferring the data of the LPADC to the GNSS

The following describes the necessary settings.

{0x200} LPADC_A0 Select “1” when using the LPADC.

{0x204} LPADC_A1 Select the four-channel AD data to send the GNSS. Then select time share processing.

Procedure:

When CK_SCU_SCU is OFF, turn it ON when setting registers.

Set the registers of the LPADC

If necessary, turn CK_SCU_SCU OFF after the setting is completed

Caution: CK_SCU_U32KL is the main clock of the LPADC, therefore, it cannot be stopped when using the LPADC.

3.21.14 Restrictions

3.21.14.1 Delay at the LPADC Startup

When starting the LPADC up, there will be maximum one sampling period of delay until the first sample is taken. The time stamp delays according to the delay of the first sample.

3.21.14.2 Delay at the HPADC Startup

When starting the HPADC up, there will be maximum one sampling period of delay until the first sample is taken. The time stamp delays according to the delay of the first sample.

3.21.14.3 Other Restrictions

For sequencer, MATH_PROC, and the restrictions of the time stamp, refer to Chapter of the SCU (3.9).

3.21.15 Error Handling

Some error interrupts for the ADC may occur. Refer to Section 3.9.14 of the Error Handling described in Chapter of the SCU.

4 Appendix

4.1 Words and Terms

4.1.1 Words and Terms Used in This User Manual

The following describes words and terms used in this user manual.

Table Words and Terms-808 Words and Terms Used in This User Manual

Abbreviation	Word and Terms	Explanation
ADSP	Application Processor	The ADSP is a group of processors equipped with six Cortex [®] -M4. Each of the ADSP are explained in this manual with numbers referred to as from ADSP0 to ADSP5. The ADSP contains Cortex [®] -M4, Interrupt input register, Timer, WDT, SLEEPING signal monitor, and Debug function. The Tile address converter and the memory protection unit are equipped outside the ADSP. (Refer to エラー! 参照元が見つかりません。)
APP	Application Domain	The APP is the functional block of Imaging/2D, Storage/Connectivity, and Audio, equipped with six Arm [®] Cortex [®] -M4 processors with FPU 32 bit RISC, indicated in エラー! 参照元が見つかりません。. Refer to Section 2.5.1 as well.
APP_DSP	---	The APP_DSP corresponds to the functional block of the Application Domain excluding Imaging, Storage, and Audio.
APP MAIN Bus	---	The APP MAIN Bus means the matrix bus which connects Application Processor with the APP SRAM and the APP SUB Bus.
APP SRAM	---	The APP SRAM is 1.5 MByte of SRAM inside the Application Domain.
APP SUB Bus	---	The APP SUB Bus is inside the APP. Refer to エラー! 参照元が見つかりません。.
CRG	Clock and Reset Generator	For details, refer to Chapter 3.5
DSP	---	The ADSP and the GDSP are collectively referred to as the DSP.
fs	---	“fs” means the sampling frequency of the audio data. In this document, it means 48 kHz.
GDSP	GNSS DSP	The GDSP means Cortex [®] -M4 inside the GNSS Domain.
GNSS	GNSS Domain	The GNSS is the GNSS functional block equipped with one Arm [®] Cortex [®] -M4 processor with FPU 32 bit RISC, indicated in エラー! 参照元が見つかりません。.

HPADC	High Performance A/D Converter	The HPADC is the A/D Converter in the CXD5602.
HOST I/F	HOST Interface	The HOST I/F is the format to communicate with the external HOST CPU.
Local AHB	---	The Local AHB is the matrix bus which connects the System and I/O Processor with the SYS SRAM and the SYSTEM Bus.
LPADC	Low Power A/D Converter	The LPADC is the A/D Converter in the CXD5602.
NVIC	Nested Vectored Interrupt Controller	For the NVIC, refer to the following URL. http://infocenter.arm.com/help/topic/com.arm.doc.ddi0337e/Cihcffda.html
PMIC	Power Management IC	The PMIC is the IC to control power supply. As a companion chip for the CXD5602, the CXD5247 is prepared. In this document, the CXD5247 is assumed as the PMIC.
PMU	Power Management Unit	The PMU is the block that performs overall power supply control of the CXD5602. Refer to Chapter 3.4.
POR	Power On Reset	The POR is the reset that is enabled when power is supplied.
RCOSC	---	The RCOSC is the internal oscillator block. Refer to Section 3.5.3.1.
RF	Radio Frequency	The RF is the frequency band of the GNSS signal.
RTC	Real Time Clock	For the RTC, refer to Chapter 3.6
SCU	Sensor Domain	The SCU is the block which is equipped with the HPADC, LPADC, and the interface to the external sensors. Please check エラー! 参照元が見つかりません。 . For details, refer to Chapter 3.9.
Sleep	---	Sleep is the status that any of the power domains of the CXD5602 becomes OFF, or any of the DSPs belonging to the power domains is not in operation.
SYSCPU	System and I/O Processor	The SYSCPU contains Cortex®-M0+, Interrupt input register, Timer, WDT, SLEEPING signal monitor, and Debug function (ITM). The Tile address converter and the memory protection unit are equipped outside the SYSCPU. (Refer to エラー! 参照元が見つかりません。)
SYSIOP	System and IOP Domain	The SYSIOP is the functional block equipped with one Cortex®-M0+, to perform a variety of controls of the CXD5602, indicated in エラー! 参照元が見つかりません。 . Refer to Section 2.5.2 as well.
SYSPLL	---	The SYSPLL is the internal PLL. Refer to Section 3.5.3.3.
SYSTEM Bus	---	The SYSTEM Bus is the BUS inside the SYSIOP. Refer to エラー! 参照元が見つかりません。 .
SYS SRAM	---	The SYS SRAM is 256 KByte of SRAM inside the System and IOP Domain.
Wakeup		Wakeup is the status that the power domains of the CXD5602 becomes ON, or the DSPs belonging to the power domains starts operations.

WDT	Watchdog Timer	The WDT is so called the Watch Dog Timer. It monitors the CPU's operation.
WFI	Wait For Interrupt	The WFI is the status that the power domains of the CXD5602 is waiting for an interrupt to enter into sleep mode.
XOSC	X'tal Oscillator	The XOSC is the internal oscillator block. Refer to Section 3.5.3.2.
---	Processor	“Processor” means Cortex®-M0+ and Arm® Cortex®-M4 processor with FPU 32 bit RISC in the CXD5602.

4.2 Reference

PrimeCell® μ DMA Controller (PL230) Technical Reference Manual

[PrimeCell® DMA Controller \(PL080\)](#) Technical Reference Manual

[PrimeCell® Single Master DMA Controller \(PL081\)](#) Technical Reference Manual

[PrimeCell® Synchronous Serial Port \(PL022\)](#) Technical Reference Manual

[PrimeCell® UART \(PL011\)](#) Technical Reference Manual

Arm® Cortex®-M4 Processor Technical Reference Manual

Cortex®-M4 Devices Generic User Guide

ARMv7-M Architecture Reference Manual

AMBA® Design Kit Technical Reference Manual

Revision History

Date	Revision	Description
2019/07/05	1.0.0	Initial version.

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